Journal of ELECTRICAL ENGINEERING, VOL. 53, NO. 1-2, 2002, 50–53

COMMUNICATIONS

Nth–ORDER ALLPASS FILTERS USING CURRENT CONVEYORS

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A special cell with a general four-port second-kind zero-class current conveyor is presented. The use of this cell for high-order allpass filter design is described. Some two-port realizations using the universal current conveyor are derived. It is shown that the designed network can operate in three different modes. Simulation results illustrate the properties of the proposed filters.

K e y w o r d s: current conveyors, allpass filters, group-delay equilizers

1 INTRODUCTION

The high-order allpass filter can be used as a group-delay equilizer in video and communication applications to compensate the delay in the filter passband. Any transfer function of an nth-order allpass filter has the following form:

$$H(s) = \frac{P(-s)}{P(s)} = A\frac{\sum_{i=0}^{n}(-1)^i\alpha_i s^i}{\sum_{i=0}^{n}\alpha_i s^i}\,. \qquad (1)$$

Here, A is a constant, $P(s)$ is a polynomial of complex frequency variable s with coefficients α_i.

The simplest way how to obtain voltage/current transfer function (1) is the simple cascade approach. However, function $H(s)$ has in this case too many terms. A procedure of circuit realization of eqn. (1) called the *pole-zero mirroring technique* was recently published in [1]. The authors have used $n+2$ special active elements denoted as MO-OTAs (*multi-output operational transadmittance amplifiers*). This filter can operate only in the current mode.

An interesting circuit realization of eqn. (1) can be found in [2]. The network proposed here contains only $n+1$ *current differencing buffered amplifiers* (CDBAs). The voltage transfer function has the canonical form, but the circuit has too many feedback resistors.

We proposed a simple building cell using a GCC element (see Fig. 1), which is suitable for the nth-order allpass filter design. Subscript k in Fig. 1 relates to the serial number of the cell connected in cascade.

The symbol GCC denotes here a general *four-port second-kind zero-class current conveyor*, the schematic symbol of which is shown in Fig. 2 [3]. For the node voltages and node currents of the above element the following relations are valid:

$V_x = a_1V_{y1} + a_2V_{y2}$ (second-kind), $I_x = I^*$, $I_{y1} = I_{y2} = 0$ (zero-class), $I_{z1} = d_1I^*$.

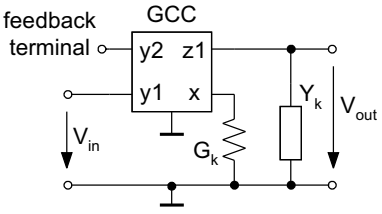

Fig. 1. A building cell

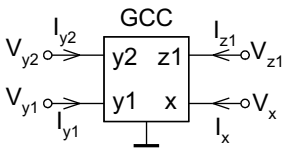

Fig. 2. Schematic symbol of a four-port general current conveyor

Here, I^* is the independent current, whereas the conveyance coefficients a_1, a_2, d_1 are either $+1$ or -1.

2 DESIGN PROCEDURE

Grounding the feedback terminal in Fig. 1, we obtain the voltage transfer function of our cell in the following form:

$$\frac{V_{\rm out}}{V_{\rm in}} = \frac{a_{1k}d_{1k}G_k}{Y_k}\,. \qquad (2)$$

The voltage transfer function of m such cells connected in cascade will therefore be:

$$\frac{V_{\rm out}}{V_{\rm in}} = \prod_{k=1}^{m}\frac{a_{1k}d_{1k}G_k}{Y_k}\,. \qquad (3)$$

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ISSN 1335-3632

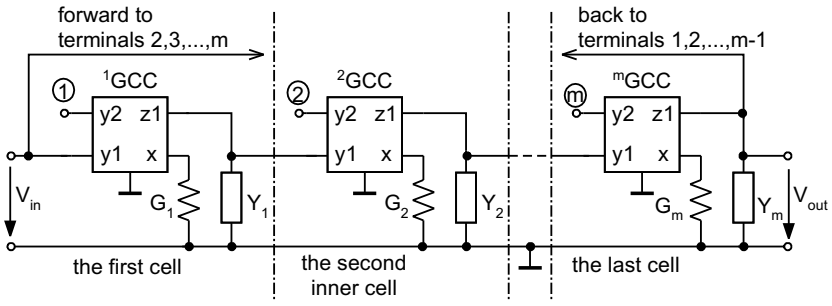

Fig. 3. A cascade connection of m building cells

This simple cascade connection forms the *main signal path* of the resulting two-port network (see Fig. 3 with grounded terminals y_2).

If, for example, $m = 3$, then we get

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{a_{11}d_{11}a_{12}d_{12}a_{13}d_{13}G_1G_2G_3}{Y_1Y_2Y_3}\,. \tag{4}$$

The numerator in (3)
$a_{11}d_{11}a_{12}d_{12}\cdots a_{1m}d_{1m}G_1G_2\cdots G_{m-1}G_m$
can be expanded using the forward connections from the input terminal to feedback terminals $2, 3, \ldots, m$ as shown in Fig. 3. Then we compute the following additional numerator terms:

$$\begin{aligned}
&+ a_{22}d_{12}a_{13}d_{13}\cdots a_{1m}d_{1m}Y_1G_2G_3\cdots G_m\\
&+ a_{23}d_{13}a_{14}d_{14}\cdots a_{1m}d_{1m}Y_1Y_2G_3G_4\cdots G_m\\
&+ a_{24}d_{14}a_{15}d_{15}\cdots a_{1m}d_{1m}Y_1Y_2Y_3G_4G_5\cdots G_m\\
&+\cdots + a_{2m}d_{1m}Y_1Y_2\cdots Y_mG_m\,.
\end{aligned} \tag{5}$$

Let us assume for the *main signal path* in (3) that:

$$\begin{aligned}
&a_{1k}d_{1k} = +1 \quad \text{for } k = 1, 2, 3, \ldots, m\\
\text{and}\qquad &a_{1k} = (-1)^{k+1}.
\end{aligned} \tag{6}$$

To obtain relation (1) the following conditions for the *numerator signal path* must be fulfilled:

$$a_{2i}d_{1i} = (-1)^{i+1} \qquad (i = 2, 3, \ldots, m)\,. \tag{7}$$

In a similar way (using the feedback connections from the output terminal to feedback terminals $1, 2, \ldots, m-1$ as shown in Fig. 3) we can expand the denominator in

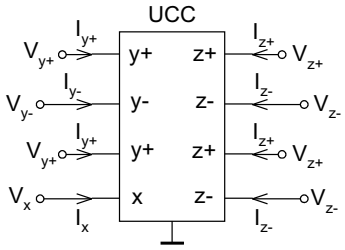

Fig. 4. Schematic symbol of a universal current conveyor

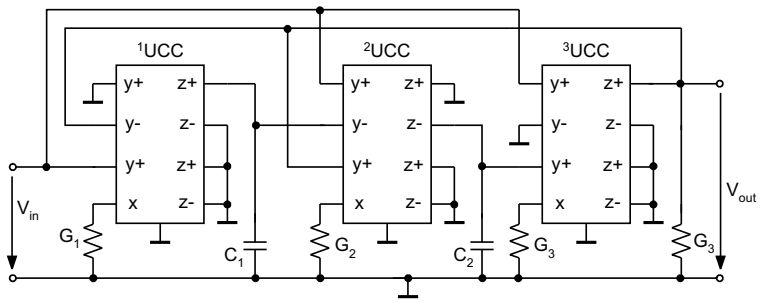

Fig. 5. A second-order allpass filter operating in the voltage mode

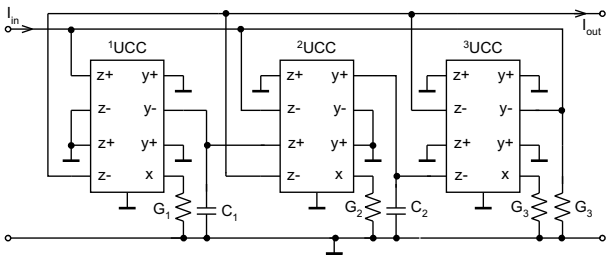

Fig. 6. A second-order allpass filter operating in the current mode

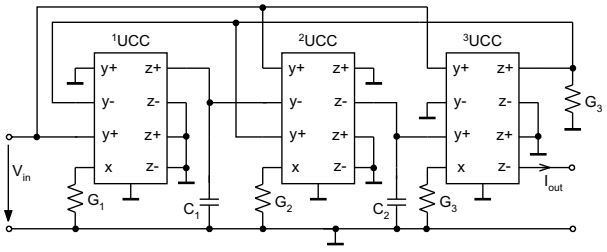

Fig. 7. A second-order allpass filter operating in the transadmittance mode

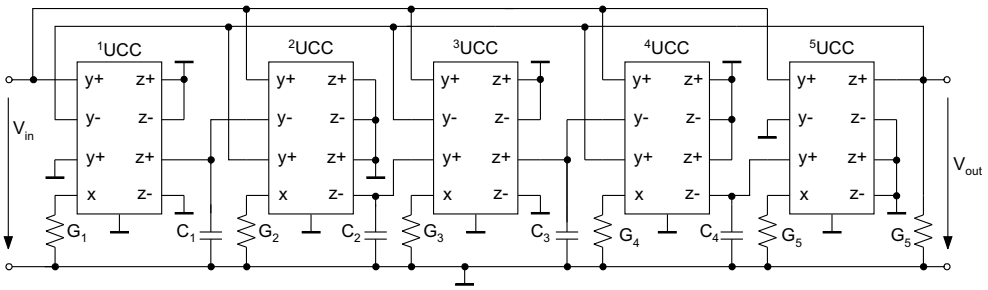

Fig. 8. A fourth-order allpass filter operating in the voltage mode

(3). Thus we obtain:

$$\begin{aligned}
&- a_{21}d_{11}a_{12}d_{12}a_{13}d_{13}\cdots a_{1m}d_{1m}G_1G_2\cdots G_m\\
&- a_{22}d_{12}a_{13}d_{13}a_{14}d_{14}\cdots a_{1m}d_{1m}Y_1G_2G_3\cdots G_m\\
&- a_{23}d_{13}a_{14}d_{14}a_{15}d_{15}\cdots a_{1m}d_{1m}Y_1Y_2G_3G_4\cdots G_m\\
&- \cdots - a_{2(m-1)}d_{1(m-1)}Y_1Y_2Y_3\cdots Y_{m-1}G_m\\
&+ Y_1Y_2Y_3\cdots Y_m\,.
\end{aligned} \tag{8}$$

According to (8) it is necessary to satisfy the following conditions for the *denominator signal path*:

$$a_{2i}d_{1i} = -1 \qquad (i = 1, 2, \ldots, m-1)\,. \tag{9}$$

3 FILTER REALIZATION

As an example, let us consider that $m = 3$. In this case we can choose: $Y_1 = sC_1$, $Y_2 = sC_2$, $Y_3 = G_3$. From (6) we obtain the following coefficients for the main signal path: $a_{11} = +1$, $d_{11} = +1$, $a_{12} = -1$, $d_{12} = -1$, $a_{13} = +1$, $d_{13} = +1$. According to relation (7) we must use for the numerator signal path the following coefficients: $a_{22} = +1$, $a_{23} = +1$. Finally, for the denominator signal path we have acc. to (9): $a_{21} = -1$, $a_{22} = +1$.

The *universal current conveyor* (UCC) [4], the schematic symbol of which is drawn in Fig. 4, enables the realization of all the above conveyance coefficients. The UCC element is described by the following equation set:

$$\begin{aligned}
V_x &= +V_{y+} - V_{y-} + V_{y+}\,, \quad I_x = I^*,\\
I_{y+} &= I_{y-} = 0\,, \quad I_{z+} = +I^*, \quad I_{z-} = -I^*.
\end{aligned}$$

The circuit diagram of the just proposed second-order allpass filter ($n = m - 1$) is shown in Fig. 5. The voltage transfer function $H(s) = V_{\text{out}}/V_{\text{in}}$ has the canonical form:

$$H(s) = \frac{G_1G_2 - sC_1G_2 + s^2C_1C_2}{G_1G_2 + sC_1G_2 + s^2C_1C_2}\,. \tag{10}$$

The same network can operate in the current mode if the input and the output port are interchanged and if we mutually interterchange these terminal pairs: $y+ \Leftrightarrow z-$ and $y- \Leftrightarrow z+$ [5]. A second-order allpass filter operating in the current mode is shown in Fig. 6. Its current transfer function $H(s) = I_{\text{out}}/I_{\text{in}}$ is also given by eqn. (10).

Considering the output current as shown in Fig. 7, we get a two-port network that operates in the transadmittance mode $\left(I_{\text{out}}/V_{\text{in}} = -G_3H(s)\right)$.

Let there be $n = 4$, which means that $m = 5$. Choosing in (5) to (9): $Y_1 = sC_1$, $Y_2 = sC_2$, $Y_3 = sC_3$, $Y_4 = sC_4$, $Y_5 = G_5$, we can state for the main signal path acc. to (6): $a_{11} = d_{11} = +1$, $a_{12} = d_{12} = -1$, $a_{13} = d_{13} = +1$, $a_{14} = d_{14} = -1$, $a_{15} = d_{15} = +1$, for the numerator signal path acc. to (7): $a_{22} = a_{23} = a_{24} = a_{25} = +1$, for the denominator signal path acc. to (9): $a_{21} = -1$, $a_{22} = +1$, $a_{23} = -1$, $a_{24} = +1$.

The realization network is shown in Fig. 8. The polynomial coefficients in (1) in the case considered are: $\alpha_0 = G_1G_2G_3G_4$, $\alpha_1 = C_1G_2G_3G_4$, $\alpha_2 = C_1C_2G_3G_4$, $\alpha_3 = C_1C_2C_3G_4$, $\alpha_4 = C_1C_2C_3C_4$, or $\alpha_0 = 1$, $\alpha_1 = R_1C_1$, $\alpha_2 = R_1C_1R_2C_2$, $\alpha_3 = R_1C_1R_2C_2R_3C_3$, $\alpha_4 = R_1C_1R_2C_2R_3C_3R_4C_4$. The filter operates in the voltage mode. The network can be easily transformed to operate in the current or in the transadmittance mode. The order of the filter can be expanded arbitrarily.

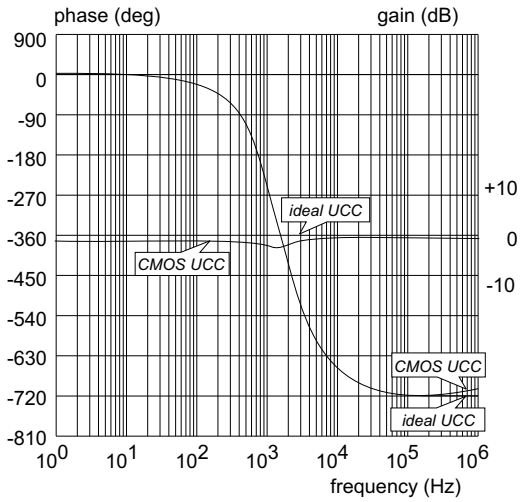

Fig. 9. Phase- and gain-frequency characteristics of the fourth-order allpass filter in Fig. 8

4 SIMULATION RESULTS

The allpas filter according to Fig. 8 was verified by means of a SPICE simulator. The filter was proposed with the following element parameters: $R_1 = 34\,\mathrm{k\Omega}$, $R_2 = 14.4\,\mathrm{k\Omega}$, $R_3 = 7.5\,\mathrm{k\Omega}$, $R_4 = 3.3\,\mathrm{k\Omega}$, $R_5 = 10\,\mathrm{k\Omega}$, $C_1 = C_2 = C_3 = C_4 = 10$ nF, and the CMOS universal current conveyor described in [6] was used. Figure 9 shows the phase- and gain-frequency characteristic of the allpass filter, giving a comparison of the filter with ideal UCCs and with simulated UCCs [6].

5 CONCLUSION

We have derived a new simple algorithm for nth-order allpass filter design. The proposed network contains only $(n+1)$ universal current conveyors (UCCs), $(n+1)$ grounded resistors and n grounded capacitors. All passive elements are grounded. In principle, the same structure (a cascade of building cells with special feedback connections) can be used for the design of filters operating in three different modes.

There are three signal paths in the designed network. The main signal path goes alternately through the $(y+, z+)$ and $(y-, z-)$ terminals of the UCC elements. The numerator signal path connects the input-port terminal with the $y+$ terminals of the following UCC elements. The denominator signal path connects the output-port terminal alternately with the $y-$ or $y+$ terminals of the preceeding UCC elements (beginning with the first one). The filter transfer function contains a minimum number of terms (it is canonical).

Acknowledgment

This paper has been supported by the Grant Agency of the Czech Republic, grants No. 102/00/1037 and 102/01/0432.

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Received 17 April 2001

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