APPLICATION OF ELECTROPLATING FOR DEVICE PROCESSING

Jaroslava Škriniarová* — Ján Jakabovič* — Ivan Kostič**

This paper presents the development in the technology of air-bridge formation for optoelectronic devices. We have introduced a double patternable planarizing lithography process for resists AZ 4560 and AZ 5214E that adds three dimensionality into the standard optical lithography. This technology offers low parasitic interconnect capacitances and inductances in devices. This method allows to define air bridges with different vertical width from $2\,\mu\mathrm{m}$ up to $12\,\mu\mathrm{m}$.

Keywords: electroplating, bridge interconnects

1 INTRODUCTION

Recently, the III—V industry has increased the demand for optoelectronic devices [1]. This has driven the III—V industry to look for various metallization processes such as evaporating, sputtering, etc. However, in many cases thin films do not provide satisfactory properties as for their mechanical characteristics (self-support ability, stiffness, strength) or electrical features (resistivity).

In some applications, thicker metallization layers are required. They can be created by classical technologies, nevertheless, there are rather expensive, time consuming and economically ineffective because of heavy material losses. In these situations, galvanic deposition can be used with advantage. Galvanic deposition of metallic lavers is particularly suitable for creating the so-called bump layer used to eliminate or reduce the effect of mechanical stresses arising in contacting the compound semiconductors A³B⁵ or in the technology of an air bridge which serves to cross two levels of electrically insulated metallizations. The inter-connections offer low parasitic interconnect capacitances and inductances. Furthermore, this eliminates uncertainty that may be caused by the small non-planarity of the surface at the chip wafer interface, which could lead to cracks or total breakage of the connection.

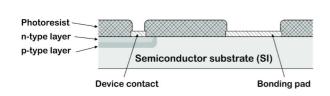


Fig. 1. Metal pads opening

In this paper we present a method for fabrication of non-supported air-bridges on an indium phosphide substrate. Our method for double patterning planarizing lithography with resists AZ 4560 and AZ5214E relies on utilizing optically sensitive resists. The process includes an air bridged metal cross from active devices to the contact pads.

2 EXPERIMENTAL

Air bridges are usually fabricated by evaporation and plating. There are many possible variations [2–4]. One of them is to deposit a thick photoresist on the sample and to pattern it. A thick metal layer (up to $2\,\mu\mathrm{m}$) is then sputtered on the patterned resist. Finally, the rest of the metal is etched and the resist is stripped, leaving a stable air-bridge.

These applications use gold thicknesses much greater than typically applied by evaporation. One of the disadvantages is the consumption of enormous amounts of gold, most of which would be deposited on places other than the sample. Even ignoring economic aspects, such a thick film is very difficult to pattern using lift-off or etching processes. Gold plating is the only economical means to provide such thick coatings. The major steps typical

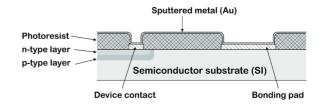


Fig. 2. Preplate metal

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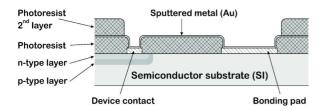


Fig. 3. Plate pattern

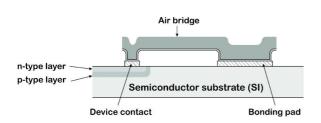


Fig. 5. Final air-bridge

for most processes are illustrated in Figs. 1–5. A layer of resist AZ 4560 is spun onto the sample and patterned to open an area over the metal pads. This step defines the areas, where the plating contacts the underlying metal (Fig. 1), with the desired thickness of the bridge.

After the preplate pattern is formed, a thin coating (150 nm) of metal is evaporated on the entire slice (Fig. 2). The "preplate metal" serves to carry the electroplating current. The 150 nm Au film was deposited using a standard evaporation system to create a continuous conductive layer. The base pressure in the chambers was better than 1.5×10^{-4} Pa (Fig. 2) and the typical working pressure for evaporation was 0.5 Pa.

Next, a second coating of photoresist AZ 5214E (the so-called plate pattern) is applied and patterned (Fig. 3).

Then the sample is plated, a thin metal layer is used to conduct the plating current to all parts of the sample. Plating is used to deposit a thick layer of gold to construct air bridges. In the second photoresist layer openings, gold is plated only (Fig. 4).

Ultra-pure soft gold is required that can be soldered easily and die bonded. Also the baths used to deposit this gold must be extremely pure. Composition of the bath and conditions we have used are described below.

 $\begin{array}{lll} {\rm KAu(CN)_2} & 15~{\rm g/liter} \\ {\rm Temperature} & 50~{\rm ^{\circ}C} \\ {\rm KOH} & 30~{\rm g/liter} \\ {\rm pH} & 6.5 \\ {\rm H_3PO_4(85\%)} & 44~{\rm g/liter} \\ {\rm Tl_2SO_4} & 20~{\rm mg/liter} \\ \end{array}$

The plating rate in the bath depends on agitation, temperature, gold concentration and on the concentration of potassium hydroxide. The bath plates at a rate

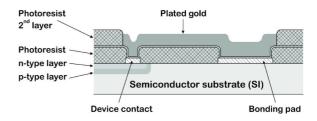


Fig. 4. Electroplating of gold

of $0.2\,\mu\mathrm{m}$ per min at 50 °C with mild agitation. However, vigorous agitation is needed to obtain satisfactory deposits.

The top resist, thin metal, and lower resist are removed after the plating operation, leaving the plated bridge (Fig. 5). This method is a low temperature process and uses the photoresist as a sacrificial material. The maximum processing temperature is about $120\,^{\circ}\mathrm{C}$.

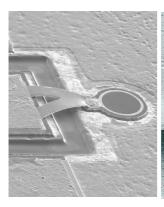
3 RESULTS AND DISCUSSION

Although the basic concept of the process is very simple, there are a number of process variations and problems. All resist layers must be sufficiently resistant to withstand the plating environment. However, the lower resist layer must not be over-baked or else it would be difficult or impossible to remove the resist from the bridge plated beneath. The thin layer of the metal that extends across the whole sample is applied by evaporation. If the metal layer is thin enough (about 100 nm), it can be broken from the plated areas by solvent actions. That is, lift-off procedures can remove both levels of resist and the intermediate layer in a single operation. If the metal layer is thicker, each of the three levels can be removed individually.

The thickness of the first layer of the resist determines the spacing between the bridge and the material beneath. Hence, this layer of resist was $6-8\,\mu\mathrm{m}$. Processing of the resist also affects the profile produced in the plating. The wet developing of the resist gives arched shapes to the air bridge (Fig. 6).

4 CONCLUSION

Air bridges are unsupported interconnects used to connect various elements on the substrate where wire bonding is difficult and inconsistent. Unlike wire bonding, air bridges are virtually identical, often resulting in reduced tuning times. There is an air gap of about 6 micrometers between the air bridge and the underlying surface of the sample. Air has the smallest permittivity, and the space under the air bridge tends to be greater than the thickness of typical dielectrics. It offers increased performance, but suffers from the weakness of being fragile and subject to damage. An unsupported air bridge requires 2 added



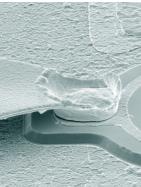


Fig. 6. Scanning electron micrograph of a plated bridged structure using the photoresist process. The length is $50\,\mu\mathrm{m}$ and the width is $12\,\mu\mathrm{m}$.

masking steps as well as associated photolithography and etching.

Acknowledgements

This work was supported by the Ministry of Education of the Slovak Republic (Grant No. 1/0152/03) and NATO SfP–9724172.

References

- HAŠKO, D.—UHEREK, F.: ECS'01. Bratislava, 5.-7. 9. 2001, 153 - 155.
- [2] BOUCINHA, M.—CHU, V.—ALPIUM, J., P.—CONDE, J. P.: Sensors and Actuators **74** (1999), 5–8.
- [3] WATANABE, Y. et al: Fujitsu Sci. Tech. J. 34 (1998), 154–161.

[4] VASILACHE, D. et al: Memmswawe Workshop, Sinaia, Romania 1999.

Received 5 September 2003

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