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COMMUNICATIONS

GAIN– AND OFFSET– COMPENSATED VERY LARGE TIME CONSTANT SC INTEGRATOR

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A novel gain- and offset- compensated (GOC) very large time constant (VLT) switched-capacitor (SC) integrator is presented. The gain, phase, and offset errors of the integrator are simultaneously lower when compared to previously proposed VLT integrators. The superiority of the new integrator is demonstrated by designing a 60 Hz notch filter.

K e y w o r d s: gain- and offset- compensation, very large time constant SC integrator.

1 INTRODUCTION

Several difficulties arise in designing very large time constant (VLT) switched-capacitor (SC) circuits in which the pole (zero)/sampling frequency ratios are very small. The time constant of the conventional SC integrators is approximately given by $\tau = C_2/(C_1 f_S)$, where C_1 is the input sampling capacitance, C_2 is the integrating (feedback) capacitance, and f_S is the sampling frequency. In order to get a very large time constant, a very large C_2/C_1 ratio is needed. Hence, the capacitor spread becomes too large to be practical for monolithic implementation. Several approaches have been investigated for making VLT SC integrators in an area-efficient manner. Published before 1989 and novel conventional and VLT integrators are compared in [1] using the $\alpha\beta\gamma$ criteria. The time constants of the VLT integrators, described in [1] , are determined by the product of two capacitor ratios. This enables us to obtain very large time constants with reasonable capacitor ratios. Virtually all area-efficient implementations for VLT integrators suffer from higher sensitivity to a finite gain A and offset voltage V_{os} of the operational amplifiers. For example, if the Nagaraj-88 VLT integrator [2] reduces the capacitance spread by a factor of k, the amplifier dc gain must be increased by the same factor to maintain the same accuracy as that of the conventional basic-79 integrator [3]. The output offset voltage is also k times larger.

With the implementation of the gain- and offset- compensation (GOC) technique, the effect due to A and V_{os}, can be reduced [4, 5, 6, 7]. Most of the GOS VLT integrators are obtained by modifying the corresponding uncompensated VLT structures. Thus, the Ki#3-89 GOC VLT integrator [1] is a modification of the Nagaraj-88 uncompensated VLT integrator. The phase errors of the published GOC VLT integrators are considerably smaller than those of the uncompensated circuits. However, their gain errors are comparable to the gain errors of the uncompensated integrators except for a weaker frequency dependence.

This paper presents a novel GOC VLT SC integrator which has simultaneously a lower gain, phase and offset errors when compared to previously proposed VLT integrators.

2 CIRCUIT ARCHITECTURE

The circuit schema of the Nagaraj-88 VLT integrator [2] is shown in Fig. 1. The clock phases inside brackets apply to the noninverting integrator, whereas those outside brackets apply to the inverting integrator. The nonzero input-referred dc offset voltage V_{os} of the operational amplifier (OA) is modeled as a voltage source at the noninverting input terminal. In the ideal case, the integrator's z-domain transfer function is given by

$$H_{id}(z) = \mp \frac{\frac{C_1}{C_2}\frac{C_3}{C_2} z^{-1/2}}{\left(1+\frac{C_3}{C_2}\right)\left(1-z^{-1}\right)}. \qquad (1)$$

In order to ensure optimal matching accuracy, the number of different capacitor sizes should be reduced to a minimum. It is reasonable to assign $C_1 = C_3 = 1$ unit and $C_2 = 1/k$ units, where $k < 1$. Then (1) can be expressed as

$$H_{id}(z) = \mp \frac{k^2 z^{-1/2}}{(1+k)(1-z^{-1})}. \qquad (2)$$

By adding an auxiliary (holding) capacitor C_h and a few switches, the Ki#3-89 GOC VLT is obtained (Fig. 2), where $C_h = 1$.

The proposed GOC VLT integrator (shown in Fig. 3a) is with the same sample correction property as in [8, 9]. Compared with the Nagaraj-88 integrator (Fig. 1), the OA has been replaced with the block shown in Fig. 3a. In addition to the clock phases 1 and 2, the integrator requires two nonoverlapping clocks, e and o , shown in

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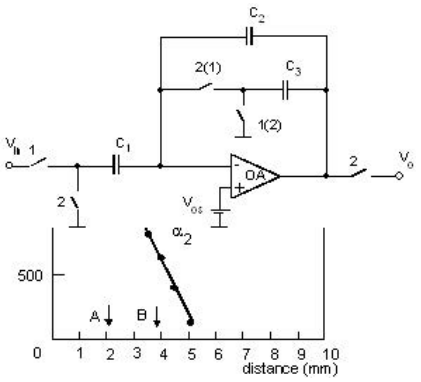

Fig 1 Nagaraj-88 VLT integrator

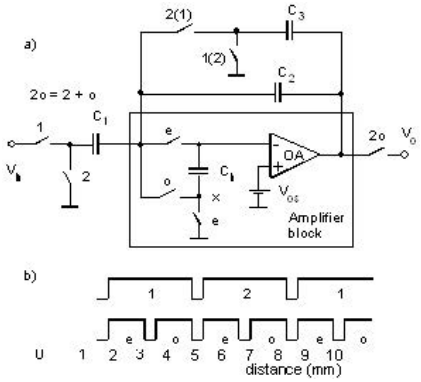

Fig 2 Ki #3-89 GOC VLT integrator

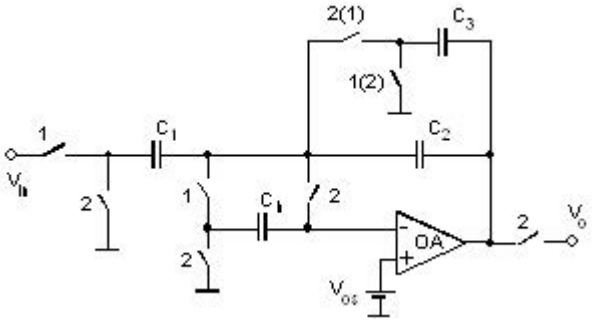

Fig 3 Proposed GOC VLT integrator and clocking scheme, a) GOC VLT integrator, b) Clocking scheme

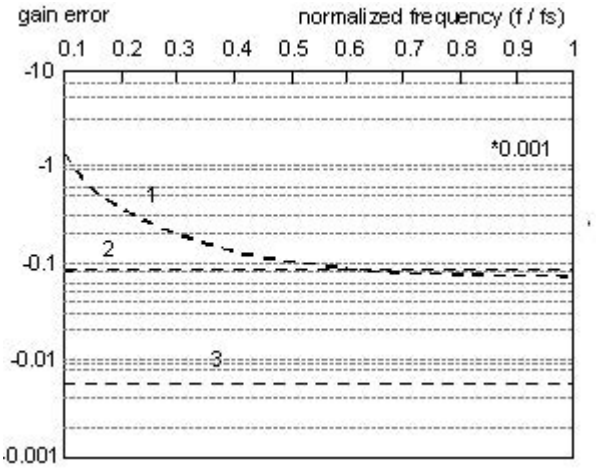

Fig 4 Gain error curves of VLT SC integrators for $k = 1/25$ and $A = 500$, 1 — Nagaraj-88 VLT integrator, 2 — Ki#3-89 GOC VLT integrator, 3 — Proposed GOC VLT integrator

Fig. 3b. The value of the holding capacitor C_h is not critical and can be made very small. The only factor governing its choice is that it forms a potential divider along with the parasitic capacitance at the input of the OA during the o phase. In most applications it will be adequate to set C_h equal to the unit capacitance (smallest filter capacitance). The output voltage V_o is sampled in phase $2o$. Then the ideal z-domain transfer function is given by

$$H_{id}^{2o}(z) = \mp\frac{k^2 z^{-3/4}}{(1+k)(1-z^{-1})}. \qquad (3)$$

In the following the bandwidth of the OA is assumed to be sufficiently large to guarantee in any case a settling time smaller than the sampling period. Then, a linear frequency-independent approximation for the voltage gain of the amplifier can be used

$$A(j\omega) = -A\,. \qquad (4)$$

This assumption is adequate for the analysis of SC circuits containing fast and relatively low-gain amplifiers.

During phase $2o$, C_h is placed in series with the inverting node of the OA, thus forcing node x to be a "super-virtual ground", the potential of which is given by

$$V_x^{2o}(n) = -\mu\left[V_o^{2o}(n) - V_o^{2e}\left(n-\tfrac{1}{4}\right)\right] \quad \mu = \frac{1}{A}. \qquad (5)$$

It is obvious that the "super-virtual ground" will not be affected by the offset but by the difference between two successive output voltages in the same output phase 2.

The transfer function of a nonideal integrator can be expressed in the continuous-time domain as

$$H(j\omega) = H_{id}(j\omega)[1+m(\omega)]\exp[j\theta(\omega)]\,. \qquad (6)$$

Here $m(\omega)$ is the gain error and $\theta(\omega)$ is the phase error due to the finite amplifier gain.

Table 1 compares the proposed inverting VLT integrator (Fig. 3) with the earlier ones Nagaraj-88 and Ki#-89 in terms of gain and phase errors. The gain errors are illustrated in Fig. 4 for $A = 1/\mu = 500$ and $k = 1/25$ ($C_1 = C_3 = C_h = 1$, $C_2 = 25$) [3].

Moreover, the compensation of the amplifier dc offset can be manifested in the suppression factor γ [1] of the offset voltage V_{os} as listed in Table 2. The expressions for the dc gains $H(0)$ of the integrators are also given.

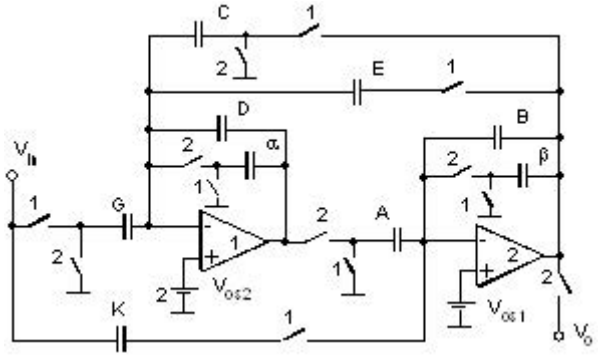

Fig 5 Circuit schema of a notch filter with the Nagaraj-88 integrators

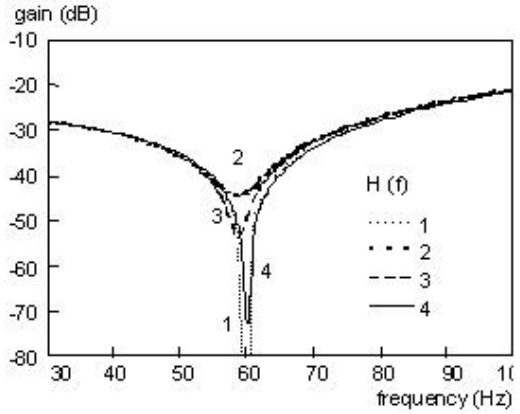

Fig 6 Simulated magnitude responses of 60-Hz notch filter 1 — ideal response ($A \to \infty$), 2 — with the Nagaraj-88 integrators ($A = 100$), 3 — with the Ki#3-89 integrators ($A = 100$), 4 — with the proposed integrators in Fig. 3 ($A = 100$)

Table 1. Error formulas for SC integrators with finite opamp gain $A = 1/\mu$ for $C_1 = C_3 = C_h = 1,\ C_2 = 1/k$

Integrator	Gain error $m(\omega)$	Phase error $\Theta(\omega)$
Nagaraj-88	$-\mu\left(2+k+\frac{0.5k}{1+k}\right)-$ $-\frac{\mu^2k^2[1-(1+k)\mu]}{8(1+k)^2\,\mathrm{tg}^2(\omega T_S)}$	$\frac{\mu k}{2(1+k)\,\mathrm{tg}(0.5\omega T_S)}$
Ki#3-89	$-\mu\left(2+1.5k+\frac{1.5k}{1+k}\right)$	$-\frac{\mu k^2[1-(1+1/k)\mu}{2(1+k)\,\mathrm{tg}(0.5\omega T_S)}$
Proposed in Fig. 3	$-\frac{\mu k(2+3k)}{(1+k)^2}-\frac{\mu^2 2(1+7k)}{(1+k)^2}$	$\frac{\mu^2 k}{2\,\mathrm{tg}(0.5\omega T_S)}$

Table 2. Comparison of VLT integrators

Integrator	Offset voltage error γ	DC gain $H(O)$
Nagaraj-88	$\frac{k[1-\mu(1+k)]}{1+k}$	$\frac{k}{\mu[1+(1+k)\mu]}$
Ki#3-89	$-\frac{k^2[1-\mu(3+3k+1/k]}{1+k}$	$\frac{1}{\mu[1-(1+1/k)\mu]}$
Proposed in Fig. 3	$k\mu$	$\frac{k}{\mu^2(1+k)}$

Table 3. Performance parameters of the three filter structures

Notch filter with integrators:	f_Z, Hz	δf_Z, %	attenuation [dB] at f_z ; 60 Hz	
Nagaraj-88	58.86	-1.9	-42.10	-41.40
Ki#3-89	58.94	-1.77	-51.96	-47.91
Proposed in Fig. 3	59.95	-0.083	-74.86	-72.42

The factors by which the phase errors and the offset voltage errors for the proposed integrator are reduced, when compared with the Nagaraj-88 and the Ki#3-89 integrators, are approximately given by $1/[(1+k)\mu]$ and $k/[(1+k)\mu]$ respectively.

The following relations are valid

$$\begin{aligned} \frac{\theta_N(\omega)}{\theta_P(\omega)} &\approx \frac{\gamma_N}{\gamma_P} \approx \frac{H_P(0)}{H_N(0)} \\ \frac{|\theta_K(\omega)|}{\theta_P(\omega)} &\approx \frac{|\gamma_K|}{\gamma_P} \approx \frac{H_P(0)}{H_K(0)} \end{aligned} . \tag{7}$$

The index N refers to the Nagaraj-88 integrator, K — to the Ki#3-89 integrator, and P — to the proposed integrator.

3 60 HZ NOTCH SC FILTER WITH DIFFERENT VLT INTEGRATORS

The circuit schema of a 60 Hz high-pass notch SC filter using the Nagaraj-88 integrators is shown in Fig. 5 [3]. The sampling frequency is $f_S = 128$ kHz. The relative capacitor values are $A = G = 1,\ B = 10,\ C = 11.58,\ D = 50,\ E = 43.6,\ K = 10.23568,\ \alpha = 1.43$ and $\beta = 1.9$. Both of the integrators in the original structure (Fig. 5) have been consecutively replaced by the Ki#3-89 integrators and by the proposed in Fig. 3 integrators where $C_{h1} = C_{h2} = 1$ was chosen. Figure 6 shows the simulated magnitude responses of the notch filter designed with the three VLT integrators for $A_1 = A_2 = A = 1/\mu = 100$. The biquads based on the Nagaraj-88 and on the Ki#3-89 integrators exhibit nearly the same notch frequency shift because the integrators have comparable gain errors for $f/f_S > 0.0005$. The much lower notch frequency shift for the biquad with the new integrators is due to the smaller gain error. Table 3 summarizes the actual notch frequencies, the notch frequency shifts, and the attenuations at f_Z and 60 Hz.

The steady state output voltages of the notch filter designed with the Nagaraj-88, with the Ki#3-89, and with

the new integrators for $A = 100$ are correspondingly:

$$\lim_{n\to\infty} V_O(n) = 4.353 Vos_1 + 0.436\, Vos_2\,,$$
$$\lim_{n\to\infty} V_O(n) = -1.032 Vos_1 + 0.091\, Vos_2\,,$$
$$\lim_{n\to\infty} V_O(n) = 0.096 Vos_1 - 0.115\, Vos_2\,.$$

4 CONCLUSIONS

A new area-efficient gain- and offset-compensated very large time constant SC integrator has been presented and compared with previously proposed uncompensated and compensated integrators. It has been shown to have gain and phase errors and offset voltage error that are much smaller than those of the other very large time constant integrators.

The feasibility of the new integrator has been demonstrated by designing a 60-Hz notch filter. The resulting biquad has better performance than the same filter based on the Nagaraj-88 and Ki#3-89 VLT integrators.

References

[1] KI, W.-H.—TEMES, G. C.: Offset-Compensated Switched-Capacitor Integrators, Proc. ISCAS'90, 1990, pp. 2829–2832.

[2] NAGARAJ, K.: A Novel Parasitic-Insensitive Switched-Capacitor Technique for Realizing Very Large Time Constants, Proc. IEEE Custom Integrated Circuits Conference, 1988, pp. 12.4.1–12.4.4.

[3] NAGARAJ, K.: A Parasitic-Insensitive Area-Efficient Approach to Realizing Very Large Time Constants in Switched-Capacitor Circuits, IEEE Trans. Circuits Syst. **CAS 36,** (9) (1989), 1210–1216.

[4] LIN, J.—KI, W.-H.—THOMPSON, K.—SHAMMA, S.: Realization of Cochlear Filters by VLT Switched Capacitor Biquads, Proc. ICASSP'92, 1992, vol. 2, pp. 245–248.

[5] KI, W. H.—TEMES, G. C.: Area-Efficient Gain- and Offset-Compensated Very-Large-Time-Constant SC biquads, Proc. ISCAS'92, 1992, pp. 1187–1190.

[6] LIN, J.—KI, W. H.—EDWARDS, T.—SHAMMA, S.: Analog VLSI Implementations of Auditory Wavelet Transforms Using Switched Capacitor Circuit, IEEE Trans. Circuits Syst. **CAS-41,** (9) (1994), 572–583.

[7] ENZ, C. C.—TEMES, G. C.: Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization, Proc. IEEE **84,** (11) (1996), 1582–1614.

[8] SHAFEEU, H.—BETTS, A. K.—TAYLOR, J. T.: Novel Amplifier Gain Insensitive Switched-Capacitor Integrator with Same Sample Correction Properties, Electron. Lett. **27** (24) (1991), 2277–2279.

[9] SENG-PAN, U.—MARTINS, R. P.—FRANCA, J. E.: Highly Accurate Mismatch-Free SC Delay Circuits with Reduced Finite Gain and Offset Sensitivity, Proc. ISCAS,99, 1999, vol. 2, 57–60.

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