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TRENDS IN DEVELOPING NEW SEMICONDUCTOR POWER DEVICES BASED ON SiC AND DIAMOND MATERIALS

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In this article, silicon carbide and diamond are presented as materials of the future for semiconductor power device manufacturing. An overview of their properties and drawbacks is given for a comparison with the so far used silicon. Unipolar and bipolar devices based on silicon carbide as the most acceptable material for commercial manufacturing are analysed. Diamond is a promising material for application in high-power electronics and high temperature electronics. Characteristic values of devices are shown along with their best-achieved performances. An estimate of possible progress in the research and manufacturing of semiconductor power devices based on the new materials is given.

K e y w o r d s: SiC power devices, SiC unipolar power devices, SiC bipolar power devices, diamond power devices, diamond unipolar power devices, diamond bipolar power devices

1 INTRODUCTION

Silicon is presently the only semiconductor material used in making commercially available power devices. This is due to the fact that silicon can be grown in single crystal form with larger diameters and the greatest purity of any available semiconductor. There are, however, other materials that have superior properties compared to silicon for power device applications. Unfortunately, they are not available in sufficient purity or sizes to be considered for devices manufacturing.

Silicon carbide is a material of intense current interest for the fabrication of power devices. It has a significantly larger energy gap than silicon, thus rendering it useful at higher temperatures than silicon. In addition, the thermal conductivity of SiC is several times higher than that of silicon. The most significant advantage of SiC compared to silicon is the order-of-magnitude larger breakdown electric field strength of silicon carbide.

Diamond is the material with the greatest potential for power devices. It has the largest bandgap of any of the materials listed in Table 1, [1]. It also has the largest thermal conductivity and, most important of all, the largest breakdown electric field strength. Its carrier mobility is larger than that of silicon.

The state of diamond device technology is primitive compared to that of other materials including SiC. There are no methods of fabricating single crystal wafers of diamond. The methods of producing thin films of diamond that have been developed in the last few years produce polycrystalline films. Techniques for doing selective diffusion of impurities are poor and ohmic contacts to diamond require major research and development efforts. Selective etching methods for diamond are a major problem area.

2 SILICON CARBIDE POWER DEVICES

Technological processing and manufacturing of silicon carbide unipolar power devices and silicon carbide bipolar power devices have been considered.

P r o p e r t i e s o f S i l i c o n C a r b i d e

In order to withstand a certain voltage U_{BR}, the barrier layer of the semiconductor must have a specific thickness δ, which depends on how strong field E_{MAX} the base material can take without a breakdown. The smallest thickness of the layer is calculated from the equation

$$\delta_{MIN} > \frac{2U_{BR}}{E_{MAX}}\,, \tag{1}$$

Table 1. Properties of semiconductor materials with potential for power devices.

Property	Si	GaAs	4H-SiC	6H-SiC	Diamond
Bandgap at 300 K (eV)	1.12	1.43	2.2	2.9	5.5
Relative dielectric constant	11.8	12.8	9.7	10	5.5
Saturated drift velocity (cm/s)	1×10^7	2×10^7	2.5×10^7	2.5×10^7	2.5×10^7
Thermal conductivity (W/cm- °C)	1.5	0.5	5.0	5.0	20
Maximum operating temperature (K)	300	460	873	1240	1100
Melting temperature (°C)	1415	1238	Sublime$\gg$ 1800	Sublime$\gg$ 1800	Phase change
Electron mobility at 300 K (cm^2/V-s)	1400	8500	1000	600	2200
Breakdown electric field (V/cm)	3×10^5	4×10^5	4×10^6	4×10^6	1×10^7

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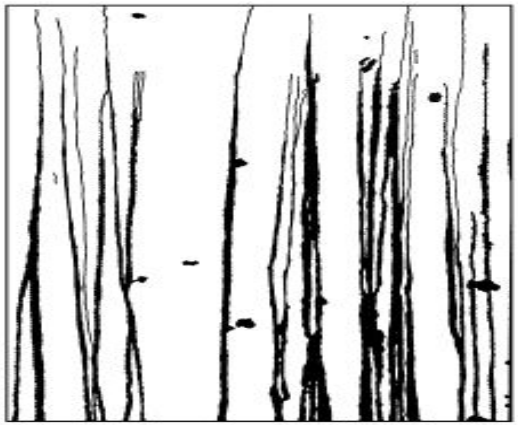

Fig. 1. Micro-pipes in a thick SiC substrate

keeping in mind that factor 2 can be omitted in certain circumstances, [3].

E_{MAX} is a variable depending on temperature, but in this place it can be considered as a constant value because a very small deviation is thus made. E_{MAX} for SiC is approximately ten times greater than for Si and this is the most significant advantage of SiC. It means that for a certain voltage the needed thickness of a SiC device will be just a tenth part of a Si device.

From Maxwell's equation, condition for the amount of impurities doped in the base material can be established:

$$\frac{\mathrm{d}E}{\mathrm{d}x} = \frac{\rho}{\varepsilon_0 \varepsilon_r} = \frac{qN_d^+}{\varepsilon_0 \varepsilon_r}\,, \tag{2}$$

where ρ is the charge density, ε_0 is the permittivity of vacuum, ε_r is the relative permittivity of material, q is the elementary electric charge, N_d^+ is the concentration of ionised donors. Along with that, it is presumed that voltage is set on the low-doped N-layer, which is the case with the most semiconductor power devices whether they are devices based on Si or SiC.

If we assume that the concentration of dopants is constant, applying eq. (1) and eq. (2) we get

$$N_d^+ < \frac{\varepsilon_0 \varepsilon_r E_{MAX}^2}{2qU_{BR}}\,. \tag{3}$$

Equation (3) shows that for each given breakdown voltage and ten times greater field strength, the drift region in a doped SiC semiconductor is going to be about a hundred times smaller than the drift region of Si. SiC provides the realisation of MOSFETs or Schottky diodes with much higher reverse voltages than those in Si-based devices. Wide application of MOSFETs can be expected, even in places where system voltages reach several kilovolts, for instance in the reactive power compensation.

SiC devices can operate at significantly higher temperatures than Si ones. Leakage currents of the PN-junction are very small and they provide latching at much higher temperatures than in Si. Operating temperatures of over 200 °C can be very easily achieved and critical temperature can exceed even 600 °C.

Difficulties in Manufacturing SiC – based Power Devices

Manufacturing of semiconductor power devices includes etching, dielectric layer deposition, oxidation, metalising and leads implementing. Therefore, contrary to the Si-based manufacturing, the major part of the process is realised without ordering the substance from other manufacturers. Namely, doping as the most controlled procedure for adding impurities to the crystal structure at a high temperature is not favourable for SiC. Instead, the doping substance is added simultaneously with the epitaxial growth. For achieving a contact layer, ion implantation can be used as with Si.

Silicon carbide does not melt at normal pressure, but sublimes at approximately 2500 °C. It means that the crystal has to be obtained from the gaseous state, which is more complicated than getting silicon from drip state at a temperature of about 1400 °C.

One of the major obstacles for a breakthrough of silicon carbide is non-existence of a substrate that would have a quality high enough for industrial production. Namely, as for Si a monocrystal substrate (wafer) is needed before the beginning of the production. At the late seventies and early eighties, the so-called modified Lely method for manufacturing big SiC substrates was developed. However, a substrate made in this way has severe defects known as micro-pipes and shown in Fig. 1.

Such a micro-pipe with a diameter of 1μm, which passes through the PN-junction, makes holding reverse voltages at PN-junction impossible. Nevertheless, these defects were greatly reduced during the past three years for example, from 1000/cm^2 to about several hundred over cm^2. Even with such developments the chip size is limited to a few mm^2, and the number of correct devices amounts to a few percent. Also, the nominal current is limited to a few amperes for each device.

2.1 Silicon Carbide Unipolar Power Devices

SiC is unique among compound semiconductors in that its native oxide is SiO_2, the same oxide as of silicon. This means that the work-horse power devices used in silicon, *ie* the power MOSFET, insulated gate bipolar transistor (IGBT), and various types of MOS — controlled thyristors (MCTs) can all be fabricated in SiC. Because of the higher breakdown field, SiC power devices can have specific on-resistances up to 400 times lower than similar devices in silicon.

The operating temperature of unipolar devices is limited by the temperature above which the charge carriers density in the semiconductor can not be controlled by doping, but by changing the width of the gap between the energy bands. If this limit is exceeded, the ability of controlling the current or latching is lost. For Si this limit is at about 200 °C, and for SiC this temperature exceeds even 600 °C.

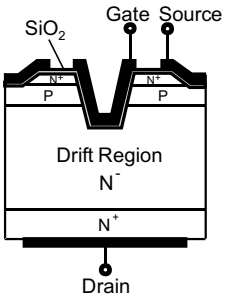

Fig. 2. Structure of a typical vertical N - channel SiC power MOSFET

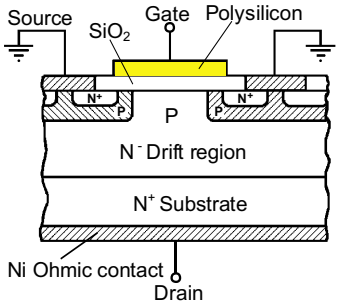

Fig. 3. Cross section of a Si ion-implanted "DMOS" power transistor

Table 2. Drift region doping levels and lengths required for a 1000 V step junction fabricated

Material	$N_d(\mathrm{cm}^{-3})$	$\delta_d(\mu\mathrm{m})$
Si	1.3×10^{14}	100
SiC	1.1×10^{14}	10
Diamond	1.5×10^{17}	2

The Si-based unipolar devices operating temperature must not exceed 150 °C because with the decrease of charge carriers mobility the on-state dissipation losses increase.

Silicon Carbide Vertical Diffused Power MOSFET

Figure 2 shows a cross-section of a typical SiC power VDMOSFET. MOSFETs designed so far have blocking voltages up to 1000 V. One of the reasons for it is shown in the equation

$$R_{DS(on)} = R_{DS} \cdot A = \frac{4U_{BR}^2}{\mu\varepsilon_0\varepsilon_r E_{MAX}^3}\,, \qquad (4)$$

where $R_{DS(on)}$ is the specific on-state resistance, A is the cross-sectional area of the drift region and μ is the electron mobility, [1], [3].

A convenient way to compare the potential benefits of using other materials is to use eq. (4) to compute the specific drift region resistance of devices having identical breakdown voltage ratings but which are made with other materials. If all devices were compared against silicon-based, a normalised specific resistance ratio would be

$$\frac{R_{on}(x)}{R_{on}(Si)} = \frac{\varepsilon_{Si}\mu_{Si}}{\varepsilon_x\mu_x}\left[\frac{E_{MAX(Si)}}{E_{MAX(x)}}\right]^3 \qquad (5)$$

where x stands for the material being compared with silicon. For Si the resistance ratio is 1, for SiC 9.6×10^{-3} and for diamond 3.7×10^{-5}. The values for the parameters in eq. (5) were taken from Table 1.

From eq. (4) it can be seen that the resistance is increasing with the increase of thickness of the drift region and decreasing with the increase of doping, when more charge carriers are involved in conducting of current. According to eq. (4) the resistance of the drift region of the MOSFET increases with the square of reverse voltage. In Si based MOSFETs that resistance reaches great values when U_{BR} increases to several hundred volts. At the critical field strength, the resistance is decreasing with the third power. Critical electric field strength of SiC being nearly ten times greater than the one of Si, on-state power dissipation of SiC based MOSFETs is incomparably smaller than that of Si-based devices, especially in voltage region under 100 V in which the on-state dissipation is dominant over the drift region dissipation. These losses depend on operating temperatures and current densities as in Si devices. This also counts for other unipolar devices like JFETs and Schottky diodes.

A final telling comparison is to estimate the carrier lifetime required in a PN-junction diode fabricated in each of the different materials. Such a comparison gives for Si 1.2 μs, SiC 40 ns and for diamond 7 ns. A breakdown voltage of 1000 V was used for the comparison. The much shorter carrier lifetimes required in the other semiconductors compared to silicon mean that minority carrier devices fabricated in these materials will be significantly faster than the silicon counterpart.

Another revealing way to compare the benefits of these other materials is to compute the drift region doping level and length required to support a specified value of breakdown voltage in a PN-junction diode. Such a numerical comparison is made in Table 2 for a simple step junction having a breakdown voltage of 1000 V, [1].

Larger doping densities and shorter drift region lengths that are required as we go from silicon toward diamond clearly indicate the superior properties of the other materials compared to silicon.

Silicon Carbide Double -- implanted MOS or DMOS Power Transistor

Silicon carbide double-implanted MOS or DMOS power transistor is shown in Fig. 3. This device is analogous to the silicon DMOS, or "double-diffused MOS", power transistor except that the P base and N^+ source regions are produced by ion implantation instead of thermal diffusion (diffusion is not practical in SiC because of the very low diffusion coefficients in the material), [4]. In this device, a forward bias on the polysilicon gate creates a surface inversion layer at the interface between the SiO_2 and the P-type SiC.

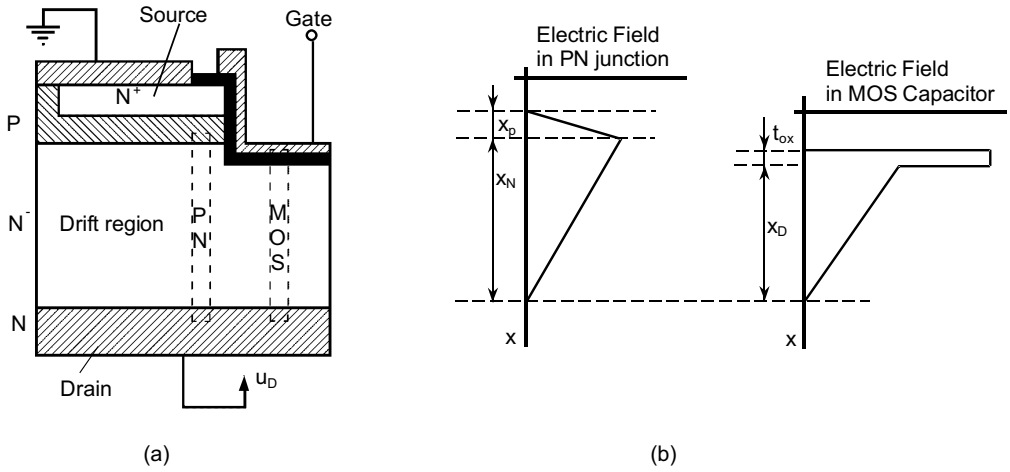

Fig. 4. Cross section of a UMOS power transistor in silicon carbide

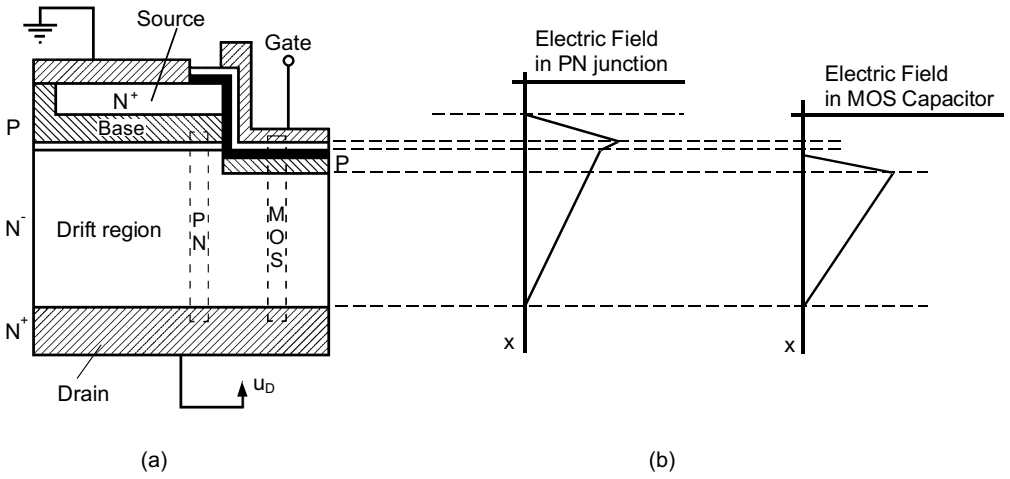

Fig. 5. Cross section of the Optimised UMOS power transistor

Electrons flow from the N^+ source along the inversion layer to the N^- drift region. Upon reaching the drift region, electrons flow vertically to the N^+ drain at the bottom. The thick, lightly doped N^- — drift region is needed to withstand a large drain voltage when the device is in the off state (gate at ground).

Silicon Carbide Trench – gate MOS or UMOS Power Transistor

Silicon Carbide Trench-gate MOS or UMOS power transistor is shown in Fig. 4.a, [5].

Electric fields are illustrated on the right side of Fig. 4.b for two regions within the device, the PN-junction region and the MOS capacitor region. The field in the oxide at the base of the trench is 2.5 times higher than the peak field in the semiconductor because of the discontinuity in dielectric constants at the interface. Such a high electric field can lead to catastrophic breakdown of the oxide. The field at the corner of the trench is even higher due to two-dimensional effects. This oxide breakdown problem represents a major limitation to the UMOSFET structure in SiC.

Silicon Carbide Optimised UMOS ACCUFET

"Optimised" UMOS structure or UMOS ACCUFET, [6] limits the electric field in the trench oxide while simultaneously reducing on-resistance. This structure is shown in Fig. 5, along with the electric fields in the blocking state.

The new P-type region in the bottom of the trench reduces the electric fields at the oxide/semiconductor interface to zero, thereby protecting the oxide from high electric fields in the blocking state. The new N-type epilayer beneath the P-base prevents pinch-off of the conducting channel in the on state and facilitates lateral current spreading into the drift region. The device in Fig. 5 also includes a lightly doped N-type epilayer grown on the side-walls of the trench. This layer converts the device into an accumulation-layer MOSFET, or "ACCUFET", increasing the MOSFET mobility and further reducing on-resistance.

Figure 6 shows the static I–V characteristics of an Optimised UMOS ACCUFET in 4H SiC, [6]. The blocking voltage is 1400 V, which is 87 % of the theoretical value for the 10μm drift region in the device. The break-

down is non-destructive, indicating that oxide failure does not occur.

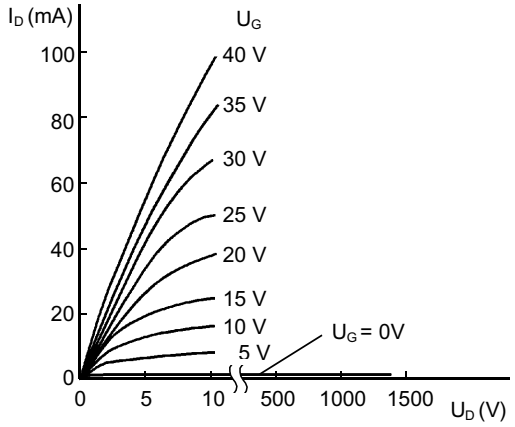

Fig. 6. $I-V$ characteristics of the optimised UMOS ACCUFET in 4H–SiC

The highest value for a power MOSFET in any material system are 25 times higher than the theoretical limit for silicon power MOSFETs.

Silicon Carbide Lateral Power MOSFETs

Until recently, power-switching devices in SiC, both MOSFETs and thyristors, were fabricated as vertical structures, with the substrate serving as the anode terminal. In the off state, a reverse-biased PN-unction blocks the voltage. To achieve a high blocking voltage, one side of this junction, the drift region, is thick (typically around 10μm) and lightly doped (5 - 10^{15}cm^{-3}). Until very recently, commercially available SiC epilayers were limited to about 10μm in thickness, and the maximum possible blocking voltage for this thickness was about 1600 V.

One way to avoid this limitation is to turn the device on its side, *ie*build a lateral device. The basic structure of lateral DMOSFET, [7] is shown in Fig. 7.

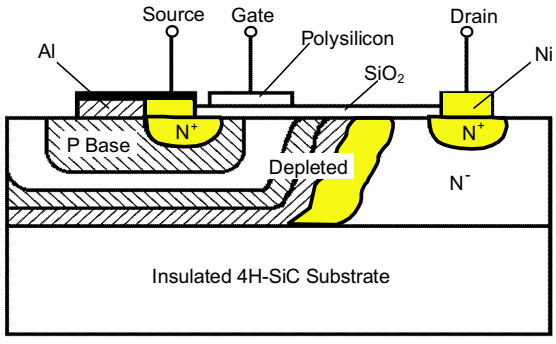

Fig. 7. Cross-section of lateral DMOSFET in the blocking state

In the blocking state, the depletion layer spreads mainly into the lightly doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain, which is now located on the top surface. In this device, the maximum blocking voltage is not limited by the thickness of the epilayer.

Figure 8 shows $I-V$ characteristics of a lateral DMOSFET having a 10μm gate length and a 35μm gate-to-drain spacing, [8].

The blocking voltage of this device is about 2.6 kV. This voltage is not limited by electrical breakdown in the device, but rather by arcing in the Fluorinert solution in which the device is immersed during testing.

It is important to realise that by implementing the device laterally rather than vertically, we do not necessarily increase the surface area required for the device.

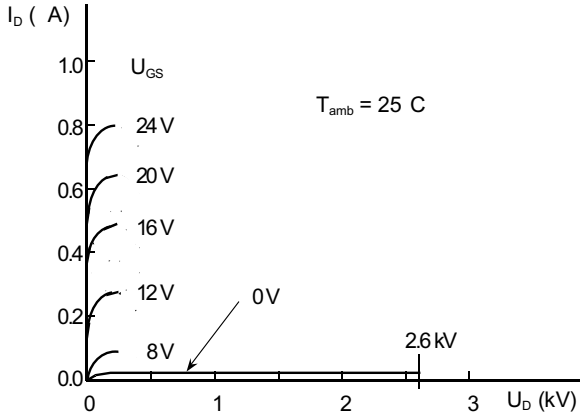

Fig. 8. I-V characteristics of a lateral DMOSFET

Silicon Carbide Schottky Barrier Diodes

Schottky barrier diodes (SBDs) are used as high-voltage rectifiers in many power-switching applications. Whenever current is switched to an inductive load such as an electric motor, high-voltage transients are induced on the lines. To suppress these transients, diodes are placed across each switching transistor to clamp the voltage excursions. PN-junction diodes could be used for this application, but they store minority carriers when forward biased, and extraction of these carriers allows a large transient reverse current during switching. SBDs are rectifying metal-semiconductor junctions, and their forward current consists of majority carriers injected from the semiconductor into the metal. Consequently, SBDs do not store minority carriers when forward biased, and the reverse current transient is negligible. This means the SBD can be turned off faster than a PN diode, and dissipates negligible power during switching.

SiC Schottky barrier diodes are especially attractive because the breakdown field of SiC is about 8 times higher than in silicon. In addition, because of the wide bandgap, SiC SBDs should be capable of much higher temperature operation than silicon devices.

The cross section of the SBD on 4H-SiC using both Ni and Ti as Schottky metals is shown in Fig. 9.

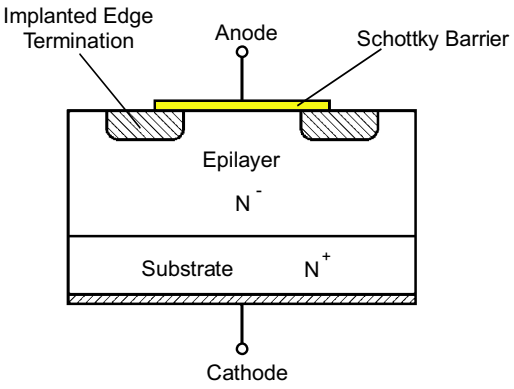

Fig. 9. Cross section of an implant-edge-terminated Schottky barrier in SiC

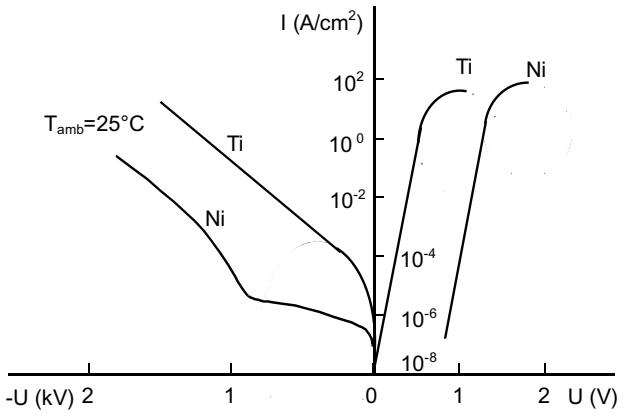

Fig. 10. Forward and reverse current — voltage characteristics for Ti and Ni Schottky barrier diodes on 4H-SiC

Special edge termination is required to minimise field crowding at the edge of the metal contact. This results in a resistive layer at the surface that spreads the field lines without causing a significant increase in junction leakage, [9].

Table 3. Performance figures-of-merit for the most recent SiC unipolar power devices

Device	Blocking Voltage (V)	Specific On-Resistance ($m\Omega/cm^2$)
SB Diode (4H)	1720	5.6
SB Diode (4H)	3000	34
DMOSFET (6H)	760	125
DMOSFET (4H)	900	–
UMOSFET (4H)	1400	433
UMOSFET (4H)	1410*	275
DMOS ACCUFET (6H)	350	18
UMOS ACCUFET (4H)	450	10.9
UMOS ACCUFET (4H)	1400	15.7
LATERAL DMOSFET (4H)	2600	–

Asterisk (*) denotes thick epilayer ($> 15\mu$m)

Forward and reverse I–V characteristics for the Ti and Ni SBDs are shown in Fig. 10.

The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 and 1.3 V, respectively. The lower barrier height gives Ti lower forward voltage drop but higher reverse leakage current as compared to the Ni barrier. The reverse blocking voltages are 1480 and 1720 V, respectively.

In Table 3 an overview of SiC-based unipolar devices with the best-achieved performances is given.

2.2. Silicon Carbide Bipolar Power Devices

Since SiC-based MOSFETs can not be used for voltage regions above 1000 V, for higher system voltages bipolar devices must be used.

According to eq. (3), it is evident that the number of charge carriers N_d limits resistance. In bipolar devices like PN diodes, IGBTs and GTOs the amount of charge carriers needed to increase device conductivity is realised with anode and cathode injection. Therefore, a drastic decrease of on-state dissipation in comparison to MOSFET follows. Nevertheless, a drawback of injecting charge carriers in bipolar devices is the need of extracting the charge from the device during latching before turning the device to off-state. This is achieved with a reverse current and a recombination of both electrons and holes. The time needed for extracting the excess charge carriers is can not be ignored and, besides that, during that process both the voltage and current can reach high values and therefore cause great circuit losses. It means that relatively small ON-state losses are "paid" with great circuit losses.

The total quantity of injected specific charge is

$$q_{IN} = \tau J\,, \tag{6}$$

where J is the current density, τ is the minority charge carriers lifetime or mean time of recombination of one electron-hole pair.

The minority charge carriers lifetime in power device depends on the concentration of structural imperfections or impurities that the manufacturer can control.

When high system voltages are needed, devices must be in the series connection. In this case reverse voltage of the devices is determined and both system operation and losses are optimised by it. Thyristors for such applications have typical values for reverse voltage of 6–7 kV, and they are the result of a compromise between prices, required high voltage and circuit losses. Such high reverse voltages require a Si-layer thickness of 1 mm and minority charge carriers lifetime of about 100 μs, which results in significant circuit losses. SiC based semiconducting materials provide devices with a higher reverse voltage, even notably higher than 10 kV. In these cases the minority charge carriers lifetime has to be between 1 and 10 μs, which makes a basis for good switching properties.

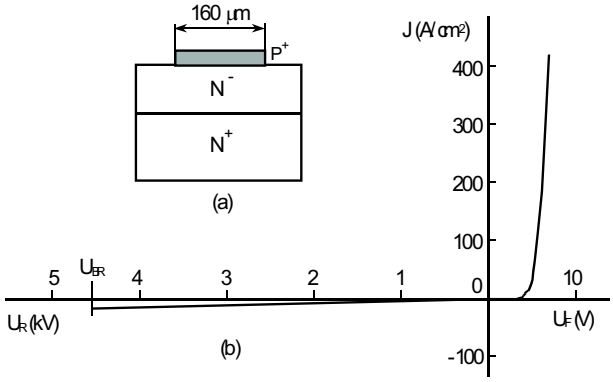

Fig. 11. Silicon carbide bipolar power diode: a) cross-section structure; b) I–V characteristics

Si-based bipolar devices must not exceed the temperature of 125 °C because their reverse current at the PN-junction increases with the increase of temperature thereby representing a risk of uncontrolled temperature rise, and, besides that, their charge carriers lifetime increases therefore increasing the risk of generating parasite destructive elements.

Table 4. Performance figures-of-merit for the most recent SiC bipolar power devices

Device	Blocking Voltage (V)	Specific On-Resistance ($\mathrm{m\Omega/cm^2}$)
PN Diode (6H)	4500*	—
PN Diode (4H)	5500*	5.4 V&100 $\mathrm{A/cm^2}$
Thyristor (4H)	700	0.82
Thyristor (4H)	900	1.7
GTO (4H)	1000	11.5 V&1600 $\mathrm{A/cm^2}$

Asterisk (*) denotes thick epilayer ($> 15\mu$m).

Table 5. Electronic properties of diamond

Property	Value
Bandgap	$E_G = 5.4$ eV
Thermal conductivity	$\lambda = 20$ W/(cm·k)
Break down field strength	$E_{BR} = 10^7$ V/cm
Relative dielectric permittivity	$\varepsilon_r = 5.5$
Electron saturation velocity	$v_S = 2.7 \times 10^7$ cm/s
Hole saturation velocity	$v_S = 1 \times 10^7$ cm/s
Electron mobility	$\mu_e = 2200\,\mathrm{cm^2/(Vs)}$
Hole mobility	$\mu_h = 1800\,\mathrm{cm^2/(Vs)}$

Silicon Carbide Bipolar Diode

According to available data from ABB company, [3], SiC bipolar power diode is realised and is shown in Fig. 11.a.

Until now, it was considered that minority charge carriers lifetime is limited to fewer than 100 ns values. 4.5 kV diode, Fig. 11.a, has a minority carriers lifetime of 0.5 μs. In some cases even higher values are achieved.

With the growth technique a layer with a thickness of 90μm and purity under $10^{14}/\mathrm{cm^3}$ of usual doping is realised. This is the best-achieved result so far. The epitaxial quality of the material contributed to this achievement. A diode with a reverse voltage of 4.5 kV is realised in this way. Figure 11.b shows the diode I–V characteristics.

In Table 4, an overview of SiC-based bipolar devices with their best performances is given.

3 DIAMOND POWER DEVICES

Diamond is a potential material for high-temperature, high-power and high-speed electronic applications. This expectation originates from the physical, chemical, and electronic properties as measured for undoped (type IIa — insulating, nominally undoped, clear, white) or lightly ($\sim 10^{16}\mathrm{cm^{-3}}$) boron doped (type IIb — conducting, boron-containing, deep blue) natural diamond samples (Table 5).

Due to the large bandgap, the intrinsic carrier concentration at 1000 °C is comparable to that of silicon at room temperature. Therefore, diamond devices operating at such high temperatures seem feasible. The material itself has been shown to withstand temperatures as high as 2000 °C, [10].

Using the data listed in Table 5, diamond exhibits the highest figures of merit in comparison with all other electronic materials except probably AlN. This is even true for P-channel FETs, which are realistic devices to date.

Unfortunately, there have been serious drawbacks which have prevented diamond from becoming a relevant electronic material up to now. Some properties such as the carrier mobility depend strongly on temperature and impurity concentration. In addition, up to now only boron doping has been possible, forming a deep acceptor with an activation energy of $E_A = 0.38$ eV. Donor doping by phosphorus with an activation energy of $E_A = 0.43$ eV has only recently been demonstrated, but not yet implemented in the form of devices, [11].

In spite of these problems, important technological breakthroughs have been made recently. The improved growth processes, doping techniques, and contact technologies reported here have already enabled Schottky diode operation at 1000 °C and allowed to predict an increase in the FET RF power performance to 30 W/mm for 0.1μm gate length.

Properties of CVD Diamond

The term "CVD diamond" refers to the Chemical Vapor Deposition (CVD) growth process used in low-pressure synthesis, in contrast to synthetic HPHT diamond, which is obtained at very High Pressure and High Temperature (HPHT) by transformation of graphite into

diamond. The present applications of low-pressure synthetic diamond exceed by for those of natural and HPHT synthetic diamond.

The synthesis of CVD diamond can by performed by a variety of methods using conventional laboratory equipment, while the synthesis of HPHT diamond requires special industrial equipment which is used by very few companies.

Of special interest are market niches, where CVD diamond offers "enabling technologies"; that is the manufacturing of new products such as electronic devices. Only low-pressure synthesis can provide diamond in the shape of wafers and films. The unique possibility of growing layered diamond structures using CVD technology is exploited for adhesion layers for δ-doping in electronic devices.

3.1 Diamond Unipolar Power Devices

Until now diamond unipolar power devices have been realized as diodes and transistors.

D i a m o n d M O S F E T

The diamond MOSFET has been developed in ion-implanted and epitaxial boron-doped channel material. Using low-doped channel material, high mobilities have been observed, but also freeze-out at room temperature. Hence, special doping profiles based on narrow-spike doping have been employed leading the improve of the thermal activation.

These transistor structures have been implanted into basic logic function and a voltage gain could be obtained in the quasi-static switching (100 kHz regime), [12]. The high-temperature operation of these MOSFET is attractive due to the increased carrier activation (around 500 °C), [13]. The best result were achieved at 325 °C ($I_{\max}$ = 30 mA/mm G = 1.3 mS/mm at 2μm gate length).

D i a m o n d M E S F E T

Technological problems arise when producing diamond MESFET as well as MOSFET. To reduce carrier freeze-out, high narrow doping profiles are needed. These steep profiles may be called delta (δ) doping. Such a structure has shown an improved activation, resulting in $I_{\max}$ = 0.4 mA/mm and $G_{\max}$ = 0.12 mS/mm at 300 °K, [14]. Poor output characteristics at room temperature are considerably improved at 350 °C. Comparison between those characteristics is given in Table 6.

Table 6. Output characteristics diamond MESFET at room temperature and at 350 °C

Gate length 3.5μm width of 500μm	I_D (mA/mm)	V_{sat} (V)
300 °K (27 °C)	0.05	100
350 °C	5	25

V_{sat} is open — channel saturation voltage.

Combination of the concept of the high-temperature stable contact technology with the δ-doping concept has resulted in a δ-channel FET with a cross-section as shown in Fig. 12. The source and drain contacts were selectively grown, [10]; the metallization, both for the ohmic contacts and the Schottky contact, was prepared using qm-Si.

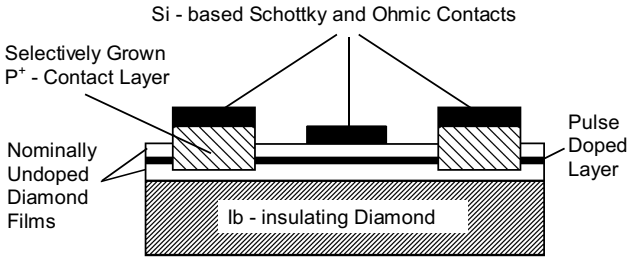

Fig. 12. A cross-section of a δ-doped MESFET prepared on a synthetic highly insulating nitrogen doped substrate

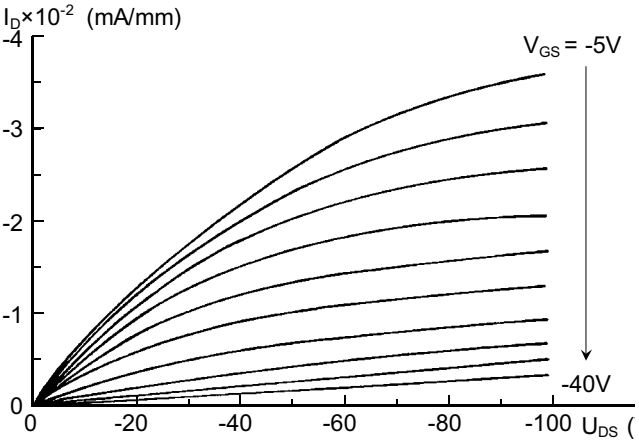

Fig. 13. The $I-V$ characteristics of a δ-doped FET at a) room temperature and b) 350 °C

The output characteristic are shown in Figs. 13.a, b at room temperature and 350 °C, respectively.

At 450 °C the gate diode reverse breakdown voltage is reduced slightly and the channel can not be pinched off completely. Thus, the high-temperature qm-Si contact technology still needs to be further refined when applied to these FET structures.

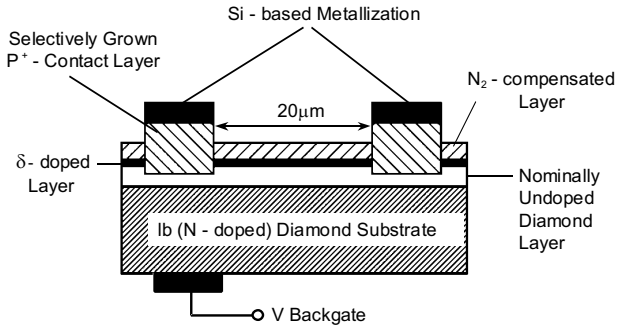

Fig. 14. A cross-selection of a junction FET using Ib (insulating by carrier freeze-out, nitrogen-containing, yellow) substrate as gate contact

Diamond JFET

In the structure illustrated in Fig. 14, the highly nitrogen doped substrate is used as a control gate from the back. In this case, the full source-to-drain separation represents the electrical gate and channel length simultaneously. No large-channel series resistances are expected.

For diamond it was found that the δ channel could be modulated at high current levels at a temperature of 300 °C see Fig. 20. At this temperature, full activation is expected according to a channel conduction activation energy of 0.1 eV, as determined by Hall measurements. The high gate resistance still causes a low transconductance and high pinch-off voltage.

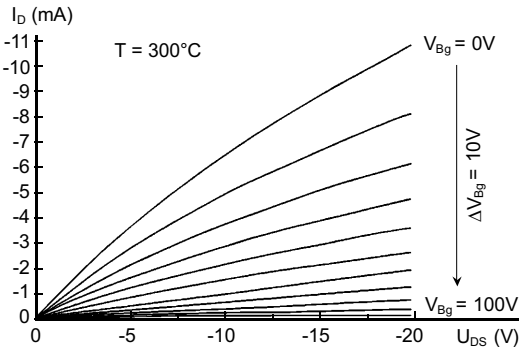

Fig. 15. The output characteristics: a) of a back gate junction FET; b) of a nitrogen/boron junction FET

As an alternative, a nitrogen-doped gate control layer can be placed on top of the δ-doped channel by selecting epitaxy, thus reducing the gate resistance considerably.

In that case, a high output current could be obtained at 200 °C as result of reduced activation energy of δ-doped channel of 0.14 meV (result in 65 % activation), [10]. Scaling this result to 1μm gate length leads to a maximum output current of 300 mA/mm.

Hence, with delta doped channel structures, full activation can be reached at a moderate temperature and high current levels comparable with these of other wide-gap semiconductor materials can be obtained.

Diamond Surface Channel FET

The termination of the diamond surface with hydrogen produces a room temperature activated hale conduction at the surface. The sheet change of this surface channel is of the order of $10^{13}\,\mathrm{cm}^{-2}$. Thus attempts have been made to utilize this surface layer as the FET channel. For these high-performance devices, a maximum channel current of 20 mA/mm and a maximum transconductance of 16.4 mS/mm have been reported for a gate length of 3μm.

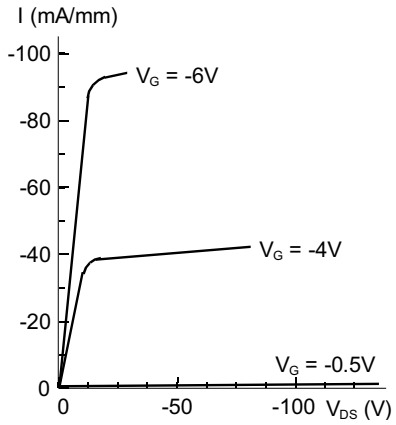

Fig. 16. The output characteristics of a surface channel FET prepared on a single-crystal substrate ($L_G = 3\mu$m)

Figure 16 shows the output of a device with a gate length of 3μm. The maximum current is 90 mA/mm at a gate bias of $V_G = -6$ V. This is several times the diode barrier height (SBH= 0.8 V) and shows that the characteristics are still dominated by a large series resistance due to a high channel sheet resistance and the relaxed geometry of the circular structure. The maximum trasconductance is 25 mS/mm. Breakdown at pinch-off is above $V_{DS} = -200$ V, which was the limit of the source unit, [16].

Diamond Schottky Barrier Diodes

Since a technical diode already needs to operate at room temperature with an acceptable series resistance, special attention has to be paid to the design of the active epitaxial layer configuration (doping-thickness profile).

There are two widely used basic techniques for the characterization of Schottky diodes which link the electrical performance to the physical junction properties.

I–V characterization: for the determination of the ideality factor, series resistance, Schottky barrier height, breakdown field strength and thermal activation energies.

C–V characterization: for the determination of the doping profile, built-in voltage, surface state density and deep level traps. In Fig. 17, the I–V characteristics of a homoepitaxial and heteroepitaxial diode representing the present state of the art are shown.

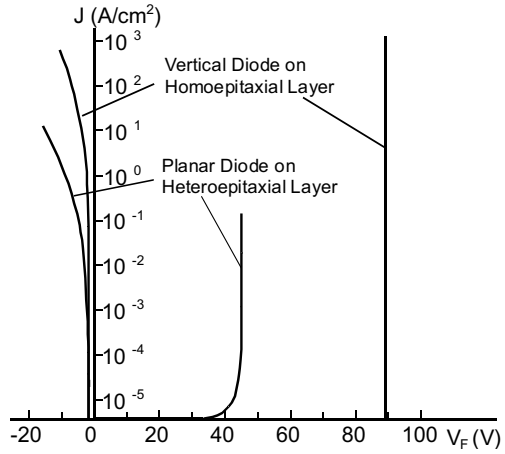

Fig. 17. The I–V characteristics of Schottky diodes on homoepitaxial diamond and heteroepitaxial diamond on silicon

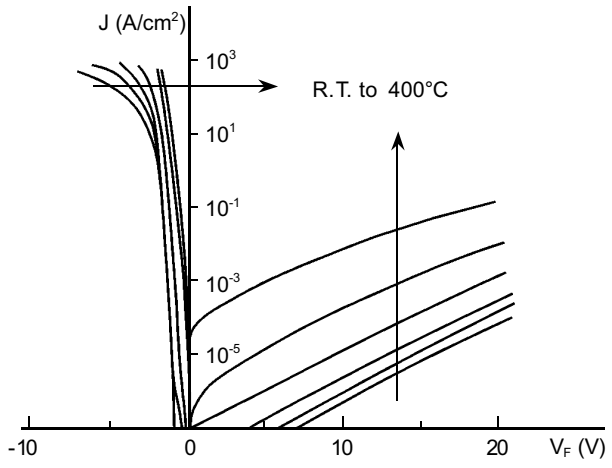

Fig. 18. The temperature dependent I–V characteristics of a diamond diode

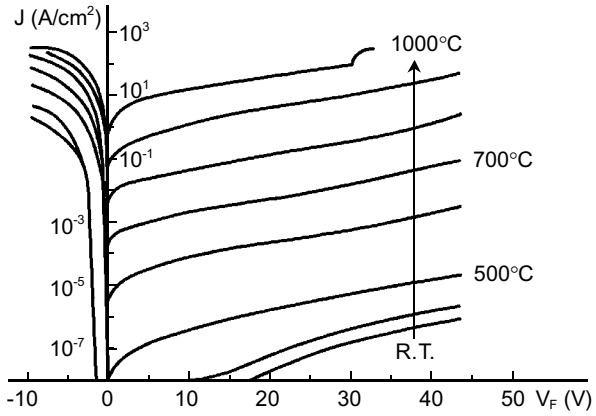

Fig. 19. The logarithmic I–V characteristic of a high-temperature Schottky diode

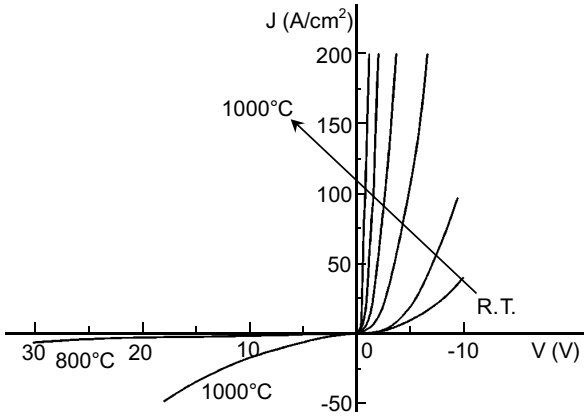

Fig. 20. The linear I–V characteristic of a high-temperature Schottky diode

By fitting the forward branch of the diode I–V characteristics (Fig. 17) using the equation

$$I = I_0\left[\exp\left(\frac{q(V - IR_S)}{nkT}\right) - 1\right] \tag{7}$$

the ideality factor, n, and the series resistance, R_S, of the diode can be extracted.

For diodes made on CVD — diamond layers, I–V characteristics exhibit a strong increase in the reverse current with bias and temperature (Fig. 18). The capacitance-voltage characterization is a versatile tool to determine the net doping concentration (*eg* $N_A - N_D$ and the built-in voltage (V_B) by plotting $1/C^2$ versus V. The slope of this plot is inversely proportional to the net doping concentration:

$$N_A - N_D = \frac{-2}{q\varepsilon_0\varepsilon_r A^2 \frac{\mathrm{d}(1/C^2)}{\mathrm{d}V}} \tag{8}$$

where A is the Schottky contact area.

At high reverse bias, breakdown in diamond diodes is usually not observed due to the steady increase of the reverse current up to the forward value and the high thermal stability of the material. However, by improving the quality of the material and the interface, breakdown behaviour becomes observable, as illustrated in Fig. 17.

A first investigation, on an inhomogeneously doped, successively grown layer [17], showed an increase in the breakdown voltage with increasing film thickness. However, the analysis of the depleted part of the profile showed that the thickness itself is not the decisive factor but that the decreasing surface doping concentration is. From this, the breakdown field strength E_{BR} of the material is estimated.

The extracted value of $E_{BR} = 2 \times 10^6$ V/cm is nearly the same as that measured for thick undoped heteroepitaxial diamond, [18] but it is still by one order of magnitude lower than the value measured on natural diamond. Therefore, it is still important to evaluate the possibility of CVD-diamond growth with a high breakdown strength.

Diamond High-temperature Schottky Diodes

One of the expected fields of application of diamond electronics is high temperature operation in the range

up to 1000 °C. An important prerequisite is the thermal stability of the contact metallization and of the diamond metal interface. The temperature stability of the interface of ohmic contacts was found to be not critical, since the contacts are made on highly doped layers and the alloying with refractory metals is performed at high temperatures.

Using a high-temperature stable contact, the feasibility of diamond devices operating at temperatures of up to 1000 °C has been demonstrated (Figs. 19 and 20), [19].

In this experiment, the diode has been cycled from R.T. up to 1000 °C, where the operation failed at 32 V reverse bias. The contact was held at each temperature for 15 min and the bias ramped up to 45 V within 1 min.

In the lower part of the characteristics, it can be seen that the reverse leakage current shows an extremely weak thermal activation up to 500 °C as compared with earlier results shown in Fig. 18. It is thought that this is the combined result of a stabilized interface, possibly passivating defects, a reduced surface doping concentration and a reduced acceptor compensation due to a low-nitrogen background.

In the linear current scale (Fig. 20), which is more relevant for the loss determination of a rectifier diode, hardly any reverse leakage current can be observed up to a temperature of 800 °C and a reverse voltage of 20 V. However, the forwards resistance was found to vary over two orders of magnitude upon heating to 1000 °C.

As a special requirement, the diamond surface has to be shielded against oxidation above 400 °C.

3.2 Diamond Bipolar Devices

Until now only diodes have been technologically processed and satisfactorily realised.

Diamond Bipolar Transistor

Due to problems with effective diamond donor doping no satisfactory characteristics of bipolar transistors have been reached.

Diamond PN – Junction Diodes

The first reported diamond diode was a planar PN diode made by ion implantation of boron as acceptor and phosphorus as donor. The current obtained was mainly defect-related. A vertical PN diode was realised by growing a boron-doped homoepitaxial layer on a synthetic nitrogen-doped diamond, [20].

Due to the high activation energy of the nitrogen donors, it could be operated only at temperatures above $\sim$ 600 °C. The I–V characteristics of this device are shown in Fig. 21.

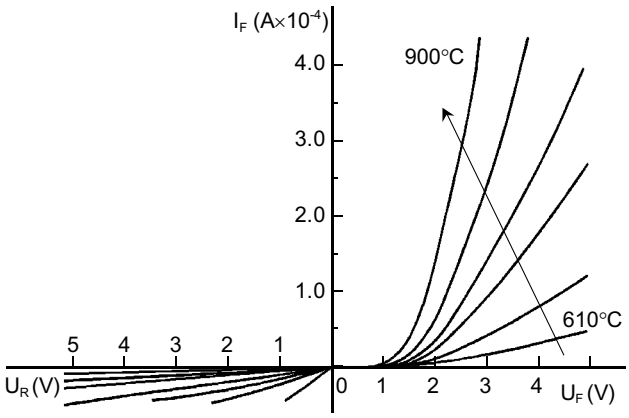

Fig. 21. The I–V characteristics of a homeoepitaxial PN diode operated between 610 °C and 900 °C

Alternatively, vertical hetero-junction PN diode structures are obtained by depositing P-type diamond on N-type Si substrates, [17].

However, it should be noted that the interface of these diodes is formed by the nucleation layer, and that these structures can only be operated at rather low temperatures due to the small bandgap of Si.

4 CONCLUSION

Silicon carbide and diamond are materials of the future for manufacturing semiconductor power devices.

Due to the ability to withstand high reverse voltages (over 10000 V), high current density (over 1000 A/cm^2), high temperature (over 300 °C), little on-state and circuit losses along with the ten times smaller active layer than in Si, SiC is going to push aside the use of Si as a base material for semiconductor power devices manufacturing in the near future.

Most promising are MOS structures, Schottky diodes and bipolar diodes. Blocking voltages of 1400 V in vertical MOSFETs are achieved already, 2600 V in lateral MOSFETs, 3000 V in SB diodes and 5500 V in PiN diodes. There is a possibility of developing a power JFET that could stand temperatures over 600 °C.

One of major obstacles for a faster breakthrough of SiC is achieving economical SiC wafers (having a diameter of more than 50 mm) of sufficiently high quality, without defects (micro-pipes!). So far, a wafer with surface area of few square millimeters was designed, its current thereby not exceeding a value of few amperes.

Micro-pipes represent a serious problem in wafer manufacture. Only one micro-pipe with a diameter of 1μm passing through the PN-junction causes the loss of latching capability. The amount of micro-pipes has been reduced from about 1000 to several hundred per square centimeter, and is still reducing. Among other existing problems, surface passivation and MOS fringe area (which is a critical factor for MOS structures) are to be solved.

The revolutionary finding that diamond can be synthesized at a low pressure by the chemical Vapor Deposition (CVD) method has opened up a new field of technical applications for this interesting material.

The active electronic applications for diamond are more demanding in terms of materials and process technologies, however, they offer the greatest scope of applications for CVD diamond not yet realised.

Expectations for diamond electronics have been largely based upon extrapolations from a few measurements made on either natural or high-pressure synthetic single crystals of diamond. The hole ($1600\,\mathrm{cm^2V^{-1}s^{-1}}$) and electron ($2200\,\mathrm{cm^2V^{-1}s^{-1}}$) mobilities of diamond hint at high-frequency applications. Thermal conductivities of up to $20\,\mathrm{Wcm^{-1}K^{-1}}$ point towards power devices capable of dissipating the heat generated by enormous current throughput. The wide bandgap of diamond (5.45 eV) coupled with the relatively high activation energy of the boron acceptor (365 meV) suggests that diamond would have a significant role in high-temperature electronics.

The factors limiting the use of diamond in electronics include the following: The high acceptor activation energy means that carrier saturation is achievable at $\sim 500\,^{\circ}\mathrm{C}$, which has ramifications for obtaining a material with sufficiently low sheet resistances for some applications. Then, it is a partially compensated P-type semiconductor. Furthermore, the hole mobility of diamond drops with temperature as a factor of $T^{2.8}$, yielding a figure of $\sim 125\,\mathrm{cm^2V^{-1}s^{-1}}$ at $500\,^{\circ}\mathrm{C}$. Coupled with these factors, the thermal conductivity of diamond decreases with temperature.

Although synthetic diamond has top predispositions as a material for semiconductor power devices manufacturing, several years will pass before its application starts due to the complicated manufacturing process.

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