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COMMUNICATIONS

DETERMINATION OF INTERFACE TRAP DENSITY IN UNIPOLAR STRUCTURES USING QUASISTATIC C–V METHOD

Pavol Písečný — Milan Ťapajna — Ladislav Harmatha — Andrej Vrbický *

The design and realization of computer controlled measurement for determination of the trap density on the insulator-semiconductor interface (D_{it}) using quasistatic C–V method is described. This method is simple, nevertheless, it is the most accurate technique for D_{it} determination in comparison to other ones. Using appropriate theoretical analysis, one can also obtain the energy distribution of interface trap density in the bandgap. In the experiment, two series of samples were used: (1) high-quality MOS structures prepared by different oxidation processes and (2) samples irradiated by 305 MeV Kr^+ and 710 MeV Bi^+ ions with different fluencies. From pulsed MOS capacitor measurement (the so-called C-t technique), surface generation velocity S_g was evaluated and, subsequently, the interface capture cross-section was calculated. All the results are discussed with regard to the amount of interface defects as well as their electrical activity.

K e y w o r d s: MIS structure, quasistatic C–V measurement, interface trap density

1 INTRODUCTION

The measurement of the low frequency capacitance-voltage (C–V) curve of a MIS (metal-insulator-semiconductor) structure is one of the methods for determining the energy distribution of the insulator-semiconductor interface trap density [1]. This parameter is related to the quality of the gate stack and its interface with underlying semiconductor. The interface traps create energy levels in the bandgap of the semiconductor, thus they act as generation-recombination centres. The origin of these defects yields from:

- structural defects, for example lattice discontinuity, silicon or oxygen vacancy created during oxidation
- metal impurity, for example Na, Pt, Au,
- defects induced by irradiation which breaks the atomic bonds in the crystal.

The present unipolar technology requires the value of $D_{it} < 10^{15}\,\mathrm{m}^{-2}\,\mathrm{eV}^{-1}$. The problem of the interface quality becomes essential with regard to present scale decreasing and replacement of silicon dioxide with a high-κ material insulator layer. There are many ways how to measure the low frequency C–V curve, however, the quasistatic charge-voltage method is mostly used at present. One of the main advantages of the low frequency C–V method is that the distribution of D_{it} is determined over the full width of the bandgap.

2 THEORY

For determining the energy distribution of the interface trap density it is necessary to know the dependence of band bending on the gate bias $\varphi_S = f(V_G)$. This dependence could be obtained from integration of the measured low frequency C–V curve and is given as [2]

$$\varphi_S = \int_{V_{FB}}^{V_G} \left(1 - \frac{C(V_G)}{C_I}\right) \mathrm{d}V_G\,, \tag{1}$$

where V_{FB} is the flat-band voltage and C_I is the insulator layer capacitance. The φ_S is linearly proportional to the energy in the bandgap

$$E - E_i = q(\varphi_S - \varphi_F)\,, \tag{2}$$

where φ_F is the Fermi level in the semiconductor. The capacitance of the interface trap is given as [1]

$$C_{it} = \left(\frac{1}{C_{LF\mathrm{real}}} - \frac{1}{C_I}\right)^{-1} - \left(\frac{1}{C_{LF\mathrm{ideal}}} - \frac{1}{C_I}\right)^{-1}\,, \tag{3}$$

where $C_{LF\mathrm{real}}$ is the measured capacitance and $C_{LF\mathrm{ideal}}$ is the capacitance of the ideal MOS structure obtained from the theoretical low frequency dependence $C = f(V_G)$ [2]. The density of interface trap is given by [1]

$$D_{it} = \frac{1}{q^2} C_{it}\,. \tag{4}$$

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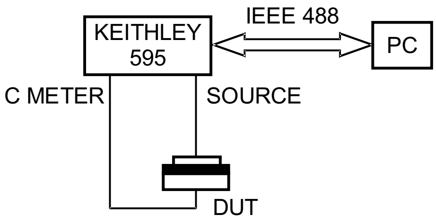

Fig. 1. Measurement set-up.

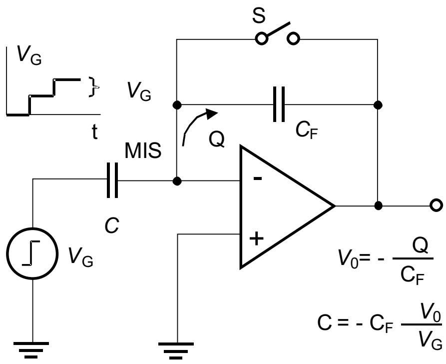

Fig. 2. Principle of quasi-static charge-voltage method.

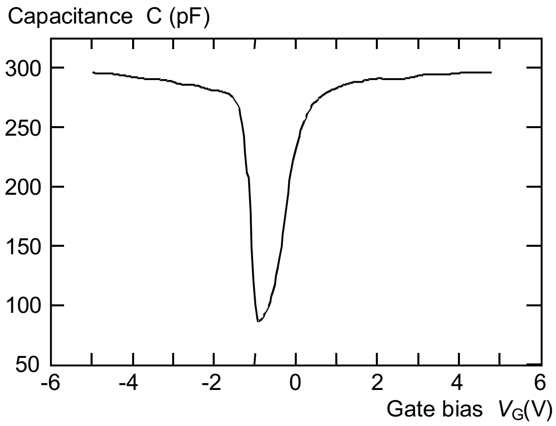

Fig. 3. Low-frequency C–V curve of structure FA 2-4.

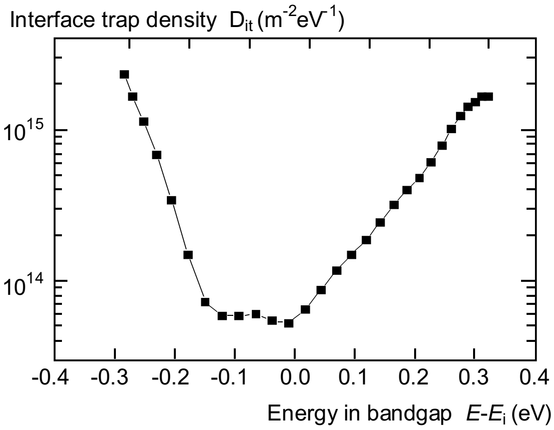

Fig. 4. Energy distribution of interface trap density structure FA 2-4.

Table 1. Parameters of oxidation process

Sample	FA 2–4	FA 3–2	PY	D0,D1,D2,D8
Oxidation ambient	$O_2 + 3\,\%HCl$	$O_2 + H_2$	dry O_2	dry O_2
Oxidation temperature (°C)	1050	1000	1050	1050
Oxide layer thickness (nm)	80	76	73	100

Hence, one can obtain the energy distribution of interface trap density $D_{it} = f(E - E_i)$ in the semiconductor bandgap by linking the values of energies from eq. (2) with the values of D_{it} from eq. (4) at the same gate bias. Performing C-t measurement [2] to acquire the surface generation velocity S_g, the magnitude of the interface capture cross-section σ_{ni} could be determined, which defines the electrical activity of traps as [3]

$$S_g = \sigma_{ni} v_{th} D_{it}\,, \tag{5}$$

where v_{th} is electron thermal velocity (for silicon $v_{th} = 1 \times 10^5\,\mathrm{ms}^{-1}$).

3 MEASUREMENT SET–UP

For quasistatic measurement we utilized a C–V meter Keithley 595 which implements the charge-voltage method (Fig. 1). In this method, a linear step voltage is applied to the gate of the MIS structure and subsequent charge transfer from the response to the voltage increment is measured (Fig. 2) [4]. Another way of quasistatic measurement is the current-voltage method. However, the charge-voltage technique has a better noise resistance in comparison with the current-voltage method. The next advantage arises from application of Q/t current, from which it is possible to distinguish the equilibrium of measurement. For controlling the measurement and data visualization, program ZENON was designed. The input parameters of the measurement are very important for the low-frequency C–V curve. The main parameter is the rate of the voltage step (voltage step and delay between single steps), which provides retrieving of the structure to the equilibrium state and thereby influences the magnitude of the oxide capacitance in inversion. Note that equation (3) can be applied only in equilibrium. For cal-

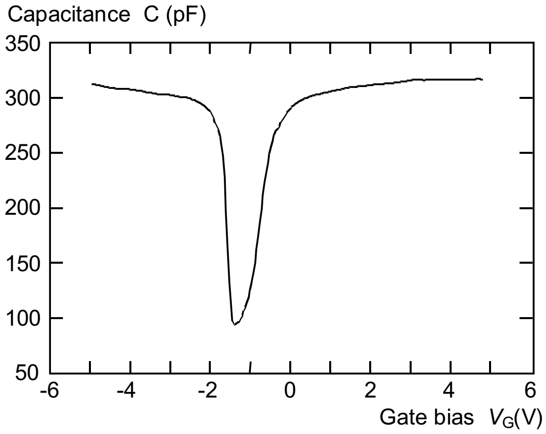

Fig. 5. Low-frequency C–V curve of structure FA 3-2.

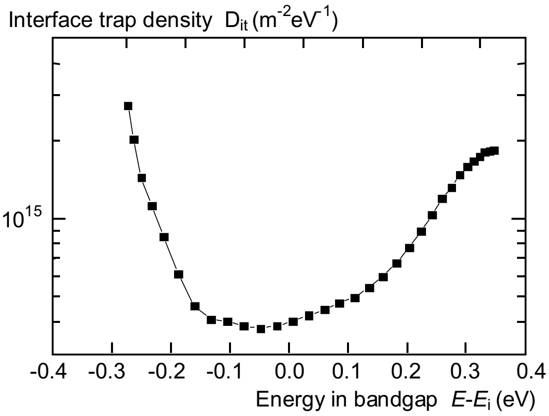

Fig. 6. Energy distribution of interface trap density of structure FA 3-2.

Table 2. Parameters of investigated structures (the first series).

Sample	FA 2–4	FA 3–2	PY
Oxidation ambient	O_2+ HCl	$O_2 + H_2$	dry O_2
V_{FB} (V)	−0.13	−0.69	−0.01
D_{it}(m^{-2}eV^{-1})	8.1×10^{13}	4.1×10^{14}	1.6×10^{14}
S_g (ms^{-1})	1.2×10^{-4}	6.6×10^{-5}	1.5×10^{-3}
τ_g (μs)	280	1220	1200
σ_{ni} (m^2)	8.15×10^{-24}	2.93×10^{-24}	9.37×10^{-23}

culation of the interface trap density energy distribution the program ARTEMIS was designed.

4 EXPERIMENT AND RESULTS

To verify the function of the designed measurement set-up and to demonstrate the method feasibility, two series of samples were analyzed. In the first one, high-quality MIS structures with SiO_2 as an insulating layer were fabricated by thermal oxidation in different ambient and temperature. The second series of samples were exposed to heavy-ion (Kr^+, Bi^+) irradiation with different fluencies in order to damage the SiO_2-Si interface. From the measurements described above, the cross-section of radiation defects was evaluated. The V_{FB} and S_g values are obtained from high-frequency C–V and C-t measurements, respectively [5].

An n-type, antimony doped, $\langle 100 \rangle$-oriented homogeneous wafer with resistivity of 2–5 Ωcm and thickness 300 μm was used as a substrate of all structures. The SiO_2 gate layer of all structures was prepared by thermal oxidation listed in Tab. 1. Gates were prepared by vapour deposition of Al with thickness 1.3 μm and patterned photolithographically. The samples were annealed in $N_2 + H_2$ at 460 °C for 20 minutes after manufacturing. After these steps, samples D1, D2 and D8 were exposed to various irradiations (Tab. 3).

Figures 3, 5 and 7 show experimental low-frequency C–V curves of structures FA 2-4, FA 3-2 and PY, respectively. As one can see, capacitance in strong inversion is equal to that in accumulation (n-type substrate), hence according to equations described in section 2, differences between experimental data and fitted theoretical ones yield the energy distribution of D_{it} in the band gap (shown in figures 4, 6 and 8).

For comparison, the interface trap density D_{it} was determined as mean values at ± 0.1 eV near the middle of the band gap (Tab. 2). The lower D_{it} of the structure FA 2-4 made in O_2 + 3 % HCl in comparison with the structure FA 3-2 made in $O_2 + H_2$ is probably due to gettering effects of Cl atoms at the Si–SiO_2 interface. It is interesting that structure FA 2-4 with interface trap density as low as 8.1×10^{13} m^{-2}eV^{-1} exhibits a higher value of surface generation velocity than sample FA 3-2 (with $D_{it} = 4.1 \times 10^{14}$ m^{-2}eV^{-1}). This effect is caused by changed electrical activity of interface traps regarding to the approximately 3 times higher interface capture cross-section of structure FA 2-4. From these results it is obvious that several methods have to be employed for complex study of interface.

Structure PY (Fig. 7) prepared by present technology in dry O_2 shows excellent flat-band voltage ($V_{FB} = -0.01$ V) and low value of D_{it}. It indicates a negligible amount of effective defect charge in SiO_2 layer and at its interface with silicon. However, S_g determined from C-t measurement has an exceptionally high value. This issue is reflected in a large capture cross-section of interface traps or, in other words, the concentration of traps at the interface is low but they act as efficient generation-recombination centers, thereby causing carrier mobility lowering in the channel. For their sufficient suppressing by process optimization it is necessary to use both equilibrium as well as non-steady state measurement methods.

Figure 9 shows low-frequency C–V curves of non-irradiated (D0) and irradiated (D1, D2 and D8) samples, where in the second case various ion masses and fluencies were used (Tab. 3). The values of D_{it} in Tab. 3 were determined at 0.22 eV over the middle of the bandgap (Fig. 10).

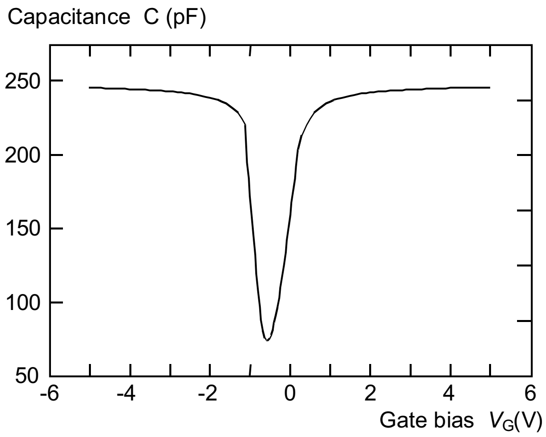

Fig. 7. Low-frequency C–V curve of structure PY.

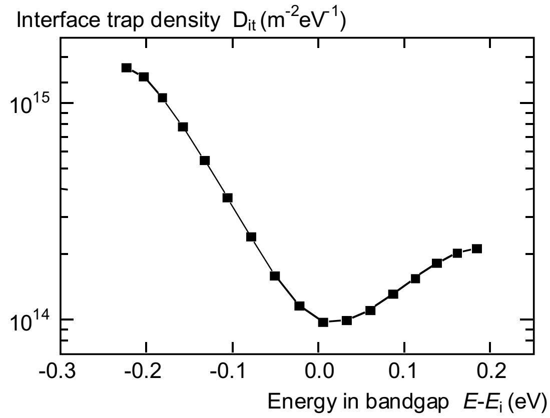

Fig. 8. Energy distribution of interface trap density of structure PY.

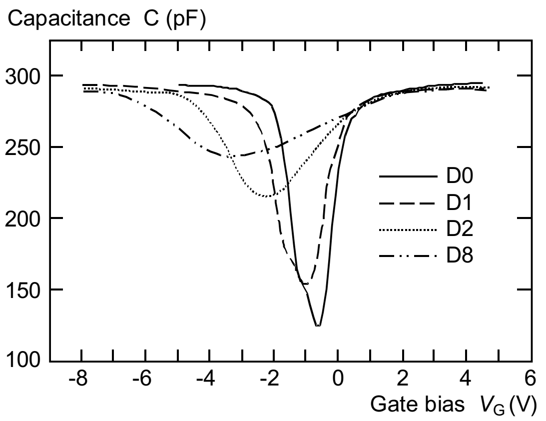

Fig. 9. Low-frequency C–V curves of structures D0, D1, D2 and D8.

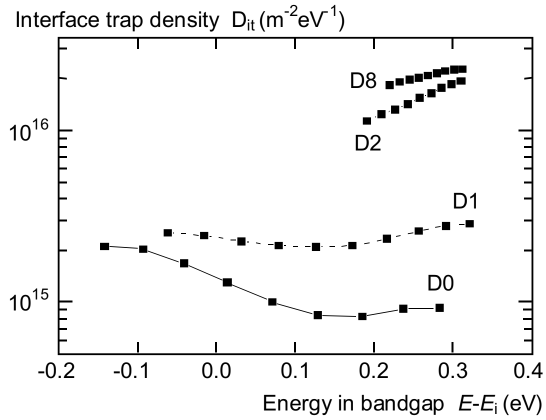

Fig. 10. Energy distribution of interface trap density structures D0, D1, D2 and D8.

Table 3. Parameters of investigated structures (the second series).

Sample	D0	D1	D2	D8
Irradiation	–	Kr^+	Kr^+	Bi^+
Energy (MeV)	–	305	305	710
Fluency (cm^{-2})	–	10^9	10^{10}	10^9
V_{FB} (V)	-0.1	-0.4	-1.2	-0.5
D_{it} ($m^{-2}eV^{-1}$)	9.1×10^{14}	2.4×10^{15}	1.3×10^{16}	1.86×10^{16}
S_g (ms^{-1})	2.2×10^{-3}	3.1×10^{-3}	1.3×10^{-1}	4.5×10^{-1}
σ_{ni} (m^2)	2.42×10^{-23}	1.29×10^{-23}	1.0×10^{-22}	2.42×10^{-22}

The radiation changes interface trap density D_{it} which can be observed on the slope of C–V curves in depletion and weak inversion region. Also the flat-band voltage V_{FB} shifts to a higher negative value with increasing fluency (compare D1 with D2). From the experimental data one can conclude that the increase of fluency and ion mass induces a growth of D_{it} and S_g, thus the interface deteriorate. Nevertheless, irradiated MOS structures retain their basic capacitance behavior even after high-energy radiation. One could speculate about the nature of the interface traps. Non-irradiated sample (D0) and sample D1 have interface capture cross-sections which are very close to counterpart samples D2 and D8 with approximately one order higher magnitude of σ_{ni}. Variation of interface capture cross-sections suggests transition of defects, therefore in the case of Kr^+ irradiation, an approximate threshold value of fluency $10^9\,cm^{-2}$ could be deduced. At fluencies higher than this value, Kr^+ irradiation results in the formation of high order defects. However, for a better understanding of the defect structure other analytical methods have to be used [6].

5 CONCLUSION

We described the design of a low-frequency C–V curve measurement set-up by quasistatic method. The methodology of measurement was investigated and the influence of input parameters upon the results of measurement was studied on a set of structures prepared by various technologies. From the experimental data and subsequent theoretical analysis, the energy distribution of interface trap density was obtained. Thereby, the quasistatic method represents an efficient tool for quality characterization of the semiconductor-insulator interface with a significant impact upon the charge transfer in unipolar technology. We also investigated the applicability of this method to the irradiated MOS structure. The density of interface traps and their electrical activity increased markedly with the fluency and the mass of heavy ions. In regard to measurement results, the interface Si–SiO_2 has a crucial influence on the irradiated MOS structure quality.

It is furthermore concluded that for complex investigation of interface properties, usage of other methods (*eg*, C-t technique) is desirable.

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References

[1] NICOLLIAN, E. H.—BREWS, J. R.: MOS (Metal Oxide Semiconductor) Physics and Technology, Wiley, New York, 1982.

[2] SCHRODER, D. K.: Semiconductor Material and Device Characterization, 2nd ed., Wiley, New York, 1998.

[3] PIERRET, R. F.: Solid-State Electronics **17** (1974), 1257.

[4] KEITHLEY instruments: Model 595 Quasistatic CV Meter : Instruction Manual. 1st ed. Cleveland, 1986.

[5] GURNIK, P.—HARMATHA, L.: An Assembly for Diagnostics of Semiconductor Structures, J. Electrical Engineering **48** No. 1-2 (1997), 52–56.

[6] BENKOVSKÝ, I. *et al*: XPS Surface Analysis of GaAs Thin Films Prepared by MBE, In: Proceeding of 1st International Workshop about MBE, Bratislava, EF STU Bratislava, 1991.

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