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SWITCHED CAPACITOR–BASED IMPLEMENTATION OF INTEGRATE–AND–FIRE NEURAL NETWORKS

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This paper is dealing with an analogue implementation of an Integrate and Fire neural network consisting of the learning synapse, which is a vital part of a self-organising neural network and the neurone designed according its biological counterpart. The proposed synapse includes a post-synaptic potential forming block, which makes it possible to uniquely characterise each synapse output in a complete neural network. This approach is conceptually closer to its biological counterpart. The design uses switched capacitor technique in order to be able to make the above described modifications realisable.

K e y w o r d s: integrate and fire neurones, learning synapses, neural networks implementation, built-in learning, hebbian learning rule

1 INTRODUCTION

Among all models of the neural networks the Integrate and Fire network is conceptually the nearest approach to the biological counterpart. This kind of network works with pulse coded signals where the value of the network output is given not only by the pulse frequencies of single neurone but by the correlation between the signals as well. Therefore the same number of neurones could have more computing power than neurones within another model of the network.

In many neural network applications an implementation of self-organised learning is required. The following neurone and synapse parameters should be taken into account: neurone hyper-polarisation threshold (when an input signal of the neurone reach this value, the neurone produces pulse on its output), time constant of a depolarisation sensitivity recovery (it is a time, when neurone is insensitive to the input signals), time constant of exponential decrease of post-synaptic potential — PSP (defines the shape of the neurone input signal from one synapse and is typical for this synapse), learning rate for up and down learning, and external NMDA learning threshold potential (the NMDA abbr. is derived from chemical substance N-metyl-D-asparat causing changes in synapse efficiency). It is important for each synapse to have a specific output signal characteristic (time constant of PSP discharge is assumed in our case). Therefore a PSP forming circuit is needed on the output of each synapse. [1], [2]

In this paper, the designed circuit for realisation of a neurone and a synapse with built-in hebbian learning is presented. In order to achieve an efficient synapse implementation from the area point of view, a switched capacitor technique was employed for the design. Moreover, in a switched capacitor circuit the synapse output and neurone depolarisation characteristic of each synapse and neurone can be easily and accurately tuned by capacitance ratio. Finally, the time dependencies are defined by the number of clock cycles and therefore they do not depend on the clock signal frequency. This offers the possibility to use the solution over a wide frequency range.

2 REALISATION

The neurones are the basic computing elements of the network and the synapses providing interconnections between them. In a biological network, the neurone consists of a body (soma), an input path (dendritic tree with synapses) and an output path (axon with synapses). The synapse is the point where information (a burst of pulses) is electrochemically transferred from the output of the transmitting neurone to the input of the receiving neurone. The influence of a synapse on a neurone is characterised by a single parameter — weight. The neurone pulses are transformed to the post-synaptic soma potential (PSP) with an exponential time characteristic, which allows the integration of signals over time. This exponential time characteristic differs between two different synapses. When the soma potential exceeds the input threshold of a neurone it causes hyper-polarisation of the neurone and the neurone "fires". This is followed by the recovery period (depolarisation) when the neurone is unable to fire.

In this approach the neurone has an analogue current input and a binary (logical) voltage output, and vice versa for the synapse. This allows to connect a number of synapses to a single input of a neurone. It is necessary to use a special neurone with an analogue voltage input for

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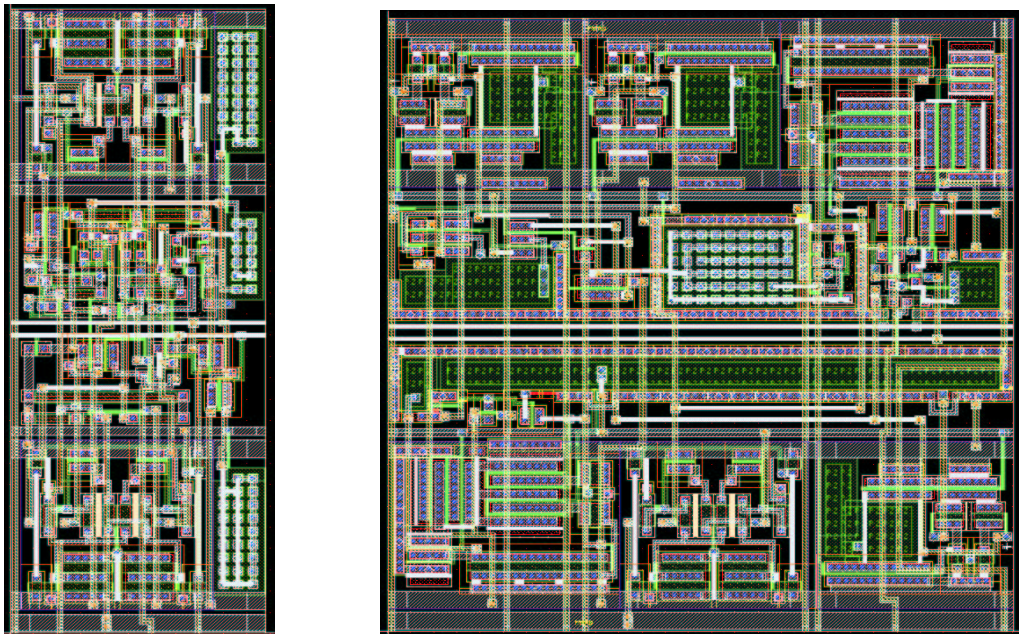

Fig. 1. Layout views of the realised "I&F" neurone and the learning synapse

the input layer of a complete network, to achieve voltage inputs of a chip.

The CADENCE Design Framework II Virtuoso and Composer tools and AMS 0.8 technology library was used for the design. All blocks were designed in order to build a robust library of all necessary parts to allow a simple approach to the design of a neurochip by simple placing of neurones and synapses and all necessary auxiliary parts of the design (*eg* clock generator, analogue memory maintaining circuits, inputs, outputs). This library could be used for automatic layout generation using leaf cell techniques.

The final layouts of the neurone and the synapse could be seen in Fig. 1. The spacing of all power and signal lines is equal on each neurone and synapse removing the necessity of additional interconnections to be placed by the designer. The area of the designed cells allows to place 15 full connected neurones on a $10\,\mathrm{mm}^2$ die (15 neurones, 225 synapses and all necessary auxiliary circuits including pads). This is the minimum die size to be produced within Europractice project in this technology

3 NEURONE

Each neurone has a simple current comparator at its input, which compares the current flowing in from the dendritic tree with an adjustable threshold. It provides also the depolarisation period of the neurone by increasing the threshold value. In this part two voltage-to-current converters are used. The output of the current comparator is fed to a dynamic D flip-flop controlled by a common clock signal (Fig. 2).

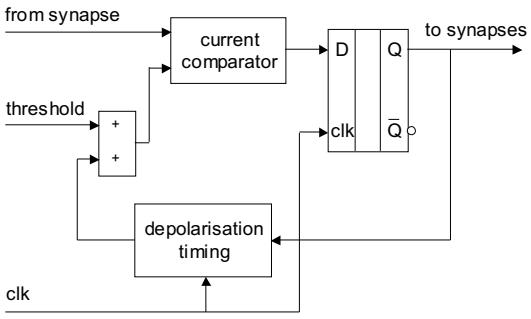

Fig. 2. Block diagram of the "I&F" neurone.

The dynamic D flip-flop consists of four inverters with long channel transistors, two buffers and two single transistor switches, which takes less area than a standard D flip-flop. This part performs output signal shaping to produce a pulse with a fixed width of one clock cycle. The neurone contains also the switched capacitor based circuit for timing the depolarisation started by the output pulse. [6] Several neurones were designed with different input sensitivities (maximum input currents are $40\,\mu\mathrm{A}$, $20\,\mu\mathrm{A}$, and $10\,\mu\mathrm{A}$ and minimal thresholds are $2\,\mu\mathrm{A}$, $1\,\mu\mathrm{A}$, and $0.5\,\mu\mathrm{A}$ respectively). The type of neurone used in a design depends on the number of the synapses connected to the input of the neurone.

4 SYNAPSE

The basic functions of the synapse are as follows: weighting of the neurone output signal, PSP-like shaping

of its output signal, analogue weight storage and weight refreshment [3]. A voltage adder computes a new start-value for the PSP circuit continuously (NewValue = PSP + Weight). After the "spike" from a transmitting neurone arrives this computed value is sent to the PSP circuit via a transfer gate. The PSP circuit consists of an array of 54 minimum value (unity) capacitors and two single transistor switches controlled by the main clock signal on opposite phases. The time constant of exponential decay of the PSP is given by the ratio of capacitors created within the array (the ratio is set by connecting the capacitors together. On the recent designed chip, the ratio was set by metallization at fabrication but we would like to use analogue switches in the future). The output of the PSP circuit is fed through a V-to-I converter to the dendritic tree. [5] In addition to this each synapse also provides a self-learning capability (weight changing depending on specific conditions) based on hebbian learning. The basic principle is very simple: When a transmitting neurone excites or contributes to excitation of the receiving neurone through the synapse in defined time-frame the synaptic weight is increased, otherwise the synaptic weight is decreased. The increase of the synaptic weight is proportional to the value of PSP, the decrease is proportional to the external signal *const.* T time-frame is given by the NMDA threshold potential and the value of PSP within the synapse. The weight change process is started by excitation of the receiving neurone (Fig. 3).

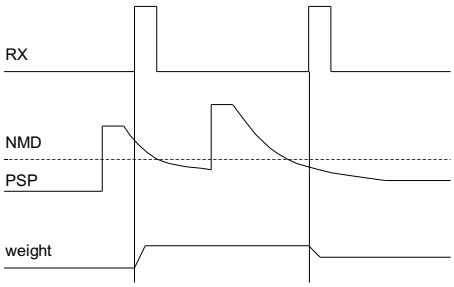

Fig. 3. Principle of the built-in hebbian learning

All these parts of the synapse use switched capacitor based circuits, instead of analogue memory. For example the soma potential capacitor and the auxiliary capacitor (used for shaping the PSP) using this technique have a value of 250 fF and 5 fF, respectively (compared to tens of pF in non-SC design [1], [4], [6]). The circuit for changing weight works on the principle of Hebb's learning rule, where the value of the change depends on the time difference between the output pulses of the transmitting and the receiving neurone, connected by the synapse (Fig. 4) [1].

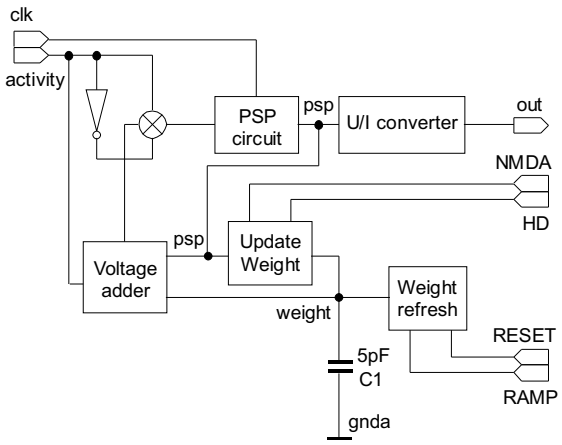

Fig. 4. Block diagram of learning synapse

There are basically two kinds of synapses: excitatory, which may cause hyper-polarisation of a neurone and inhibitory, which suppress the post-synaptic activity at the input of a neurone. The maximum synapse output current is approximately $2\,\mu$A in both directions.

5 SIMULATION RESULTS

Each part of this design was simulated with the Cadence Analogue Artist tool using SpectreS and SpectreSVerilog. We used models of the transistors from the AMS–$0.8\,\mu$m library version 3.12.

The synapse was simulated with a 500 kHz main clock signal, an initial memory value of 0.7 (when 1 is the maximum) and a capacitor ratio in the SC PSP circuit of $52:2$ (number of unity capacitors of the PSP and auxiliary capacitor respectively). The NMDA learning threshold and the learning constant for the down learning were 1 V above the analogue ground.

We simulated the neurone with the same clock rate as the synapse above, the ratio of the SC depolarisation block was $62:2$, the input threshold was set to 0 V and the dendritic input emulating the soma potential was $1\,\mu$A. The simulation results are shown on Figs. 5 and 6.

6 FABRICATION

For fabrication within a multi-project chip a test design has been constructed, consisting of two neurones with different input current sensitivity and one learning synapse connected between them. The total design area (without the area of the padring cells) is $266 \times 200\,\mu\text{m}^2$. The main system clock and the analogue voltage ramp for memory refresh are generated in cells in the padring of the chip. The total number of pads for providing measurements on the neurones and the synapse is 16 including power supply, ground and analogue ground. The die photo of the realised chip is shown on the Fig. 7.

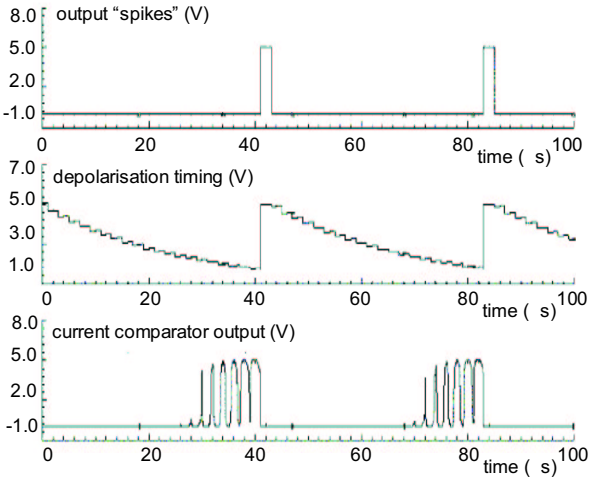

Fig. 5. Simulations of the neurone. The first signal shows firing of the neurone, the second shows output of the depolarisation circuit (after-hyperpolarisation) and the third shows the output of the input current comparator.

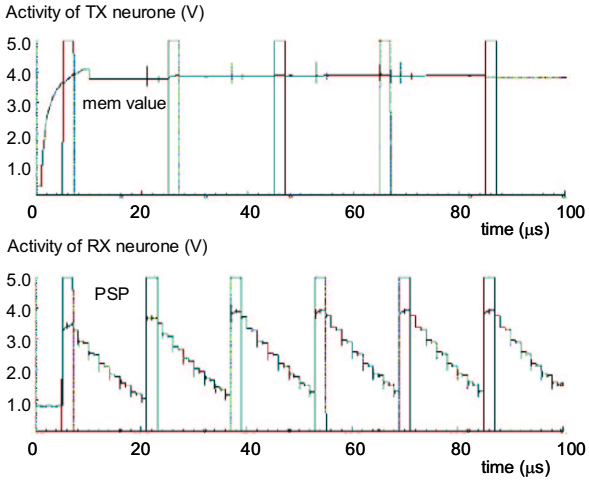

Fig. 6. Simulations of the synapse. The first graph shows output of the receiving neurone and the voltage across memory capacitor — weight value. The second graph shows the output of the PSP switched capacitor block and the output of the transmitting neurone.

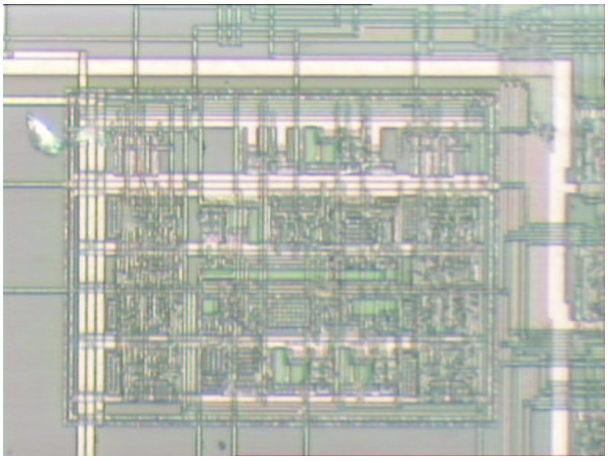

Fig. 7. A photo of the fabricated implementation of the synapse, two neurones and the clock buffering and distribution blocks above synapse and each neurone.

7 MEASURED RESULTS

All measurements were made using a dual channel HP digital oscilloscope connected to PC for signal capturing. The measured signals are depicted in Figs. 8–11.

Current consumption of this chip is $34\,\mu$A. The main problem in measurement was the sensitivity of the second neurone and synapse output. As you can see in Fig. 10, the PSP signal is activated for a relatively small voltage amplitude, in which the second neurone is firing (voltage range 200 mV).

In the other side, PSP signal has a similar shape such as simulation result (Fig. 5 or Fig. 6). The memory signal (Fig. 11) influenced by the signal NMDA (learning up or down), firing of neurones, signal constant and finally PSP. The clock signal is working on 1 MHz frequency.

8 DISCUSSION

In this paper an analogue design of a complete Integrate-and-Fire neural network using a leaf cell design technique is presented. This kind of network could be used for serial data processing such as artificial hearing or pattern recognition within sound data. Typical application using Hidden-Markov model of such network simulated in Matlab was presented in [1].

Each cell is described by a mathematical model for faster simulation of the complete network. The total design area in the AMS $0.8\,\mu$m process is approximately $155\times155\,\mu\text{m}^2$ for each synapse and $55\times155\,\mu\text{m}^2$ for each neurone, what makes it possible to place 15 neurones and 225 synapses on $10\,\text{mm}^2$ chip. In addition to this area it is necessary to use some auxiliary circuit blocks providing the power distribution, main clock signal buffering and distribution and generation of the synchronised saw-tooth signal for memory refresh circuits integrated in each synapse. This realisation needs 3 power supply inputs (Vcc, digital ground and analogue ground, where is an offset of 0.8 V necessary between analogue and digital ground) and 3 inputs for saw-tooth generator. The neurone and synapse were realised using a switched capacitor technique, which significantly reduces the design area, and this makes it feasible to include a PSP in each synapse. Therefore it is possible to define a unique output characteristic for each synapse, which is closer to the biological model. In other hand this technique increases the amount of the noise within the circuits.

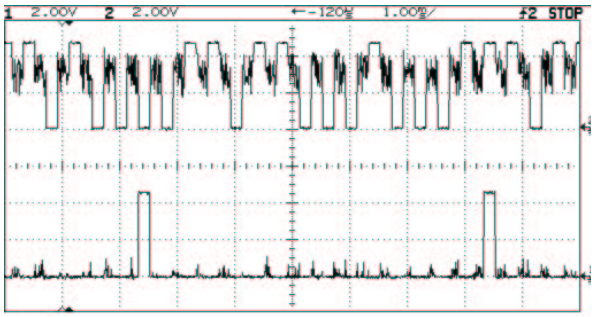

Fig. 8. The firing of both neurones with different threshold set-ups.

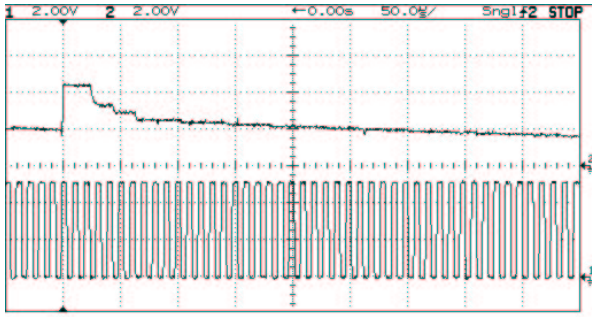

Fig. 9. Clock signal clk and PSP signal generated by the switched capacitor circuit within the synapse.

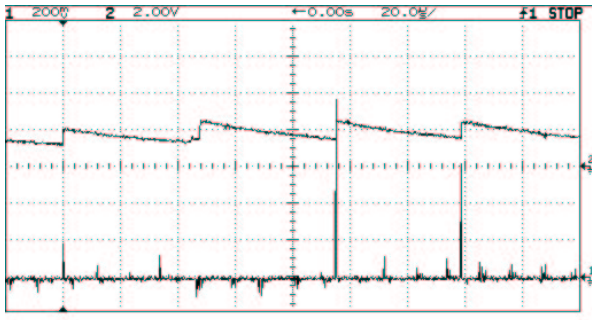

Fig. 10. Signal PSP depends on the firing of the second neurone. The spikes visible as the output of the neurone are just a switching noise, but strong enough to "fire" the synapse.

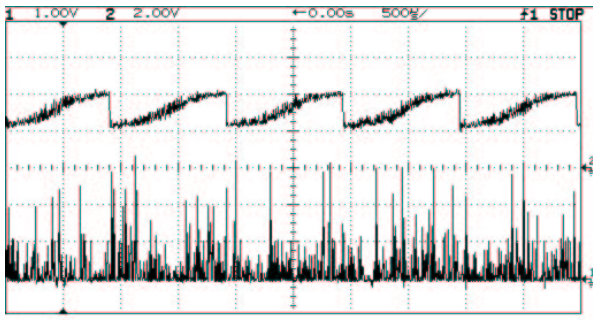

Fig. 11. Memory signal depends on the firing of second neurone. The basic triangular shape is defined by the non-functional memory refresh circuit driven by saw-tooth signal generator. The superposed noise is generated by the learning circuitry

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