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A DIGITALLY PROPULSIVE PLL FOR TIMING RECOVERY APPLICATIONS

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A novel timing recovery technique is presented that can conciliate small noise bandwidth and provide good jitter suppression with a sufficient wide loop bandwidth. It is also suitable to maintain a stable recovered clock even if the input signal exhibits missing transitions. The technique utilizes two restorative control voltages derived from two closed loops, acting in parallel, for phase and frequency tracking. The first one is composed at the filter output of a conventional Phase Looked Loop (PLL). A Digital Loop derives the second control voltage by the aid of a Digital to Analog Converter (DAC) which retains frequency lock for the whole bandwidth. The basic idea of the combined analog-digital twin-loop architecture is presented and also benefits and design issues are depicted.

K e y w o r d s: Clock Recovery, Synchronization, PLL

1 INTRODUCTION

The best-known architecture for timing recovery applications is the closed loop synchronizer. Phase Locked Loop (PLL) based implementations with analog or digital phase and/or frequency detectors are the most common building blocks for Timing Synchronization [1,2]. A major design consideration is that the clock must be recovered and remain stable for random input data. A common example is the non-return to zero (NRZ) data pulse streams, where several missing transitions can occur. In order to retain the clock stability, a PLL circuit usually utilizes a loop filter with a high DC gain or a filter with a large time constant. This results in a small loop bandwidth, which accounts also for noise and high frequency jitter suppression [2]. In contrast, the wide loop bandwidth is necessary to ensure the pull-in process, sufficient tracking of low jitter frequency (wander) and compensation of possible frequency deviation [1–5]. Thus, there is a clear conflict for loop parameter selection. So loop optimization, in order to balance the opposite constraints, becomes the designer's goal. Twin loop architectures like "quadricorrelator" with phase and frequency loops are sometimes adopted for this purpose [1, 2, 4, 5].

The technique presented in this paper is based on a twin loop architecture. The first loop, a digital one, aligns the VCO to be centred to the desired frequency, while the second analog loop tracks the phase difference. From another point of view the digital loop acts in a way to shift the VCO centre frequency as close as possible to the recovered clock frequency and retains its value constant. Based on that centre frequency, the collaborating analog loop, acting as in a conventional PLL, locks to the input phase difference. The digital loop augments the frequency stability in the case of input data missing transitions, by compromising the above mentioned conflicting design goals. An additional advantage is that it makes less stringent the dependence of the loop bandwidth on the component parameters and does not require a high quality VCO.

In the following sections the operation of the twin loop architecture is given along with simulation results. Also some design issues and circuit performance are discussed compared to conventional methods and the key advantages of the proposed technique are presented.

2 TWIN LOOP ARCHITECTURE

The main feature of the proposed method is the embedding of two control voltages derived from two contributing locked loops. As it is shown in the block diagram of Fig. 1, besides the PLL analog loop that produces the analog control voltage (V_a), a digital one has been added. The latter loop consists of a well-known sequential Phase/Frequency Detector (PFD) [2]. Its output is fed to an Up-Down counter, which gives rise to the digital part control voltage (V_d) by driving a Digital to Analog Converter (DAC). If the phase of the incoming signal leads or lags, an equivalent Up or Down control signal is generated. This forces the Up/Down counter to fluctuate its output and therefore to increment or decrement the DAC output voltage. In other words, any phase error alters the DAC voltage managing to compensate the phase error, which is a common procedure in many closed loop applications. The digital loop, as stand-alone, sometimes is adopted in clock recovery applications acting as a digital PLL [6, 7]. The filter and the DAC outputs are finally added and the control voltage (V_c) is derived.

The procedure becomes complicated as the digital loop collaborates with the analog loop and none of them has an independent operation. In Fig. 2, simulated results by

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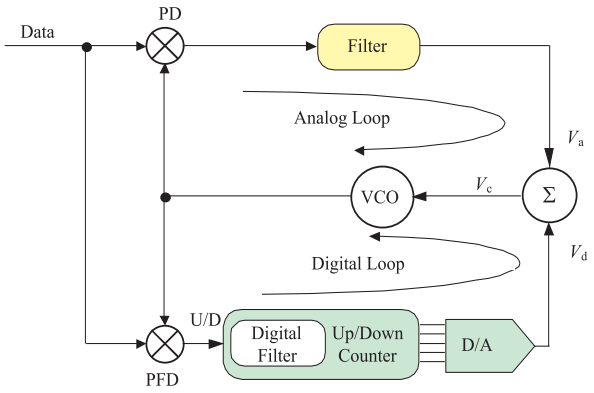

Fig. 1. Twin-loop architecture: Analog & Digital Loop.

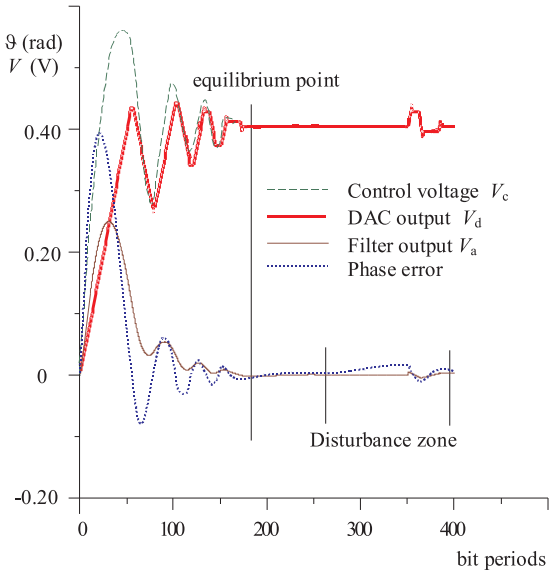

Fig. 2. Total and contributed (digital and analog part) control voltages and resulting phase error versus bit periods (simulation time).

VisSim [8] software present the combined loop operation and show the transient response for phase error versus time. The simulation model adopts an 8-bit resolution digital part, while the analog loop is considered as being second order with a passive lead-lag filter. Initially, a training sequence is considered as input data that is followed by a burst of missing transitions (disturbance zone). The total control voltage and its two components, as well as the phase error, are shown versus time. The bold line is the digital control voltage V_d (DAC output), which is forcing to settle to an equilibrium point. In a similar way, the analog control voltage V_a (filter output, thin line) pushes to lock the loop as an additive stabilizing force. The summation of the two voltages is the total control voltage V_c (dashed line). This results in filter contribution reduction as the digital control voltage approximates the desired control voltage. The operation continues up to the point that the loop is locked (beyond the equilibrium point) where the phase error (dotted line) diminishes.

Taking into account the VCO gain K_0 and the VCO centre frequency (ω_0) we can write the recovered VCO angular frequency in its linear mode as:

$$\omega_{out} = \omega_0 + K_0 V_c \text{ or } \omega_{out} = \omega_0 + K_0(V_a + V_d) \text{ that is}$$
$$\omega_{out} = (\omega_0 + K_0 V_d) + K_0 V_a \,. \quad (1)$$

Equivalently we can write:

$$\omega_{out} = \omega_{od} + K_0 V_a \quad (2)$$

where $\omega_{od} = \omega_0 + K_o V_d$ is a new centre frequency. So the digital loop shifts the centre frequency as close as possible to the proper (equal to the bit rate) frequency. Based on that frequency ω_{od} the analog loop operates as a conventional PLL by suppressing noise and by tracking the phase error.

From the above description it is clear that the digital control voltage is dominant (coarse adjustment) in relation to the analog one (fine adjustment) and retains its value even during the absence of data information. Therefore the digital loop operates as an equivalent filter with large DC gain that is essential for clock recovery applications. The digital control voltage alters in a quantized manner, by an up or down step. In this way, no rapid frequency steps are allowed and thus any abrupt input disturbance generates only minor frequency deviation. This characteristic provides an advantage for clock recovery applications, where abrupt frequency changes are not expected acting like a flywheel.

At the right side of Fig. 2 the loop behaviour in the case of a burst of missing transitions (disturbance zone) is shown. Loop filter output is zero while the DAC output retains its last value. Beyond this point the clock information is exclusively maintained by the digital loop and the control voltage does not decline. Despite that, a phase error is produced, as it is shown by the dotted line in Fig. 2, due to the quantized nature of the digital control voltage, which allows a small frequency mismatch. At the data reappearance the system resynchronizes and suppresses the phase error. Both control voltages present a transient response up to a point where the phase error is eliminated.

3 PERFORMANCE AND DESIGN ISSUES

The major contribution of the proposed design is the incorporation of a digital stage in the PLL clock recovery circuit. This stage provides an extra design parameter that influences the circuit's performance. A first issue is the digital control voltage V_d that is related to the frequency output resolution considering an "n-bit" digital part (n-bit Up/Down counter with an n-bit DAC). The digital control voltage is then $V_d = \left(V_{ref}/2^n\right)(D_{U/D} - 2^{n-1})$. $D_{U/D}$ is the Up/Down counter's output and the term 2^{n-1} has been introduced as an offset in order to make the V_d symmetric around zero Volts. V_{ref} is the DAC's reference voltage adjusted to be equal to the VCO

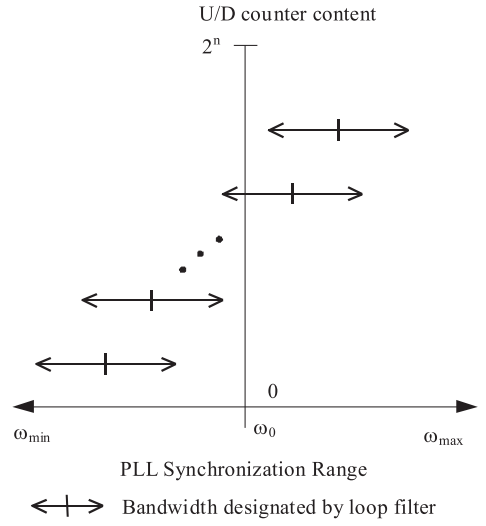

Fig. 3. Shifted individual ranges cover the total PLL *pull-in* range.

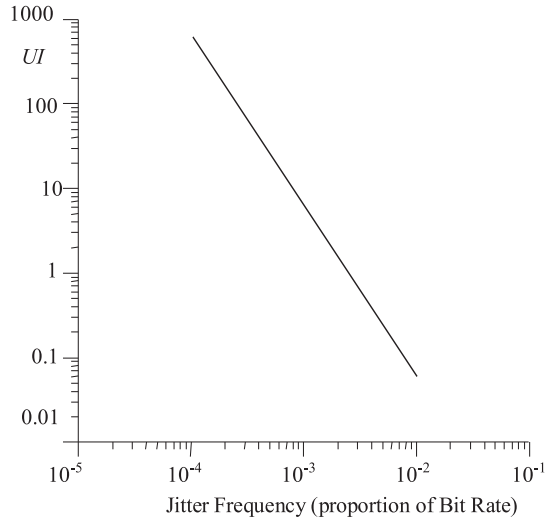

Fig. 4. Jitter tolerance in UIs versus jitter frequency as a proportion of bit rate.

input voltage range. The two-phase detectors in Fig. 1 can be constructed as a single sequential phase/frequency detector, like the one used in 74HC4046 PLL devices (Phase Comparator II) [1]. The phase/frequency detector is activated by the detection of new transition appearance. This is achieved by comparing the current input data with a one-bit delayed version of the data in order to make it tolerant and insensitive to missing transitions.

The detector output drives the Up/Down counter through a simple Random Walk digital filter embedded in the Up/Down counter, shown in Fig. 1. This filter acts so that the Up/Down counter is permitted to count Up when at least three sequential Up pulses arise, and similarly count Down when at least three sequential Down pulses arise. This stage provides a kind of inertia and ensures that the analog loop operation should be shifted to a new centre frequency only if there is a persistence to change. This persistence is evident by the number of consecutive pulses that appear. The number three has been chosen experimentally by simulation. This operation is very important when the loop is locked. As the phase error is minor, the digital loop freezes its contribution, forcing the VCO to run in a new centre frequency ω_{od}, as specified in Eq. (1). The loop then acts as a conventional PLL that tracks the phase error and the additive noise.

The digital control voltage V_d determines a frequency control step $\Delta\omega$ that can be easily calculated. For a full-scale adjustment, the DAC reference voltage must be equal to the VCO input voltage range, which, for simplicity reasons is considered equal to 1 ($V_{ref} = 1$). The quantized VCO output frequency resolution can be calculated as $\Delta\omega = K_0 V_{ref}/2^n = K_0/2^n$. The VCO output, due to the DAC contribution, is then $\omega_{od} = \omega_0 + \Delta\omega(D_{U/D} - 2^{n-1})$. The frequency change step $\Delta\omega$ represents also the maximum frequency mismatch when the loop is locked and data exhibits missing transitions. As described previously, due to this mismatch a phase error is originated and accumulates. This is shown in the right part of Fig. 2 (named as "Disturbance Zone") where the phase error, dotted line, increases until the reappearance of input data. The magnitude of peak phase error (ϑ_e) depends on the frequency mismatch, the number of missing transitions L and the VCO gain K_0. Estimation of ϑ_e is based on the time difference between respective crossings relative to the input signal period. So, ϑ_e, expressed in rads, is $2\pi L|T_{in} - T_{out}|/T_{in}$ where T_{in} and T_{out} are the input and recovered data periods at the beginning of disturbance zone. Finally, $\vartheta_e = 2\pi L|T_{in} - T_{out}|/T_{in} = 2\pi L|\omega_{out} - \omega_{in}|/\omega_{out}$.

It is interesting to know the worst case that takes place for maximum frequency mismatch $\Delta\omega$ and for minimum output frequency ($D_{U/D} = 0$, $\omega_{out} = \omega_0 - K_0/2$). If we consider the value of K_0 as a percentage $M\,\%$ of the clock rate, then ϑ_e is $\vartheta_e = 2\pi LM/(2 - M)2^{n-1}$.

As an example it is considered that $M = 0.01\,\%$ up to $10\,\%$ of the clock rate, which specifies an acceptable loop bandwidth for most clock recovery applications. Regarding an 8-bit digital loop ($n = 8$), the peak phase error due to $L = 32$ identical bits results in 0.0000789 up to 0.0789 rads.

Usually, a critical design issue is the choice of the loop filter. As long as only the digital loop retains the required DC control voltage, a simple passive loop filter is adequate for our case. This is because the loop filter's DC gain must be minimal (equal to 1 for a passive filter) in order to prevent an additive DC offset. As it was mentioned in the introduction, the loop filter determines the synchronizer's performance. Sometimes, particularly for clock recovery applications, opposite constraints coexist and must be compromised. The major conflict is between the noise bandwidth — output phase jitter and the pull-in range [1, 4, 5]. In the proposed technique the Phase-Frequency detector facilitates the digital loop to

resolve the pull-in process while the DAC's output provides the necessary (equivalent) high DC gain. So a narrow loop filter that satisfies all transient and jitter filtering requirements can be arranged. This results in smaller noise bandwidth and better jitter tolerance. Due to the aperiodic characteristic of the phase/frequency detector, even if the loop is unlocked, a reliable signal is always present [1]. This could extend the synchronization range (Hold Range) of the digital loop boundlessly. The final synchronization range is only limited by the VCO frequency range itself, considering that the latter is covered by the DAC output voltage range. In Fig. 3 the bandwidth designated by the loop filter, *ie* , the lock-in range, as well as the total synchronization range are presented. Because the digital loop tracks the frequency difference, the predefined bandwidth acts as to be placed in one of 2^n discrete steps. Each one of these steps corresponds to the lock-in range of the analog loop alone and it is specified by its characteristics (phase detector gain, VCO gain, filter type) [1]. So the total synchronization bandwidth is covered in 2^n overlapping steps as shown in Fig. 3. The shift step is equal to $\Delta\omega$ as previously mentioned.

The rate that the digital loop tracks the phase difference specifies its jitter tolerance. The jitter tolerance calculated for minimum phase error is illustrated in Fig. 4. The horizontal axis is the input jitter frequency as a proportion of the bit rate and the vertical axis is the peak-to-peak amplitude in Unit Intervals (UI pp). For the evaluation, the input data is considered to have jitter on it in the form of frequency modulation [5]. At low frequencies (wander) the digital loop provides very high gain, and thus a significant amount of jitter can be tracked. At higher jitter frequencies the digital loop contribution is reduced. The loop filter tracks higher jitter frequency while the digital filter prevents the digital loop operation for high rate of phase-error alternations.

4 CONCLUSIONS

A novel Digital/Analog twin Phase Locked Loop suitable for clock recovery applications has been presented. With the aid of the digital part the clock recovery circuit has an extra design parameter and the loop characteristics can become more relaxed compared to the conventional methods. Also, wide loop bandwidth, acceptable jitter suppression and small noise bandwidth can coexist. Finally a major feature for the proposed technique is its ability to retain stability even if the data exhibits missing transitions.

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