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FAST DETERMINATION OF GENERATION PARAMETERS OF MOS STRUCTURES

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In this article we describe the design and realisation of computer controlled measurement for determination of the minority carrier lifetime using the constant capacitance-time method (cC-t). Unlike the Zerbst method, the cC-t technique does not require the acquisition of the entire capacitance-time curve or the derivative of the experimental data. The usage of the cC-t technique considerably reduces the data-acquisition time, especially for devices with high lifetimes. One can also obtain lifetime profiles for non-uniformly doped samples.

K e y w o r d s: MOS structure, capacitance measurement, minority carrier lifetime

1 INTRODUCTION

The pulsed gate voltage measurement of the transient capacitance of a MOS capacitor (MOS-C) is an important method for determining the generation minority carrier lifetime τ_g in semiconductors. This parameter is directly related to defect density in the operation region of the semiconductor. Usually, the MOS-C is driven from accumulation into deep-depletion with a voltage step, the resulting capacitance transient is measured, and a Zerbst plot is obtained. The lifetime is then calculated from the slope of the straight-line portion of the Zerbst plot [1].

The data acquisition time is essentially given by the MOS-C. Therefore the Zerbst technique is impractical for capacitors with relaxation times of the order of tens of minutes or more because of the need to stabilize the temperature and avoid optical generation during measurement, or for a large number of measurements, *eg*, for wafer testing. Often, it is also desired to obtain the depth profile of the lifetime, thus the variation of the lifetime with the distance into the bulk of the semiconductor, for example to assess the effect of processing, the efficacy of gettering techniques, and to find lifetime profiles for accurate numerical models of devices. However, results obtained using the Zerbst method represent only an integral value of τ_g.

Pierret and Small [2] proposed a multistep constant-capacitance technique (cC-t) that is an excellent alternative to the Zerbst technique. An initially deep-depleted MOS-C is maintained at a constant capacitance C_{fix} by adding charge to the gate to match that building up in the inversion layer. As originally proposed, a custom bias supply feedback circuit is used to take the capacitance through a number of steps during each of which the MOS-C is kept in deep depletion. The resulting voltage transients consist of a series of straight lines of different slopes, which gives τ_g for different depletion widths [3, 4].

We have replaced the custom circuit with a personal computer controlling a digital voltage source. In this paper the measurement set-up and the MOS theory used in the software are described.

2 THEORY

Let us consider an n-type silicon MOS-C. The applied gate voltage drop spans over the oxide and the semiconductor [5]

$$V_G = V_{ox} + \varphi_s \,. \tag{1}$$

The gate voltage must be swept to balance the building up of the inversion layer charge Q_{inv}

$$\frac{\mathrm{d}V_G}{\mathrm{d}t} = \frac{\mathrm{d}Q_{inv}}{\mathrm{d}t}\frac{1}{C_{ox}} \,, \tag{2}$$

where C_{ox} is the oxide capacitance.

The term $\mathrm{d}Q_{inv}/\mathrm{d}t$ is determined by thermal generation of electron-hole pairs in the bulk space charge region (scr), by lateral surface scr generation, surface scr generation under the gate, and quasi-neutral bulk generation [6]. Using the Shockley-Read-Hall equation, the generation rate in scr is given by n_i/τ_g. One obtains the generation of the minority carriers

$$\frac{\mathrm{d}Q_{inv}}{\mathrm{d}t} = \int_{x_\infty}^{x} \frac{qn_i}{\tau_g(x)}\mathrm{d}x + qn_i S_g + \frac{qn_i^2 D_n}{N_d L_n} \,, \tag{3}$$

where q is the elementary charge, N_d is the doping concentration, x_∞ is the final depletion width corresponding

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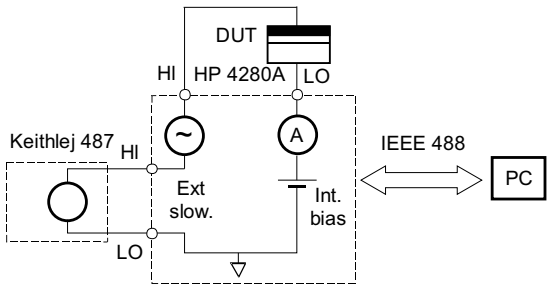

Fig. 1. Block diagram of set-up used to perform multistep constant-capacitance method

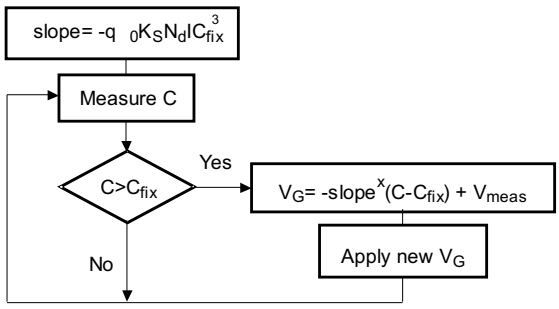

Fig. 2. Algorithm of keeping constant capacitance. When computer detects increasing of C above C_{fix} it increases gate voltage

to equilibrium strong inversion, S_g is the surface generation rate, and D_n and L_n are the diffusion coefficient and the length of electrons in the quasi-neutral bulk, respectively. The generation lifetime $\tau_g(x)$ varies as the density of traps changes with the depth. For profiling of $\tau_g(x)$ we can use two methods of evaluating the obtained voltage transients, standard and multistep (also called modified) techniques.

Standard cC-t technique. For calculation of $\tau_g(x)$ we use the slopes of the gate voltage transient $|\mathrm{d}V_{add}/\mathrm{d}t|$. Here, we ignore the surface generation and diffusion of the minority carrier from the quasi-neutral bulk. By integration one can obtain the generation rate from eqn. (3)

$$G = \frac{n_i(x_{fix} - x_\infty)}{\tau_g} A\,, \tag{4}$$

where A is the gate area, and x_{fix} is the width of scr kept constant during the measurement. Hence, $x_{fix} - x_\infty$ is the active region of bulk generation. It can bee shown [5] that

$$x_{fix} = \varepsilon_0 K_S \Big(\frac{1}{C_{fix}} - \frac{1}{C_{ox}}\Big) A\,, \tag{5}$$

$$x_\infty = \varepsilon_0 K_S \Big(\frac{1}{C_\infty} - \frac{1}{C_{ox}}\Big) A\,, \tag{6}$$

where $\varepsilon_0 K_S$ is the permittivity of the semiconductor.

Substituting eqn. (4) to eqn. (2) we can obtain for the value of the generation lifetime

$$\tau_g = \frac{q\varepsilon_0 K_S n_i \big(\frac{1}{C_{fix}} - \frac{1}{C_\infty}\big)}{C_{ox}\big|\frac{\mathrm{d}\,V_{add}}{\mathrm{d}\,t}\big|} A^2\,. \tag{7}$$

Using eqns. (5) and (7), and changing the value of the voltage pulse, *ie*, changing the scr width, we can profile the generation lifetime.

Modified cC-t technique. For monitoring of the depth profile we use also the difference between two adjacent slopes $|\mathrm{d}V_{add}/\mathrm{d}t|$. The traps at the interface SiO_2–Si below the gate are saturated in a short time, so their contribution is low. More significant are the traps along the scr lateral surface, and their contribution is constant [6]. Consequently, inserting eqn. (3) to eqn. (2) we can obtain the difference of adjacent slopes as

$$\begin{aligned}\frac{\mathrm{d}V_{add}}{\mathrm{d}t}\Big|_{(i)} - \frac{\mathrm{d}V_{add}}{\mathrm{d}t}\Big|_{(i+1)} &= \frac{qn_i}{C_{ox}} \int\limits_{x_{i+1}}^{x_i} \frac{\mathrm{d}\,x}{\tau_g} = \frac{qn_i\big(x_{(i)} - x_{(i+1)}\big)}{\tau_{g(i)} C_{ox}} \\ &= \frac{qn_i\varepsilon_0 K_S}{C_{ox}\tau_{g(i)}}\Big(\frac{1}{C_{fix(i)}} - \frac{1}{C_{fix(i+1)}}\Big),\end{aligned} \tag{8}$$

where $\tau_{g(i)}$ is the generation lifetime between widths $x_{fix(i)}$ and $x_{fix(i+1)}$. By simple editing of eqn. (8) we obtain

$$\tau_{g(i)} = \frac{qn_i\varepsilon_0 K_S\big(\frac{1}{C_{fix(i)}} - \frac{1}{C_{fix(i+1)}}\big)}{C_{ox}\big(\frac{\mathrm{d}\,V_{add}}{\mathrm{d}\,t}\big|_{(i)} - \frac{\mathrm{d}\,V_{add}}{\mathrm{d}\,t}\big|_{(i+1)}\big)} A^2 \tag{9}$$

and with eqn. (5) we can profile the generation lifetime $\tau_g(x)$. The surface generation and diffusion of minority carriers from the quasi-neutral bulk are cancelled because they are constant at each step. Finally we obtain a more accurate value of τ_g.

3 MEASUREMENT SET–UP

In our implementation a personal computer running under MS-DOS controls the measurement (Fig. 1). A Hewlet-Packard 4280A 1 MHz C Meter/C-V Plotter is utilized to measure the device capacitance. The computer's timer chip serves as the time base. By programming the 8253 timer chip, the clock rate is increased to around 1165 interrupts per second, for a granularity of close to 858 μs between clock pulses, rather than the 55 ms between normal clock pulses (18.2 times per second). The gate voltage on the MOS-C is incremented using a Keithley 487 Picoammeter/Voltage Source (up to 1 mV resolution) as necessary to maintain the capacitance near the desired measurement value. The system is capable of holding the capacitance constant better than 0.05 % on devices with generation lifetimes of the order of hundreds of microseconds.

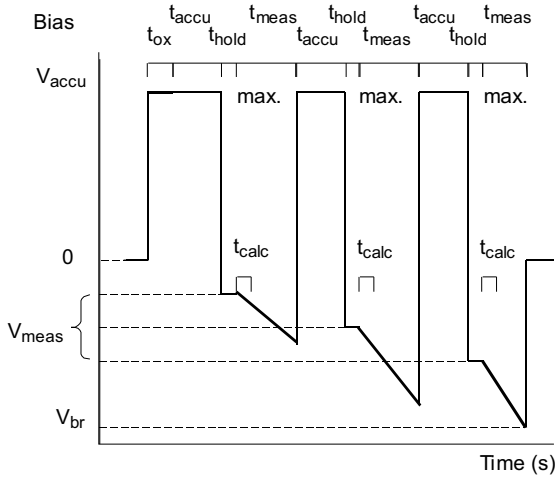

Fig. 3. Multistep output voltage sweep waveform

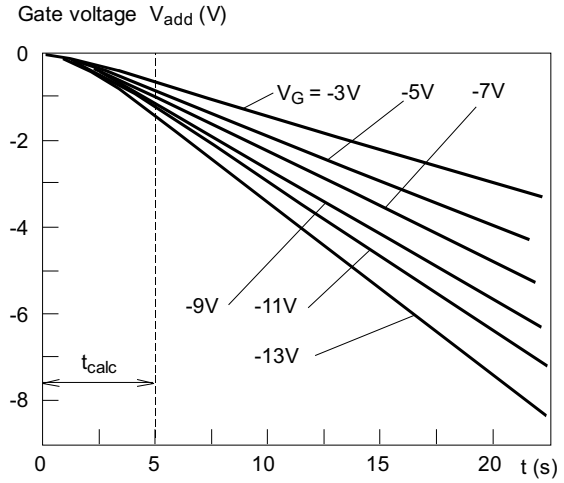

Fig. 4. Transient $V_G(t)$ plot obtained using multistep cC-t technique

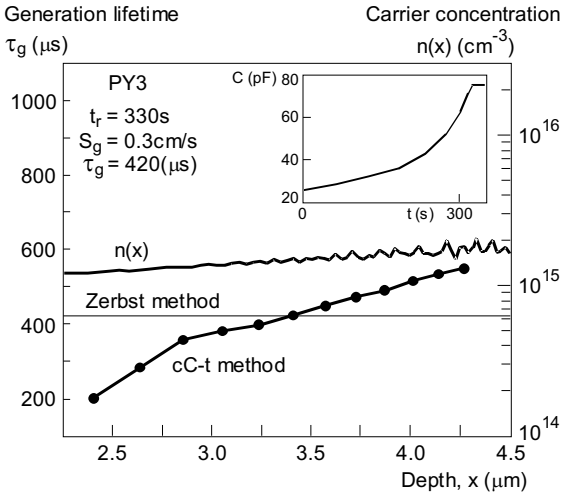

Fig. 5. Depth profile of $\tau_g(x)$ and $n(x)$ with C-t curve (inset) of structure PY3. We can see good agreement between Zerbst C-t and cC-t methods.

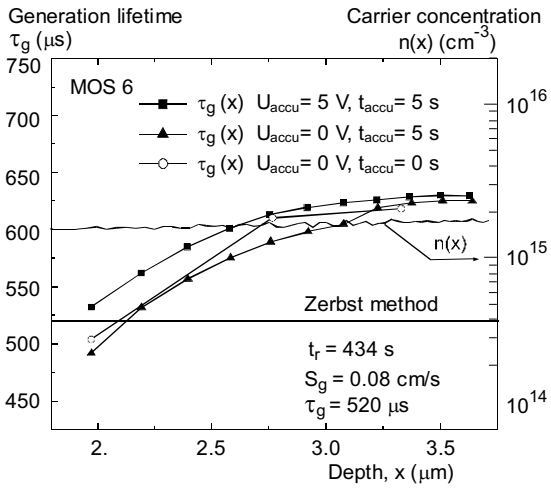

Fig. 6. Depth profile of $\tau_g(x)$ and $n(x)$. Using different mode of driving MOS structure to deep depletion we can obtain identical profile of $\tau_g(x)$.

The size of the voltage increment is calculated using the standard MOS theory. Since the voltage source increments V_G suddenly, the change in the charge in the inversion layer during the pulse can be neglected. Hence, for an n-type substrate it can be shown, using the depletion approximation, that

$$\frac{\mathrm{d}C}{\mathrm{d}V_G} = \frac{\sqrt{\varepsilon_0 K_S q N_d}}{\left(\frac{\varepsilon_0 K_S q N_d}{C_{ox}^2} - 2V_G\right)^{3/2}} = \frac{C_{fix}^3}{\varepsilon_0 K_S q N_d}\,. \qquad (10)$$

When the computer detects that capacitance C has increased above the desired measurement value C_{fix}, it increases the gate voltage sufficiently to drive the MOS-C to C_{fix} by applying the voltage increment $\left(C - C_{fix}\right)/\left(\mathrm{d}\,C/\,\mathrm{d}\,V_G\big|_{V_G=V_{meas}}\right)$ calculated using eqn. (10) evaluated at the initial voltage pulse value V_{meas} (Fig. 2).

The designed program THUNDER for profiling the lifetime changes the value of capacitance in a series of steps (Fig. 3). The resulting gate voltage transients will be a succession of ramps of different slopes. The THUNDER program supports both the standard and the modified technique of data evaluation.

4 EXPERIMENT

For a detailed study of maintaining a constant capacitance and methodology research of cC-t method, samples with different values of the relaxation time t_r and different manufacturing technologies were chosen.

Samples PY 3, MOS 6 and MOS 2 were prepared by epitaxial growth on an n-type substrate. For sample MOS 2, Au contamination was found by deep level spectroscopy. Samples PT 18 and 1A3 were also prepared by epitaxial growth on an n-type substrate, and MOS-C PT 18 had a value of the relaxation time 130 seconds and MOS-C 1A3 had a long relaxation time of 24 minutes.

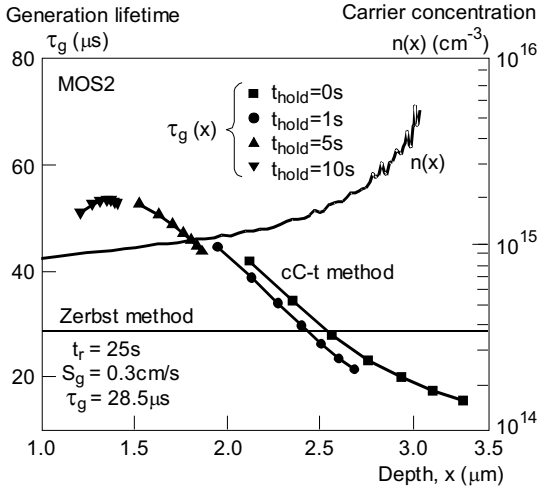

Fig. 7. Depth profile of $\tau_g(x)$ and $n(x)$. By changing value of $t_{hold} < t_r$, we can profile $\tau_g(x)$ more finely.

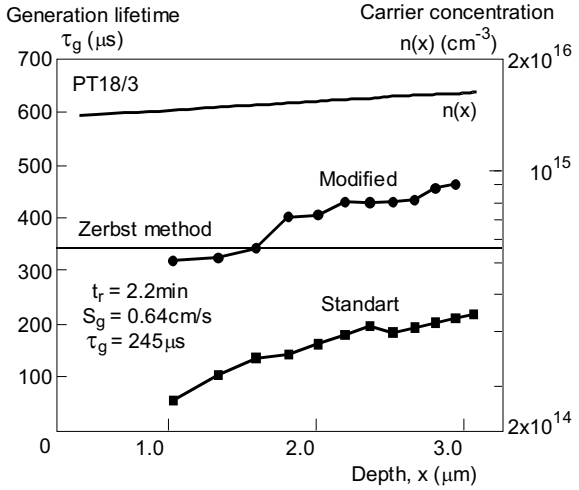

Fig. 8. Depth profile of $\tau_g(x)$ and $n(x)$ of MOS structure with high value of surface generation velocity. Using modified data evaluation technique we cancel out contribution of surface generation

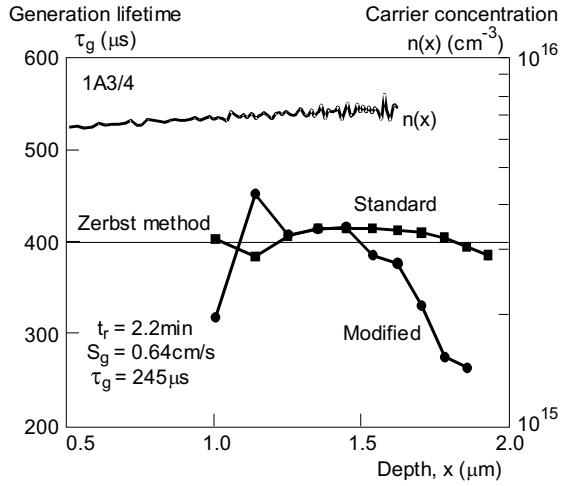

Fig. 9. Depth profile of $\tau_g(x)$ and $n(x)$ of MOS structure with low value of surface generation velocity. We obtain similar value of $\tau_g(x)$ using standard and modified technique, respectively.

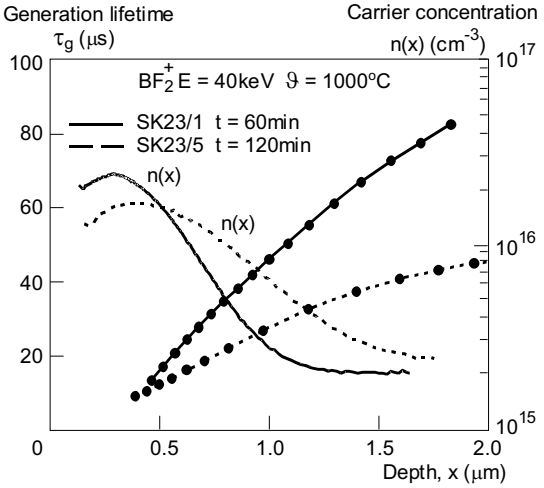

Fig. 10. Depth profile of $\tau_g(x)$ and $n(x)$ of MOS structure with ion-implanted substrate and different annealing times.

Sample SK 23 was prepared by ion-implantation of BF_2^+ into p-type substrate with different annealing times.

Figure 4 shows the resulting gate voltage transients as a succession of ramps of different slopes with very good linearity. For MOS-C PY 3 it can be seen (Fig. 5) that we achieve good agreement with the classical C-t method. The value of the generating lifetime obtained by the C-t method is only an integral value in the depletion region, whereas using the cC-t method we obtain the depth profile of $\tau_g(x)$.

For all measurements we chose the value of $t_{calc} = 5$ s. In time interval $\langle 0, t_{calc} \rangle$ the program does not consider the values of V_{add} for calculation, and the slope is then evaluated from the voltage values accounting $t > t_{calc}$.

In our investigation of the methodology, we observed the effect of the input values V_{accu}, t_{accu} and t_{hold} (Fig. 3) upon the measurement results. Using appropriate input parameters we specified the approach, if the program drives MOS-C to deep-depletion from accumulation, to a zero value of the gate voltage or if it holds MOS-C in deep-depletion during the measurement. The effect of input parameters V_{accu} and t_{accu} is shown in sample MOS 6 (Fig. 6). It can be seen that for different values of this parameters we obtained identical profiles of $\tau_g(x)$. However, in transition from accumulation or zero value of V_G to deep-depletion ($V_{accu} \geq 0$, $t_{accu} \neq 0$), the step of profiling should not be smaller than 0.5 V because this leads to a dispersion of the values of τ_g due to a change of the final inversion capacitance C_∞. In the case of holding the MOS-C in deep-depletion for the entire time of measurement ($t_{accu} = 0$), the overall time is limited by forming of the inversion layer. This procedure is applicable for fast measurement in production.

Next we observed the effect of the parameter t_{hold}. It is the time between driving the MOS-C to deep-depletion by a voltage step, and applying additional voltage V_{add} for maintaining the constant capacitance. During this time relaxation starts of the MOS-C and the width of scr is getting smaller. After t_{hold}, the increase of V_{add} starts to maintain the constant value of scr width. Using an appropriate choice of $t_{hold} < t_r$, we can profile the $\tau_g(x)$ in the subsurface region (Fig. 7) which is closely to the SiO_2–Si interface. We are not able to profile the lifetime so fine using only the voltage step V_G.

As we described in introduction, we can calculate the results using the standard or modified technique. The depth profiles of $\tau_g(x)$ and carrier concentration $n(x)$ of samples PT 18 a 1A3 obtained using both calculation method are shown in Figures 8 and 9.

For MOS-C PT 18, τ_g calculated by the standard technique is lower than that determined by the Zerbst C-t method (Fig. 8). This is due to the high value of the surface generation rate ($S_g = 0.64\,\mathrm{cms}^{-1}$) because this technique does not separate generation from the SiO_2–Si interface and diffusion of minority carriers from the neutral bulk. In contrast, for the sample 1A3 with a low value of the surface generation rate ($S_g = 0.07\,\mathrm{cms}^{-1}$), it can be seen that the surface generation and bulk diffusion terms have been cancelled out by the modified cC-t technique, leaving truly only the effect of the generation lifetime (Fig. 9).

Figure 10 shows the generation lifetime profile in an ion-implanted substrate MOS structure with different annealing times. The τ_g increases with lowering the impurity density as assumed, *eg*, with a decrease of post-implantation defect density. This result confirms a non-homogeneous distribution of electrical active defects in scr for structures with non-homogeneous doping.

5 CONCLUSIONS

We described the design of an automated measurement set-up for performing the cC-t method. The system is fully functional and we achieve good agreement of τ_g with the Zerbst C-t method. Our contribution is mainly in implementation of the measurement set-up, which provides fast measurement of the generation lifetime using computer control. This set-up can be used for fast production testing. We investigated the methodology of cC-t method and found the effect of the input parameters upon measurement results. We investigated the applicability of this method to MOS structures with high values of the surface generation velocity S_g. We measured depth profiles of the generation lifetime for non-homogeneously doped MOS-Cs with different annealing times.

A method based on someone's home-built equipment finds use in some selected research laboratories, but is never fully accepted until commercial equipment is widely available for its use.

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