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A HIGH–INPUT–IMPEDANCE BUFFER WITH MULTIPLE FEEDBACK

Štefan Lányi * — **Marco Pisani** **

The properties of bootstrapped high-input-impedance unity gain buffers have been analysed. It turned out that the input impedance and the noise may attain values much larger than it would correspond to the opamp open-loop gain. Correspondingly, the efficiency of suppression of capacitances connected to the inputs was unexpectedly high, though not of the opamp input capacitance itself. Good agreement of experimental and calculated properties was achieved using a multiple feedback model, taking into account, besides the open-loop differential gain, also the common-mode and power supply gains of the operational amplifier and, independently, the voltage transfer to the supply nodes.

K e y w o r d s: unity gain buffer, bootstrap, multiple feedback, noise, input impedance

1 INTRODUCTION

Signals from high impedance voltage sources or sensors must be frequently amplified to acceptable levels or transformed to lower impedance, allowing further processing. In many cases the circuit connected to the voltage source may introduce errors unless its input impedance is high enough. Let us mention the measurement of cell potentials [1–3], contact potentials [4–5] or inverse-capacitance position transducers [6–8]. At low frequency amplifiers based on electrometric FET-input operational amplifiers may give satisfactory results. In some cases, the requirements on the frequency range cannot be compromised or the input stage affects the result at any frequency. The parasitic capacitance connected to a capacitance displacement sensor [8] would affect the linearity of the $1/C$ *vs* distance dependence. The input capacitance of a low-frequency Scanning Capacitance Microscope, sensing the signal from a probe with sub-femtofarad capacitance [9] directly affects the useful input signal level, the dynamic range and the achievable signal-to-noise ratio.

Experiments with high-input-impedance stages, designed for operation in kHz to MHz-range, have shown that their noise and input impedance may attain unexpectedly high values [10], and the suppression of a capacitance connected to the input may be orders of magnitude more efficient than expected [11]. The aim of the present paper is to explain the causes of the observed properties and to point out the shortcomings of the usual simplified approach to the design of certain opamp-based circuits.

2 DESCRIPTION OF THE CIRCUIT AND EXPERIMENTAL RESULTS

The common way of amplifying the signals from high impedance sources is to connect them to a high-input-impedance stage, usually a unity gain buffer. The input impedance of such a stage is limited at low frequencies by the input resistance of the opamp. With FET- input amplifiers this can be higher than $10^{12}\,\Omega$. Unfortunately, unless the voltage source represents a reasonable dc path to ground or to a constant potential node, dc stability requirements dictate the use of a biasing circuit that necessarily reduces the input impedance. At high frequencies, the input capacitance of the opamp, which is of the order of picofarads, becomes dominant. The negative feedback reduces the effect of the differential input capacitance C_d but not that of the common-mode input capacitance C_c. Thus, the input impedance at high frequencies may become much lower than with an ideal opamp.

The effect of the common-mode input capacitance C_c, which is mostly a capacitance between the inputs and the supply nodes, will diminish if the potential difference between the inputs and the remaining nodes is kept constant. This can be achieved by shielding the opamp and the biasing resistor, and bootstrapping both the shield and the supply nodes. Such solution reduces also the effect of the parasitic capacitance of the biasing resistor (Fig. 1a) and it offers as additional benefits the possibility to increase the output voltage swing [12] and common-mode voltage rejection [13]. The application of bootstrap dictates the gain of the stage to be unity.

The output voltage resulting from the opamp current noise or from the thermal noise of the biasing resistor (*cf*

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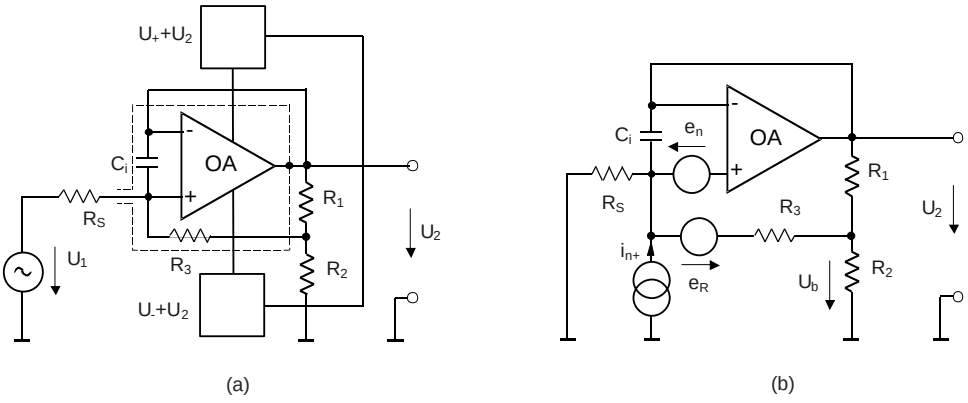

Fig. 1. Buffer with bootstrapped biasing resistor and supply nodes (a), equivalent circuit with relevant noise sources (b).

Fig. 1b), can be calculated using the expression [10]

$$\frac{u_2}{i_N} = \Big[\frac{1}{R_s} + \frac{1}{R_3'} + \frac{1}{A_{ol}(s)}\Big(\frac{1}{R_s} + \frac{1}{R_3} + \frac{1}{jX_i}\Big)\Big]^{-1}, \quad (1)$$

where i_N is either i_n, the opamp noise current, or i_R, the resistor thermal noise current with spectral density $i_R^2 = 4kT\Delta f/R$, $k = 1.38 \times 10^{-23}\,\mathrm{JK}^{-1}$ is the Boltzmann constant, T is temperature and Δf is the frequency range. By A_{ol} is denoted the opamp open-loop gain, R_s the internal resistance of the signal source, $R_3' = R_3(R_1 + R_2)/R_1$ and $X_i = 1/(\omega C_i)$ the opamp input reactance. Voltages and currents related to signal are printed in upper case, whereas those denoting noise are in lower case. With large circuit resistances, the contribution of opamp voltage noise is negligible. The resulting noise voltage is the square root of the sum of squares of individual noise contributions. In the case of R_3 in the range $1\,\mathrm{M\Omega}$ to approximately $100\,\mathrm{G\Omega}$, the resistor noise dominates. The input impedance $Z_i = e_+/I_i$ can be obtained from expressions

$$U_2 = e_+ A_{ol}(s)/[1 + A_{ol}(s)]$$

$$I_i = (U_1 - e_+)/R_s = -(U_b - e_+)/R_3 - (U_2 - e_+)/jX_i\,, \quad (2)$$

where I_i is the input current, U_b the voltage at the common node of R_1 and R_2, assuming R_3 much greater than the parallel combination of R_1 and R_2

$$Z_i = \frac{1 + A_{ol}}{A_{ol}(s)}\Big[\frac{1}{R_3'} + \frac{1}{A_{ol}(s)}\Big(\frac{1}{R_3} + \frac{1}{jX_i}\Big)\Big]^{-1}. \quad (3)$$

If $R_s \to \infty$, *ie* with an open input, the noise transimpedance (1) and the input impedance (3) differ only in the factor $(1 + A_{ol})/A_{ol} \approx 1$.

In the experimentally investigated circuits, the fast FET-input opamp OPA655 (Burr- Brown) has been used [14]. The feedback to the supply nodes was realised by transistor emitter followers. The input impedance was estimated in two different ways. The circuit was connected to a sine wave generator through a large shielded resistor ($10^{11}\,\Omega$) and at a low frequency (1–3 Hz) the output voltage of the voltage divider thus created was measured. In this way, the input resistance was obtained. Then the resistor was replaced by a small calibrated capacitor (1 fF) and the input capacitance was calculated from the frequency dependence of the output voltage. This approach is less convenient if the input resistance is very high ($\sim 1\mathrm{T\Omega}$) since it requires a too large series resistor, for which it is hardly possible to achieve a sufficiently small parasitic capacitance and the measurement has to be performed at extremely low frequencies ($\ll 1$ Hz). The second procedure was based on the similarity of expressions (1) and (3). The frequency dependence of the input impedance was obtained from the noise spectrum, *ie* using the resistor noise as a wide-band signal source. This approach gave reliable results with larger biasing resistors that resulted in a smaller bandwidth. With $R_3 = 1\,\mathrm{M\Omega}$ and $d = (R_1 + R_2)/R_1 \leq 1000$ gain peaking made the estimation of the input capacitance problematic.

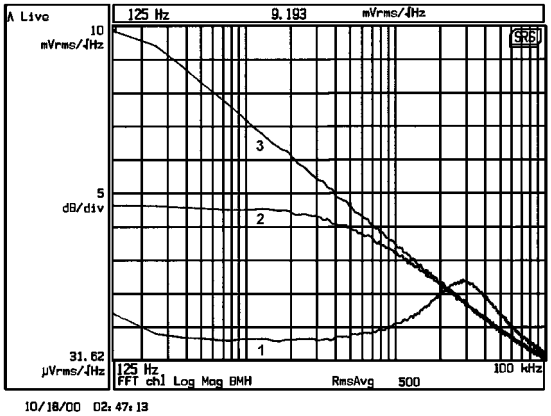

Fig. 2. Measured noise voltage spectral density with $10\,\mathrm{M\Omega}$ biasing resistor and $d = 100$ (1), 1000 (2)and with 100 % feedback (3).

Figure 2 shows the noise voltage spectral density measured by means of a Stanford Research Systems Model SR780 signal analyser. The curves marked 1 and 2 correspond to achieved input resistance 1 and $10\,\mathrm{G\Omega}$, respectively, and the topmost one (100 % of output voltage

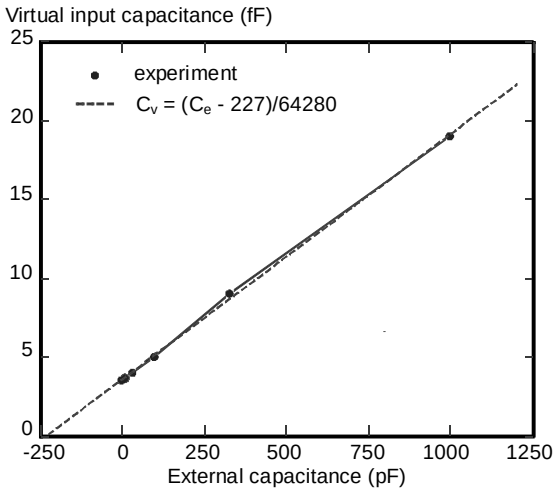

Fig. 3. Measured virtual input capacitance with external capacitors connected to the opamp inputs.

used for bootstrapping the biasing resistor) to more than 350 GΩ. In Fig. 3, the virtual input capacitance obtained with external capacitors connected parallelly to the inputs is shown.

The open loop gain of OPA655 is about 800, with a dominant pole at 300 kHz, thus the expected input resistance ought not to exceed $800\,R_3$. The real noise and input resistance in Fig. 2, with 100 % of the output voltage fed back, correspond to a gain of approximately 49000! A similar value results from the suppression of the input capacitance in Fig. 3.

3 THEORETICAL MODEL

The observed discrepancy can be explained by the fact that the considered unity gain stage is in reality a multiple feedback circuit. The output voltage must depend besides the open loop gain also on the common-mode and power supply rejection ratios of the opamp

$$U_2 = (e_+ - U_2)A_{ol}(s) + \frac{e_+ + U_2}{2}\frac{A_{ol}(s)}{CMRR(s)} + U_2\frac{A_{ol}(s)}{PSRR^-(s)} + U_2\frac{A_{ol}(s)}{PSRR^+(s)}\,.$$

The second term on the right-hand side represents the common-mode error, proportional to the average of the input voltages, the third and fourth ones the effect of imperfect suppression of the positive and negative supply voltage change, assumed to be U_2. After some algebraic manipulation, we find that expressions (1), (2) and (3) remain valid if the open loop gain A_{ol} is substituted by an effective gain

$$A = \frac{A_{ol}(s)\big[1 + \frac{1}{2CMRR(s)}\big]}{1 - A_{ol}(s)\big[\frac{1}{CMRR(s)} + \frac{1}{PSRR^-(s)} + \frac{1}{PSRR^+(s)}\big]}\,.$$

All three additional feedbacks are positive. Using the data sheet values of typical common-mode rejection $CMRR$ and power supply rejection ratios $PSRR^+$ and $PSRR^-$ 3160, 3160 and 1780, respectively, we obtain an effective low-frequency gain of approximately 16000. However, just slightly smaller $PSRR^+ = 3040$ and $PSRR^- = 1712$, or similar combinations, result in gain 49000. These values satisfy the relation [15]

$$1/CMRR(s) + 1/PSRR^-(s) + 1/PSRR^+(s) = 1/A_{ol}(s)$$

even closer than the "typical" data sheet values.

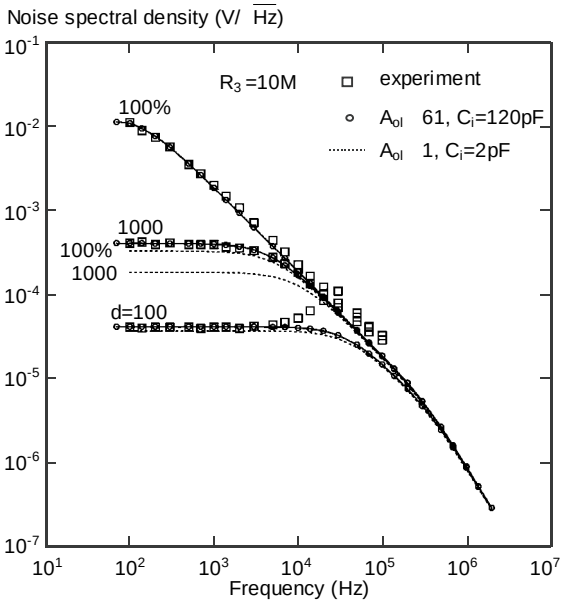

Fig. 4. Simulation of the noise using expression (1) with opamp open loop gain $A_{ol} = 800$ and effective gain $A = 49000$, assuming perfect bootstrap of supply nodes. The output noise spectral density was computed as the square root of sum of squares of opamp current noise, feedback resistor thermal noise and opamp voltage noise, the last one being negligibly small. To approximate the measured data 120 pF input capacitance was needed.

As an example, Fig. 4 shows the approximation of the noise voltage spectral density using effective gains 800 and 49000. The capacitance C_i had to be taken larger than the opamp input capacitance (1.2 pF differential and 1 pF common-mode) plus the stray capacitance of the biasing resistor ($\approx$ 0.1 pF), namely about 120 pF. To understand this at first sight disappointing result, we have to consider that the common-mode input capacitance C_c is between the inputs and the supply nodes. The bootstrap reduces the *ac* voltage on C_c, producing a negative Miller effect. Then neither the open loop gain nor the effective gain but the efficiency of the supply rail bootstrap determines the reduction of the common-mode capacitance. Therefore, this part of the input capacitance

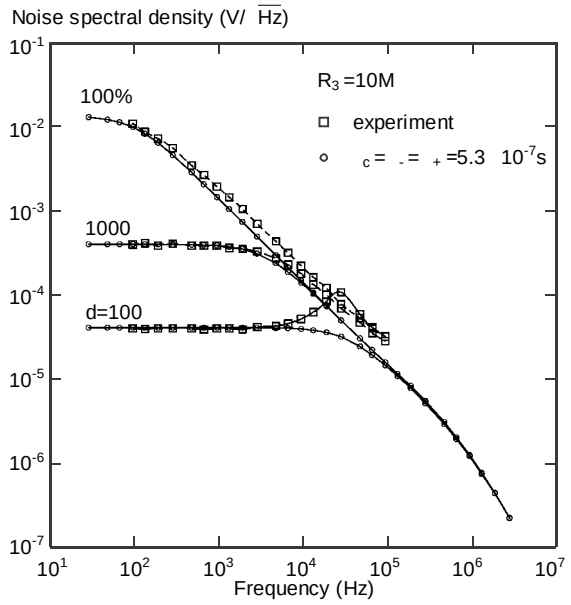

Fig. 5. Simulation of the noise using expression (6) with effective opamp gain ~ 49000 and realistic bootstrap of supply nodes, computed as in Fig. 4. The correct input capacitances and realistic parasitic capacitance of biasing resistor (0.1 pF) were used.

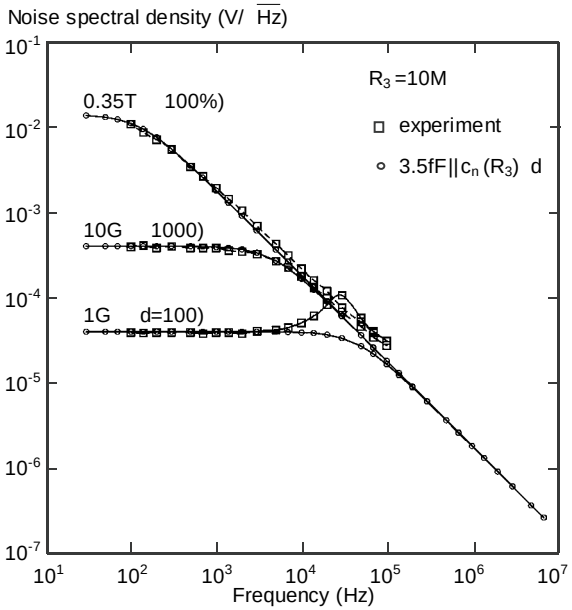

Fig. 6. Measured noise and the noise of equivalent RC network with $R = dR_3$ multiplied by d, the bootstrap ratio of the biasing resistor.

must be considered separately in the formulation of the first Kirchhoff law for the non-inverting input

$$\frac{U_1 - e_+}{R_s} + \frac{U_b - e_+}{R_3} + \frac{U_2 - e_+}{X_d} + \frac{\alpha(s)U_2 - e_+}{jX_c} = 0, \tag{4}$$

where $\alpha \leq 1$ represents the efficiency of voltage transfer from the output to the supply nodes and X_d, X_c are the differential and common-mode input reactances. Using expressions (2) and (4) we can obtain the voltage gain

$$\frac{U_2}{U_1} = \Big[1 + \frac{R_s}{R_3'} + \frac{[1-\alpha(s)]R_s}{jX_c} + \frac{R_s}{A(s)}\Big(\frac{1}{R_s} + \frac{1}{R_3} + \frac{1}{jX_c} + \frac{1}{jX_d}\Big)\Big]^{-1} \tag{5}$$

and analogously, replacing A_{ol} by A in (1) and (3) we get he expression for the noise transimpedance

$$\frac{U_2}{i_N} = \Big[\frac{1}{R_s} + \frac{1}{R_3'} + \frac{1-\alpha(s)}{jX_c} + \frac{1}{A(s)}\Big(\frac{1}{R_s} + \frac{1}{R_3} + \frac{1}{jX_c} + \frac{1}{jX_d}\Big)\Big]^{-1} \tag{6}$$

and the input impedance

$$Z_i = \frac{1+A(s)}{A(s)}\Big[\frac{1}{R_3'} + \frac{1-\alpha(s)}{jX_c} + \frac{1}{A(s)}\Big(\frac{1}{R_3} + \frac{1}{jX_d} + \frac{1}{jX_c}\Big)\Big]^{-1} \tag{7}$$

Expressions (5) and (6) are, except for the input quantity, identical, *ie* the noise gain is 1, as expected for a non-inverting unity gain buffer. In the low frequency limit the impedance is determined by both the biasing resistor and effective gain

$$Z_i = \frac{1+A}{A}\Big(\frac{1}{R_3'} + \frac{1}{AR_3}\Big)^{-1}.$$

Figure 5 shows the simulation of the noise voltage spectral density assuming realistic component parasitic capacitances. Since no manufacturer's specification of the frequency dependence of the rejection ratios is available [16], poles at or close to the dominant pole of the opamp open loop gain frequency response have been assumed. Modification of pole frequencies affects mainly the high frequency part of the plots. In the computation, α corresponding to emitter followers using low-frequency transistors ($\beta = 300$, $f_T = 200$ MHz) was assumed. Figure 6 illustrates the frequency response of the noise of an equivalent RC network (dotted) and a RC network with noise increased similarly as the input impedance, caused by the bootstrap of the biasing resistor.

4 DISCUSSION

It is evident from the analysis that the input impedance can be tailored to specific needs. The input impedance can be increased and the differential input capacitance reduced very efficiently, with the full advantage of the large effective gain. Bootstrapping the biasing resistor allows to use lower resistor values, thus reducing the influence of its

parasitic capacitance on the bandwidth. The suppression of the common-mode input capacitance affects directly the achieved bandwidth. It requires a good bootstrap of the supply rails.

It is important to note that bootstrapping the biasing resistor may significantly increase the noise compared to that which would be achieved with a larger resistor and less or no bootstrap, though as it is evident from expressions (5) and (6), without affecting the signal-to-noise ratio. On the other hand, if the buffer is connected to an impedance small compared to the input impedance, the noise is reduced to a value almost determined by the source impedance. For example, if a ratio of input and source resistances 100 were realised by bootstrapping a biasing resistor $R_3 = R_s$, the noise increase with respect to biasing resistor $R_3 = 100\,R_s$ without bootstrap would be 0.2 dB. For a ratio of 1000, the increase would amount to only 0.043 dB.

Neglecting the parasitic gains affects the effective gain also in less unusual circuits. For example, in a simple buffer it would be about 1070 instead of the open loop gain 800.

5 CONCLUSIONS

The input impedance of a unity gain buffer with a bootstrapped biasing resistor and supply rails may achieve values orders of magnitude larger than it would correspond to the opamp open loop gain. The correct calculation of the properties of the circuit must take into account besides the open loop gain also the opamp common-mode rejection ratio and the power supply rejection ratios. Effective suppression of the common-mode input capacitance requires a possibly perfect bootstrap of the supply rails.

Bootstrapping the biasing resistor increases not only the input impedance but also the current noise, however, without affecting the signal-to-noise ratio. With circuit resistances in the MΩ to approximately 100-GΩ range, dominant is the resistor thermal noise.

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