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IMPROVING THE LINEARITY OF AN ANALOG VOLTAGE–TO–PERIOD CONVERTER

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One type of a simple analog voltage-to-period converter or voltage controlled oscillator (VCO) is modified and its features are analyzed with aim to improve the linearity of its characteristic namely in upper part of working-frequency range. It is shown that reinforced current injection through to overcompensated feedback network improves its performance. Analytical solution of the circuit, allowing effective simulation in order to optimize the converter characteristic, is shown to agree well with the measurement on a fabricated converter.

K e y w o r d s: analog voltage-to-period converter, VCO, overcompensated feedback, linearization, circuit analysis

1 INTRODUCTION

We shall be concerned with a voltage-to-period converter, for circuitry see Fig.2, which may be considered as fairly simplified version of Analog Devices circuits AD-VFC32 or AD650 [1,2]. Operation of this circuit is based on integration of (more or less) square pulses (V_y, in Fig.1) that are forced to change their polarity after the resulting, triangle voltage (V_z) reaches the threshold level of a comparator included in the chain.

If the device input (regulating) DC voltage will influence the height of square pulses, the slope of triangle waveforms (V_z) will be affected accordingly, making the frequency of their polarity change dependent on the input DC level too. In such a kind of circuits in upper part of their operating frequency range one encounters always the same problem. The rise and fall times of pulses are not negligible if compared with their duration. As a consequence, the proportionality of the shorter and shorter periods to regulating DC voltage is not preserved and at higher operating frequencies the characteristic of the converter may become undesirably curved.

An idea, to override this problem by a well defined overshooting of pulses (to be integrated) for appropriately short time, is objective of this paper. The waveforms shown in Fig. 1. were observed in a fabricated converter. Required fast switching (see V_s, in Fig. 1) may cause oscillations appear on V_y and lead to deterioration of the triangle waveform, for detail see Fig.2a. One can get rid of these spikes, by connecting a small capacitance C_2 in parallel to feedback resistor R_2, Fig.2b. However, this may not be the best solution and paradoxically, similar overshooting of V_y as is the first positive pulse in Fig.2a – if controlled – may be eventually beneficial. This could be attained by adding another capacitor C_1 in parallel to R_1 providing $R_1C_1 > R_2C_2$ in order to over-compensate the feedback network. The case when equality $R_1C_1 = R_2C_2$ holds, will be referred to as compensated feedback, while for $R_1C_1 < R_2C_2$ it will be called as under-compensated. Finally, if no capacitors (except the parasitic ones) are included we shall talk about the non-compensated feedback.

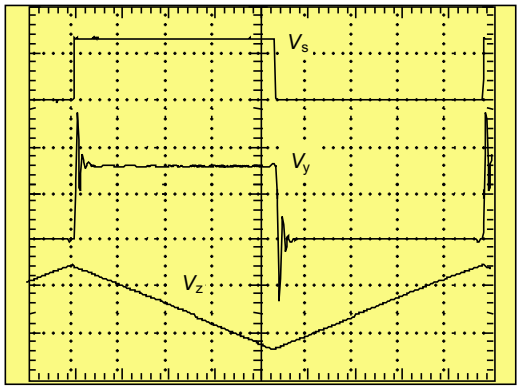

Fig. 1. The waveforms in converter circuit shown in Fig. 3. Up: $V_s(t)$ at non-inverting input of OA2. Middle: $V_y(t)$ output of OA2 to be integrated by OA3. Down: $V_z(t)$ output of integrator(OA3) to processed by comparator OA4

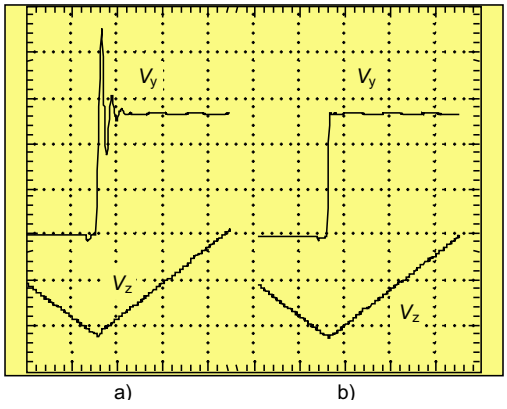

Fig. 2. Details of V_y and V_z waveforms: a) non-compensated feedback (R_1, R_2 without capacitors) — oscillations appear at integrator input, b) under-compensated feedback, $C_1 = 0$, $C_2 = 30$ pF — oscillations are removed.

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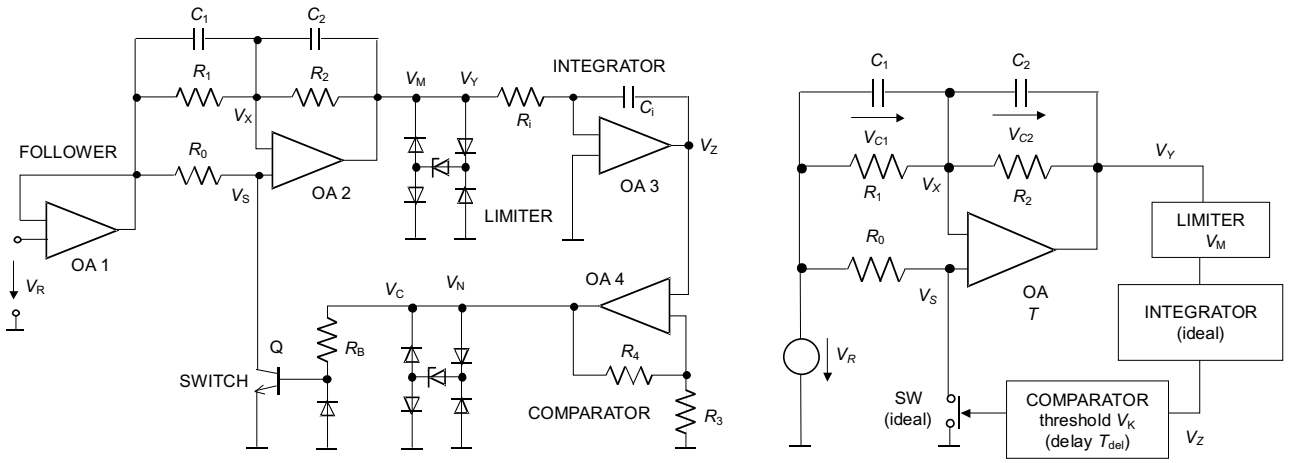

Fig. 3. Detailed circuitry of V/T converter (a) and its simplified scheme (b)

2 CIRCUIT DESCRIPTION

The key parts of converter in Fig. 3a are presented by a simplified circuitry in Fig. 3b. An ideal voltage source V_r stands for the buffer output, follower OA1 providing the regulating voltage $(0 \le V_r \le V_R)$. The switch (SW) is governed by the output voltage (V_c) of comparator OA4 and its stage is supposed to immediately change from *off* to *on* (with *zero* to *infinite* conductance) and vice versa. Nevertheless, a delay $(T_{\rm del})$ is introduced due to a finite reaction time of the comparator and switch itself after the appropriate threshold (V_K) is reached by integrator OA3 output voltage (V_z). There is a limiter $|V_C| \le V_N$ to prevent the comparator from saturation and usual means are taken to speed up the transistor (Q) switching. The integrator is said to be ideal, providing

$$V_z = V_z(t_n) + \frac{1}{T_i}\int_{t_n}^{t_{n+1}} V_y(\xi)d\xi \qquad (1)$$

in a time interval $\langle t_n, t_{n+1}\rangle$ determined by the start and end point of a particular step during the circuit operation. Both limiters (constraining the output voltages to $\pm V_M$ and $\pm V_N$) are linear for $|V_y| \le V_M$ and $|V_c| \le V_N$, and the threshold voltage of the comparator is $V_K = \frac{V_N}{1+R_4/R_3}$. The operational amplifier OA2 from Fig. 1a (depicted as OA in Fig. 1b) is modelled as element with a finite switching-constant T_σ, or appropriate switch-velocity slope $\sigma = \frac{2V_M}{T_\sigma}$, responding by a linear in time change of the output (V_y) when initiated (by change of the SW stage), and residing at the saturation voltage afterwards, until another change of SW stage occurs.

Time (t) is measured in units of T_σ (time norm), and voltages V_r, V_s, V_x, V_y, V_z, V_c and V_K are measured in units of V_M (voltage norm). Thus, the reduced (dimensionless) variables, used throughout this article $\tau = \frac{t}{T_\sigma}$

$$y = \frac{V_y}{V_M}, \quad z = \frac{V_z}{V_M}, \quad c = \frac{V_c}{V_M}, \quad K = \frac{V_K}{V_M}, \qquad (2)$$

can well exceed the unity, while

$$r = \frac{V_r}{V_M}, \quad s = \frac{V_s}{V_M}, \quad x = \frac{V_x}{V_M}, \qquad (3)$$

will always be from interval (0,1). Further we shall introduce

$$k = \frac{R_2}{R_1}, \quad m = \frac{C_1}{C_2}, \qquad (4)$$

and instead of the time constants $T_i = R_iC_i$, $T_1 = R_1C_1$, $T_2 = R_2C_2$, and $T_{\rm del}$ rather

$$\tau_i = \frac{T_i}{T_\sigma}, \quad \lambda\frac{m}{k} = \frac{T_1}{T_\sigma}, \quad \lambda = \frac{T_2}{T_\sigma}, \quad \tau_{\rm del} = \frac{T_{\rm del}}{T_\sigma}, \qquad (5)$$

will be used. A special, the so-called "compensated" case $R_1C_1 = R_2C_2$, is giving $k = m$, and particularly the case with no capacitors present (non-compensated feedback) leads to $\lambda = 0$. The circuit is normally designed to operate with $k = 1$, *ie* with matched resistors R_1, R_2.

In principle, the circuit could be in one of its "stable" stages if not in a transient state in-between. In one of them - let this be denoted as A - the switch (SW) is off, and $s = r$, $x = r$, $y = r$ where $r \le 1$, $z = z_A$, and $V_{C1} = 0$, $V_{C2} = 0$. In the other stable stage (B), the switch is on, and $s = 0$, $x = -\frac{y}{A_0} \cong 0$, $y = -kr$, $z = -z_B$, and $V_{C1} = rV_M$, $V_{C2} = krV_M$ as follows from the anticipated unlimited open-loop gain (A_0) and infinite input resistance of an ideal OA. It is important to stress that this is the case only if enough time is left for all transient currents to fade away. By other words, if the consecutive switching A $\rightarrow$ B and B $\rightarrow$ A are repeated at a relatively slow rate. Nevertheless, the absolute values of z_A, z_B may be different due to a non-symmetry of switching during A $\rightarrow$ B and B $\rightarrow$A transients, respectively even for $k = 1$. And similarly, different delay time $\tau_{\rm del\ A}$ and/or $\tau_{\rm del\ B}$ may be involved depending on the switching to occur.

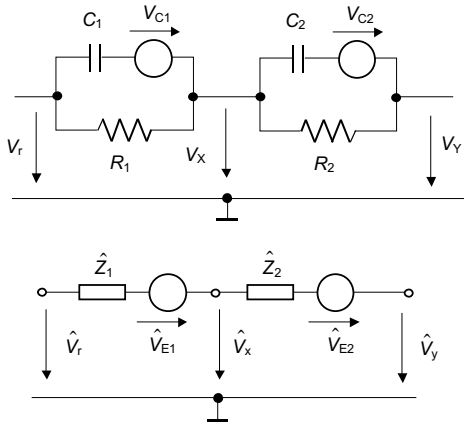

Fig. 4. The equivalent electric circuit

3 CIRCUIT ANALYSIS

Omitting the solutions for possible circuit malfunctions, let us suppose the circuit is working in a periodic duty cycle. Let SW be activated at τ_0 when signal s goes abruptly from value of r to zero and the circuit starts to change from A to B stage. Depending on the operational conditions, from two up to six consecutive intervals (phases) in a period may be distinguished. In any case, let the half-period be denoted as τ_3 (the instant when a change from B to stage A is to occur after signal s has returned from zero back to value of r), and the period of duty cycle (with the same conditions as at τ_0) be τ_6. If less than six intervals will be found effective during a period, we shall talk about zero duration of some of them. In all possible stages, the circuit can be described using an equivalent scheme, shown in Fig. 4, where V_{C1}, V_{C2} will play the role of *initial values* at any instant of time being considered as (a new) starting point.

After Thévenin-to-Norton, and subsequent Norton-to-Tévenin transformation of two-poles in the upper part of Fig. 4, one will get the circuit shown in lower part of figure, and the Laplace transform will yield

$$(\hat{V}_R - \hat{V}_X - \hat{V}_{E1})Y_1 = (\hat{V}_X - \hat{V}_Y - \hat{V}_{E2})Y_2 \qquad (6)$$

where

$$Y_1 = G_1 + pC_1 \quad Y_2 = G_2 + pC_2 \qquad (7)$$

(denoting $G = 1/R$) and

$$\hat{V}_{E1} = V_{C1}\frac{pT_1}{pT_1 + 1}, \quad \hat{V}_{E2} = V_{C2}\frac{pT_2}{pT_2 + 1} \qquad (8)$$

Expressing the initial voltages at capacitors C_1 and C_2 as the differences $V_{C1} = V_r(0) - V_x(0)$ and $V_{C2} = V_x(0) - V_y(0)$, after somewhat tedious manipulations, the back transform taking into account relations between $\hat{V}_x$ and $\hat{V}_y$ will give the desired $V_x(t)$ or $V_y(t)$ if one of these waveforms is prescribed (forced). To find $V_z(t)$ it is then necessary to evaluate integral (1).

In the circuit we are entangled with, many instances could be found depending on the choice of parameters involved but will not be discussed here. Typical signal waveforms with six distinguished intervals (phases) are shown in Fig. 5, and to present this solution we shall introduce abbreviations

$$\alpha = \frac{1+k}{\lambda(1+m)}, \quad \beta = \lambda\frac{m-k}{1+k}, \qquad (9)$$

$$\tau_{\text{down}} = \frac{1}{2}(1 + r + \delta_A), \quad \tau_{\text{up}} = \frac{1}{2}(1 + kr + \delta_B) \qquad (10)$$

Here τ_{down} and τ_{up} are reduced times needed for y to access the value of -1 when starting form $y_0 > 0$, and value +1 when starting from $y_3 < 0$ after the appropriate change of SW condition, Fig. 5.

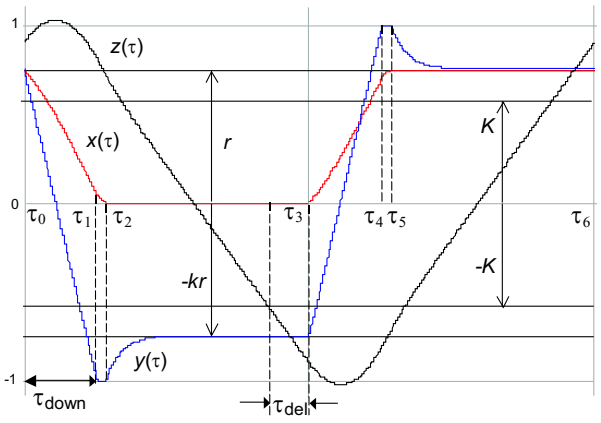

Fig. 5. Waveforms according presented solution with $\tau_i = 1.16$, $\tau_{\text{del}} = 1$, $m = 3$, $k = 1$, $\lambda = 0.182$, $\beta = 0.185$, $\alpha = 2.72$, $K = 0.464$, and $r = 0.75$ leading to: $\tau_1 = \tau_{\text{down}} = 0.88$, $\tau_2 = 0.99$ and $\tau_3 = 2.23$

SOLUTIONS

At a higher switching rates, at the beginning (τ_0) as well as in the half of period (τ_3), signals $y_0 = y(\tau_0)$ and $y_3 = y(\tau_3)$ may not match expected (stable) values of r and $-kr$ (as would be the case at a slower switching rate). Therefore differences $y_0 - r$ and/or $y_3 + kr$ are appearing in appropriate terms given below.

First interval $\tau_0 < \tau < \tau_1$, $\xi = \tau - \tau_0$,

Without a loss of generality one can put $\tau_0 = 0$. This interval (starting when the SW goes *on*) as the first phase of the transient always exists and output y is here forced to linearly decrees from value y_0 downward the limit -1 at a rate determined by parameter σ

$$\begin{aligned}(\xi) &= r - \frac{2}{1+k}\left\{\xi - (\beta + \frac{y_0 - r}{2})(1 - e^{-\alpha\xi})\right\} + \\ &\quad + (x_0 - r)e^{-\alpha\xi} \\ y(\xi) &= y_0 - 2\xi \\ z(\xi) &= z_0 + \frac{\xi}{\tau_i}(y_0 - \xi)\end{aligned} \qquad (11)$$

Values of x_0, y_0 and z_0 must obey periodicity condition. This phase of transient will end (at τ_1) due to one of three possible reasons:

(i) signal y at integrator input has reached the limit -1, *ie* further descent is unfeasible and the second phase will start (possibly followed by the third one)

(ii) signal x at inverting input of OA has reached its stable (zero) value, and the output y will tend to its stable value $-kr$ (the second interval of a "zero duration" will be followed by the third one).

(iii) signal z at integrator output has reached the threshold $-K_A$ and after a reaction delay time ($\tau_{\text{del A}}$) immediate back switching (*ie* B $\rightarrow$ A) will take place (both the second and third interval were of zero duration).

The characteristic reduced times of above cases are given:

(i) explicitly by $\xi_{y1} \equiv \tau_{\text{down}}$

(ii) implicitly by relation $x(\xi_{x1}) = 0$.

(iii) explicitly by $\xi_{z1} = \tau_{\text{del A}} + \frac{y_0}{2}\left[1 + \sqrt{1 + \frac{4\tau_i(z_0+K_A)}{y_0^2}}\right]$

The first interval will end at $\tau_1 = \tau_0 + \xi_1$ where

$$\xi_1 = \inf\{\xi_{x1}, \xi_{y1}, \xi_{z1}\} \tag{12}$$

This is, more or less, governed by value of m. Great m leads to (ii), small m to (iii) while a great m and small τ_i lead to (i).

Second interval $\tau_1 < \tau < \tau_2,\ \xi = \tau - \tau_1$

This will exist only if $\tau_1 = \tau_0 + \tau_{\text{down}}$ *ie* if signal y at integrator input has reached the limit -1, to be kept at during the whole interval. Values of x_1, z_1 are determined from previous interval.

$$\begin{aligned} x(\xi) &= x_1 e^{-\alpha\xi} - \frac{1-kr}{1+k}\left(1 - e^{-\alpha\xi}\right) \\ y(\xi) &= -1 \\ z(\xi) &= z_1 - \frac{\xi}{\tau_i} \end{aligned} \tag{13}$$

The second phase of transient will end if:

(i) signal x at inverting input of OA has reached zero (stable value) and output y is to begin decrease towards its stable level $-kr$ (during the third phase)

(ii) signal z at integrator output has reached the threshold $-K_A$ and after reaction delay $\tau_{\text{del A}}$ the back switching (B $\rightarrow$ A) will take place (without developing the third phase).

The appropriate reduced times are given

(i) explicitly by $\xi_{x2} = \frac{1}{\alpha}\ln(1 + x_1\frac{1+k}{1-kr})$,

(ii) explicitly by $\xi_{z2} = \tau_{\text{del A}} + \tau_i(z_1 + K_A)$.

The second step, if exists, will end at $\tau_2 = \tau_1 + \xi_2$ where

$$\xi_2 = \inf\{\xi_{x2}, \xi_{z2}\} \tag{14}$$

otherwise $\tau_2 = \tau_1$.

Third interval $\tau_2 < \tau < \tau_3,\ \xi = \tau - \tau_2$

This is where x is all the time forced to be zero. Values of y_2, z_2 are determined from previous interval.

$$\begin{aligned} x(\xi) &= 0 \\ y(\xi) &= (y_2 + kr)\, e^{-\xi/\lambda} - kr \\ z(\xi) &= z_2 + \frac{1}{\tau_i}\left[\lambda(y_2 + kr)(1 - e^{-\xi/\lambda}) - kr\xi\right] \end{aligned} \tag{15}$$

The third phase of transient will end only by the back–switching (B $\rightarrow$ A) passing a reaction delay $\tau_{\text{del A}}$ after signal z at the integrator output has reached threshold $-K_A$. This will occur at $\tau_3 = \tau_0 + \tau_{\text{del A}} + \xi_{z3}$, with implicitly given $z(\xi_{z3}) = -K$.

Further intervals

Fourth interval: $\tau_3 < \tau < \tau_4,\ \xi = \tau - \tau_3$. This interval is essentially the same as the first, except the output y is forced to linearly rise from y_3 up to value +1, at a rate being given by σ

$$\begin{aligned} x(\xi) &= \frac{2}{1+k}\left\{\xi - (\beta - \frac{y_3 + kr}{2})(1 - e^{-\alpha\xi})\right\} \\ y(\xi) &= y_3 + 2\xi \\ z(\xi) &= z_3 + \frac{\xi}{\tau_i}(y_0 + \xi) \end{aligned} \tag{16}$$

Values of x_3, y_3 and z_3 must be determined from the previous interval. This phase of the transient will end (at τ_4) due to one of the three possible reasons:

(i) signal y at integrator input has reached the limit +1, *ie* further increase is not possible (the fifth phase will start which may be followed by the sixth one)

(ii) signal x at inverting input of OA has reached its stable value r, and the output y will tend to the same level. (the fifth interval of a "zero duration" will be followed by the sixth one).

(iii) signal z at integrator output has reached the threshold $+K_B$ and after reaction delay $\tau_{\text{del B}}$ again switching A $\rightarrow$ B will take place (both the fifth and sixth intervals will be of zero duration).

The fifth and the sixth intervals are determined in an analogous way to the second and third ones, therefore only appropriate equations are given below without further comment.

Fifth interval: $\tau_4 < \tau < \tau_5,\ \xi = \tau - \tau_4$.

$$\begin{aligned} x(\xi) &= \frac{1+kr}{1+k}\left(1 - e^{-\alpha\xi}\right) + x_4 e^{-\alpha\xi} \\ y(\xi) &= 1 \\ z(\xi) &= z_4 + \frac{\xi}{\tau_i} \end{aligned} \tag{17}$$

Sixth interval: $\tau_5 < \tau < \tau_6,\ \xi = \tau - \tau_5\,.$

$$\begin{aligned} x(\xi) &= r \\ y(\xi) &= (y_5 + kr)\, e^{-\xi/\lambda} - kr \\ z(\xi) &= z_5 + \frac{1}{\tau_i}\left[\lambda(y_5 - r)(1 - e^{-\xi/\lambda}) + r\xi\right] \end{aligned} \tag{18}$$

The periodicity conditions are $z_0 = z(\tau_6)$, $y_0 = y(\tau_6)$ and there is a discontinuity $x_6(\tau_6-) = r$, while $x_0(\tau_0+) = 0$, since SW was anticipated (although with some delay) to operate at an unlimited speed.

4 SIMULATION AND OPTIMIZATION

Without giving details, the results of simulations (calculations based on above given solutions) will be presented. These are more or less related to a fabricated converter (for construction particulars see Tab.1) in order to compare its evaluated and measured features.

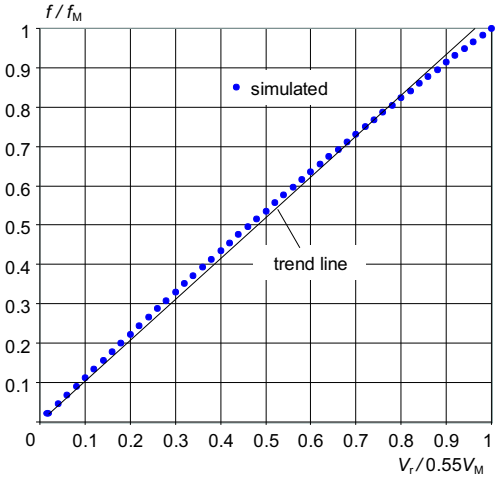

Fig. 6. Converter characteristic without capacitors C_1, C_2, non-compensated case ($m = 1$, $\lambda = 0$) for DC input voltage V_r from interval 0 to $0.55\,V_M$ and with comparation threshold $K = 0.5$. Frequency is reduced to values $f_M = f(0.55V_M)$. The trend line is un-biased, *ie* with a forced zero intercept.

In Fig. 6 the converter characteristic $f(U)$, where $f = 1/T$, is shown for a case with no means taken to improve its performance *ie* without capacitors C_1, C_2 (non-compensated case). Typical values were used for delay $\tau_{\rm del} = 1$, comparation threshold $K = 0.5$, integration constant $\tau_i = 10$, and input control voltage range $0 < r < r_{\max}$, (with $r_{\max} = 0.55$) in a symmetrical regime $k = 1$.

To assess the linearity of converter characteristic let us introduce an *ad hoc* error parameter: $e = 10^5(1 - \rho)$, where ρ is the linear regression coefficient. This, as a measure of relative improvement, will better reflect even a smaller difference than ρ, itself being close to unity for a class of linear-line like curves. Here we shall use two types of a trend-line to approximate the converter characteristic. With forced zero intercept (error e_0) and without it *ie* using an biased line (error e_1). For the characteristic in Fig. 6, the actual value is $e_0 \approx 165$.

The error, we are concerned with, is essentially caused by finite switching times and the prolongation of working period will reduce it. This can be achieved by a higher comparation threshold (K) and/or integration constant (τ_i), however both may lead to an undesirable lowering of the output frequency. How this works at changing K values (while keeping integration constant $\tau_i = 10$) is shown in Fig. 7. Contrary, in Fig. 8 are reflected the changes of integration constant τ_i at a fixed value of $K = 0.5$.

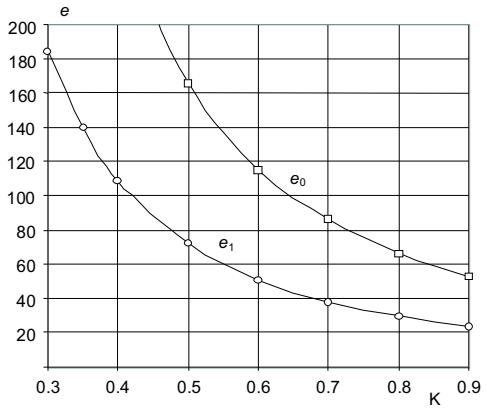

Fig. 7. Influence of comparation threshold K on linearity errors e_0, e_1 with fixed integration constant $\tau_i = 10$

For instance, in case of the fabricated converter with time norm $T_\sigma = 1.8\,\mu$s, a couple of parameters $\tau_i = 20$, $K = 0.7$ would give output frequency in interval up to $f_M \approx 5$ kHz, with errors $e_0 = 22$ and $e_1 = 10$. Nevertheless, considering dynamic input range at least 1:10, means in such a case to accept 500 Hz as the low frequency limit.

Another way how to reduce the errors — as here proposed, is to use an over-compensated feedback with properly adjusted C_1 and C_2. To optimize given circuit is a multi-parameter problem, but for most of parameters fixed, one could find some solutions varying

Table 1. Construction particulars, values of elements in circuit fabricated according to Fig. 3

R_1	R_2	R_0	R_i	R_3	R_4	R_4	C_i	C_1	C_2	OA1-OA4	Q
46.43kΩ	46.31kΩ	390Ω	8.16kΩ	5.1kΩ	6.81kΩ	2.2 kΩ	2.25 nF	*220pF	*40pF	1/4 B084D	KC509

9 × diode KA261, 2 × Zener diodes 7.2 V and 7.8 V for limiters V_M and V_N, see [3] for diodes and transistor KC509, [4] for B084D
* typical (near optimal) parameters, these values were however varied during measurements and simulations.

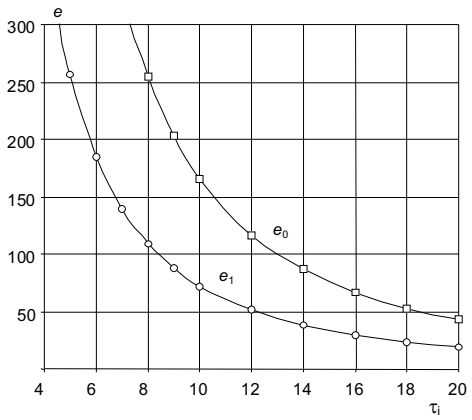

Fig. 8. Influence of integration constant τ_i on linearity errors e_0, e_1 with constant comparation threshold $K = 0.5$.

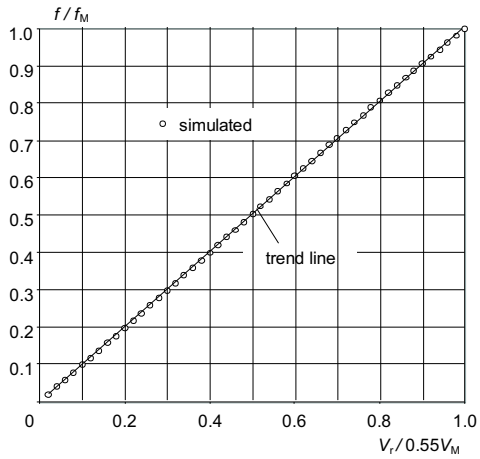

Fig. 9. Converter characteristic with capacitors C_1, C_2 ($m = 3.2$, $\lambda = 1.85$) for DC Input voltage V_r from interval 0 to $0.55V_M$ and with comparation threshold $K = 0.7$ and integration constant $\tau_i = 10$. Frequency is reduced to values $f_M = f(0.55V_M)$. The trend line is un-biased, *ie* with a forced zero intercept

$m = C_1/C_2$, $\lambda = T_2/T_\sigma$ and $K = V_C/V_M$. The best solution: $m = 3.2$, $\lambda = 1.85$, so far found for: $k = 1$, $K = 0.7$, $\tau_i = 10$, $\tau_{\text{del}} = 1$, is in Fig. 9, giving $e_0 = 6.5$ and $e_1 = 3.5$ and $f_M \approx 11$ kHz, provided $T_\sigma = 1.8\,\mu$s. Local, relative errors for this case are presented in Fig. 10. Each curve shows error as a fraction of the deviation from a straight line to the full scale for three different approximations: (i) simple $y = x$, (ii) un-biased, or zero intercept $y = ax$ and (iii) biased $y = ax - b$. Here $y = [(f/f_M)_{\text{approximated}} - (f/f_M)_{\text{simulated}}] \times 100$, $x = V_r/(0.55V_M)$ and approximations, except one referred to as *simple*, are the least square regression lines.

Since τ_i is reduced to T_σ ($\approx 1.8\,\mu$s in Fig. 9 and Fig. 10) – a value that corresponds to the fabricated converter with a relatively slow, and cheaper B084D type OpAmp, building the same network with, say, 20-times faster elements would lead to $\tau_i = 200$. For this case and the same comparation threshold $K = 0.7$, optimal values were found $m = 2.6$ and $\lambda = 2.1$ with practically equal $e_0 = 0.005$ and $e_1 = 0.005$. As illustrated in Fig. 11, a substantial improvement could be thus achieved at the same maximal output frequency (about 10 kHz). In case of equally fast but un-compensated circuit ($m = 1$, $\lambda = 0$) the error would be still about $\pm 0.1r\%$. Although 10 times smaller than that in Fig. 12, the declination from the ideal straight line in this case would be of the same nature.

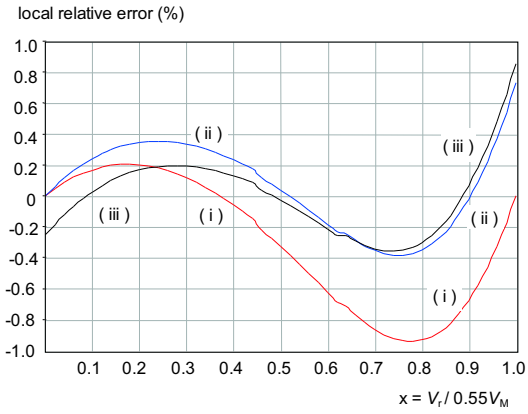

Fig. 10. Case of over-compensated feedback with capacitors $m = 3.2$, $\lambda = 1.85$ and $K = 0.7$, $\tau_i = 10$. Local relative errors of three different approximations: (i) simple $y = x$, (ii) un-biased, or zero intercept $y = 1.00692x$ and (iii) biased $y = 1.01050x - 0.00241$

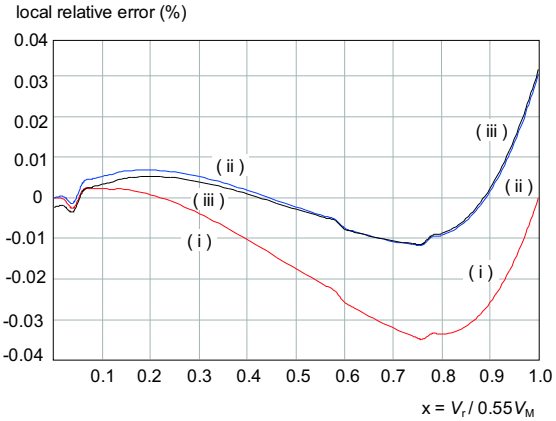

Fig. 11. Case of over-compensated feedback with capacitors $m = 2.6$, $\lambda = 2.1$ and $K = 0.7$, $\tau_i = 200$. Local relative errors of three different approximations: (i) simple $y = x$, (ii) un-biased, or zero intercept $y = 1.00033x$ and (iii) biased $y = 1.00029x - 0.00003$

5 EXPERIMENTAL VERIFICATION

On a fabricated sample of converter build according to Fig. 3a, with elements given in Tab.1, several measurements were performed in order to verify the presented theory. Firstly, the waveforms were compared (Fig. 13a and b) as captured by a digital storage oscillograph - dotted lines, and evaluated using equations (11) through (18) -solid lines. A good agreement of the superimposed shorter injection pulses (a) as well as those with duration almost equal to the half-period (b) is obvious. Not only what concerns their shape, also the (slightly different) duration is reasonable in virtue of the simplifications made.

As the measurements revealed, $x(\tau)$ did not approach the zero value as smoothly as in Fig. 5. Again, over-shots were observed (not shown here) also of $x(\tau)$ to negative values, and as a consequence a faster return of $y(\tau)$ from -1 to value $-kr$ as predicted by $e^{-\lambda}$ term occurred. This could be somewhat better seen in Fig 13b, where also the oscillations are likely to loom. The behaviour of OA should be modelled in a more realistic manner (as a frequency dependent element) to account for these oscillations not only emerging as in Fig.13, but also markedly appearing in Fig.1 and Fig. 2. Comparison in Fig. 14, where markers represent the measured and lines simulated (evaluation) data shows also quite a good agreement. Recommendable input voltage interval for fabricated converter can be 0.5 (or less) to 5 V what corresponds to parameter $r \in (0.055, 0.55)$.

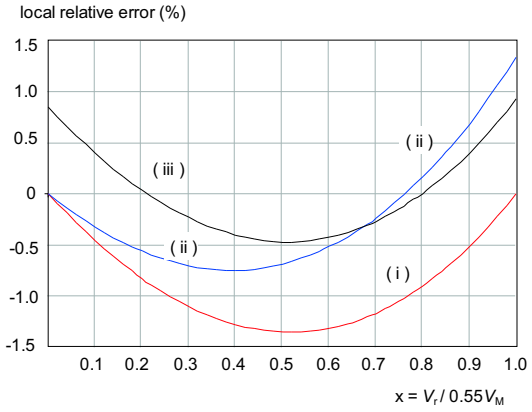

Fig. 12. Case without capacitors $m = 1$, $\lambda = 0$ and $K = 0.7$, $\tau_i = 20$. Local relative errors of three different approximations: (i) simple $y = x$, (ii) un-biased, or zero intercept $y = 1.00313x$ and (iii) biased $y = 1.00517x - 0.00137$

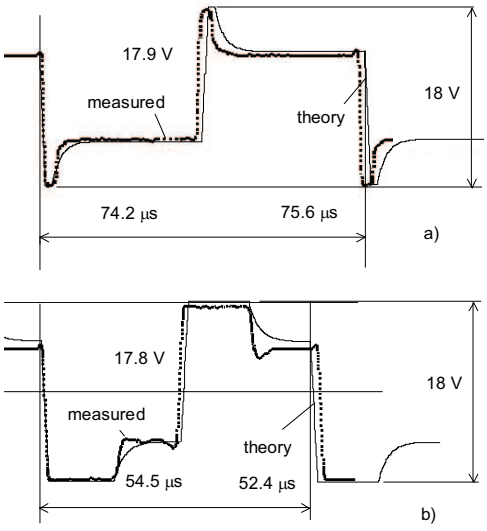

Fig. 13. The waveforms captured by a digital storage oscillograph -dotted lines, and evaluated using equations (11) through (18) - solid lines: a) $C_1 = 170$ pF, $r = 0.45$, b) $C_1 = 430$ pF, $r = 0.55$. Peak-to-peak voltages are $2 \times V_M$.

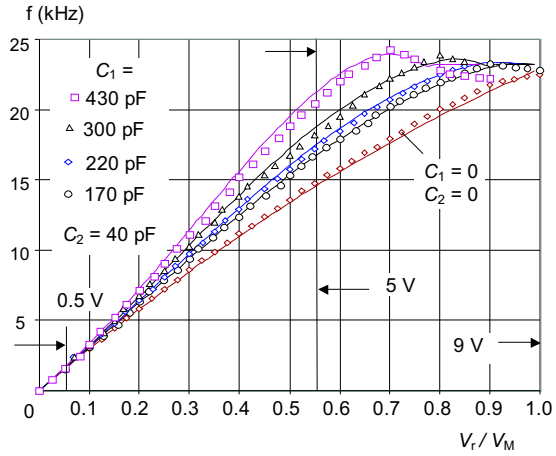

Fig. 14. Comparison of the simulated (markers) and the measured (solid lines) data. The parameters are values of capacitance $C_1 = 430, 300, 220, 170$ pF used to compensate the feedback while $C_1 = 40$ pF. In case with no compensation $C_1 = 0$, $C_2 = 0$. Recommended operation range of the input voltage 0.5 to 5V is indicated by vertical lines.

6 CONCLUSIONS

It has been demonstrated that in converter with a proposed modification of the circuitry combinations of C_1, C_2 could be found suppressing the linearity error. The characteristic of analyzed converter, depending on the feedback compensation, may change its shape to a combined convex-concave type. In virtue of a good agreement between the measurements and numerical simulation, predictions of the resulting changes in the error distribution around zero value with a properly over-compensated feedback could hopefully be reliable.

Acknowledgements

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