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ACCURATE DYNAMIC I_{DD} TESTING AND LOCALIZATION OF DEFECTIVE PARTS IN MIXED–SIGNAL CIRCUITS

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The dynamic supply current testing based on the measurement of voltage drop across a parasitic resistance of the supply voltage metal routing is presented. Auto-zero technique for voltage comparator offset cancelation, which provides very accurate and sensitive low voltage drop measurement across the sensing resistor is proposed. Therefore, the proposed sensor might be used as a current monitor for dynamic current testing of mixed-signal circuits without any additional element necessarily connected in series with the power supply line. In the proposed defect localization methodology, the mixed-signal chip is split into smaller blocks and each block is tested independently. Then the results are evaluated in the common control part, which provides the information about a defective part and shifts this data to a serial data output pin. Therefore, with only one additional pin we may exactly localize the defective part of the integrated system. A USB (universal serial bus) high side power distribution switch was used as an experimental mixed-signal device under test (DUT). The proposed current monitor together with the localization technique was implemented into a circuit under test and the whole experimental chip was designed in a standard 0.35 μm CMOS technology. Finally, the feasibility and efficiency of the proposed test and localization methodology were evaluated and the obtained results are presented.

K e y w o r d s: built-in current sensor, I_{DD} testing, mixed-signal circuits, auto-zero technique, low offset comparator, defect localization

1 INTRODUCTION

In the last two decades, the supply current monitoring (I_{DD} testing) has been used to supplement the conventional logic testing for many systems that require high quality test [1-8]. I_{DD} testing detects an abnormally increased or decreased supply current, caused by a fault present, flowing into the device under test. In order to obtain high-speed and high-resolution I_{DD} testing, the built-in I_{DD} testing (a current monitor integrated together with the DUT) has been proposed. Most of built-in current sensors detect an abnormal current by sensing a voltage drop across a resistance element [9-13]. Figure 1 shows a principal block diagram of a common I_{DD} sensor arrangement. In this structure, the supply current is transformed to voltage using the resistive sensing element. This voltage is then compared with an external reference voltage by a voltage comparator. The resistive element is usually implemented as a MOS transistor or a combination of a MOS transistor and a diode. In order to obtain high sensitivity to the abnormal defective current, the sensing element must have a high resistance that, on the other hand, causes undesired degradation of the DUT supply voltage.

Thus, for low voltage circuits, it is very important that the supply voltage degradation caused by the current sensor is minimized. Therefore, a piece of metal wire, connecting the supply pad with the DUT core, is used as the resistive element in some current monitors [2], [9–10]. This topology achieves a rather small voltage drop across the sensing element (in order of few mV). Thus, a simple voltage comparator cannot be used as the evaluating circuit (Fig. 1) due to its high input voltage offset (in order of tens mV) of the input differential pair in a CMOS technology.

Therefore, auto-zero stabilization is utilized in the current monitor proposed in this paper as a smart and efficient solution for reduction of the voltage comparator input offset. It also helps to compensate any other ineligible effects such as the offset drift (caused by temperature variations, ageing, power supply deviations, mechanical stress, *etc*), and provides the current sensing with high accuracy. Some other advantages of auto-zero structure include the possibility to feature a high open loop gain and a high power supply rejection ratio. CMOS technology is suitable for implementation of such a design, due to its analog switch capabilities and low power feature.

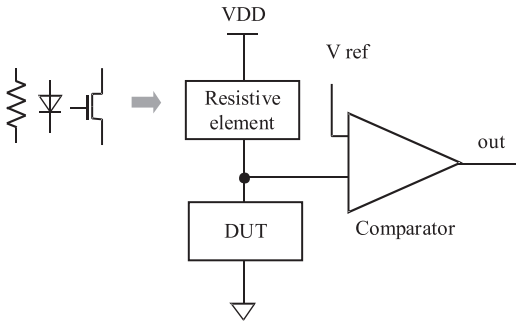

Fig. 1. Common topology of a built-in current sensor

During last couple of years, we have worked on different approaches to on-chip current testing. The more complex design, proposed in [14], describes the current conveyor architecture, which is used to convey the supply current into a threshold detector distinguishing whether the current value is nominal or defective. Furthermore, an

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off-chip supply current sensing and evaluating method for analog circuits using artificial neural networks was proposed in [15–16].

In this paper, we propose a simple supply current sensor using an auto-zero compensated voltage comparator, which compares the supply current value measured on a parasitic resistance of VDD line to the reference voltage. This approach offers very accurate and sensitive measurement of small currents (Tab. 1). The proposed circuit has been designed in a standard $0.35\,\mu$m CMOS technology together with circuit for defective parts localization and implemented into an experimental test vehicle: a USB high side power distribution switch.

2 DESIGN OF THE CURRENT SENSOR

The main task of any current-based test method is sensing the current, which is drawn by the DUT using a sensing element with a minimal resistance in order to reduce the undesired power supply degradation. Therefore, we use a certain small parasitic resistance of a metal layer used in every chip to connect the supply voltage pad to the circuit core as shown in Fig. 2. This solution has no substantial influence on the DUT performance since there is no considerable voltage drop across the current sensor. To achieve low resistance of the sensing resistor the highest layer of metallization with the smallest sheet resistance is used. Since the AMS $0.35\,\mu$m CMOS process, used to design the sensor, is three metal layer technology, we employed the third metal layer (with sheet resistance of $50\,\mathrm{m\Omega/\square}$) to implement the sensing resistor. Thus, if we consider an acceptable serial resistance of $1\,\Omega$ to sense the current, this implies the metal line of twenty squares. This value depends on the current range expected to be measured. Since we try to minimize a voltage drop on this resistive element, the value of the sensing resistance is kept as low as possible.

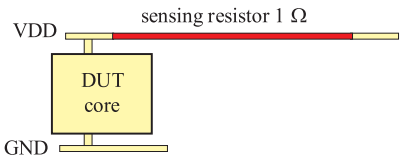

Fig. 2. Parasitic resistor as a sensing element

There is a very small voltage drop V_{do} created by small supply currents from the range of hundreds of μA to tenths of mA across this small serial resistance. In a standard CMOS technology, there is a problem to guarantee low input offset voltage in operational amplifiers. Additionally, both the offset magnitude and its polarity are unpredictable. Since the magnitude of input voltage offset in CMOS technology may achieve hundreds of μV, it is necessary to use an offset compensation technique to reduce the input voltage offset, especially in high accuracy low-voltage applications. Generally, there are more effects influencing the amplifier behavior closed to DC area, such as:

- Input offset voltage — mainly due to the process variations and lithographic errors
- Offset drift — due to temperature changes, ageing, and mechanical stress (time varying offset)
- Flicker $(1/f)$ noise — varies inversely with transistor area

In our work, we use the auto-zero technique as a dynamic approach to input offset cancellation [17, 18]. The main advantage of the selected approach is that this technique reduces also the flicker noise and the offset drift. Therefore, the proposed solution is designed for very sensitive current measurement with high accuracy.

2.1 Auto-Zero Technique

The simple auto-zero topology is shown in Fig. 3, where the voltage comparator with voltage gain A_V has its input offset voltage V_{os}. The problem with offset is that neither its value nor polarity can be predicted because it comparator input offset is the random phenomena. Thus, the signs plus and minus inside the voltage offset symbol mean that no particular offset polarity is considered.

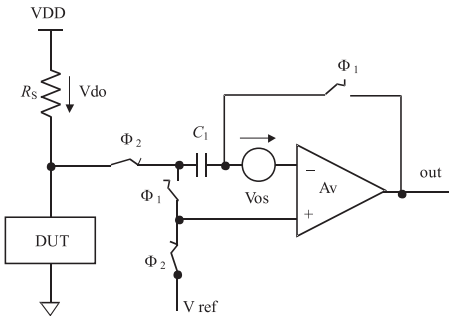

Fig. 3. Current sensor based on Auto-Zero comparator

If the switches Φ_1 are turned on, then the comparator is in unity-gain negative feedback loop configuration. This mode is called the offset cancellation phase. Then, the output voltage is expressed by the following equation:

$$V_{out} = -\frac{A_v}{A_v + 1} V_{os} \cong -V_{os}\,. \tag{1}$$

Thus, the offset voltage V_{os} is stored on the capacitor C_1 with the opposite polarity, and in the next phase, when switches Φ_1 are turned off and switches Φ_2 are turned on, the voltage previously stored in C_1 is now in series with the regular offset voltage at the comparator input and they compensate each other. Problem with this simple topology for offset cancellation is that switching the switch Φ_2 at the comparator input disturbs the comparator output signal. Hence, the undesired signal pulses are observed at the comparator output while the input switch Φ_2 is turned off, as shown in Fig. 4 (lower curve). Consequently, the current sensor might exhibit false defect detection results.

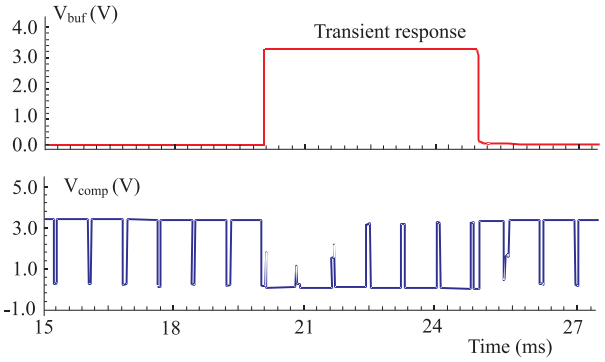

Fig. 4. Auto-Zero technique influence on the comparator output signal

Therefore, additional switch Φ_2 and capacitance C_2 are inserted at the output of the compensated comparator, as depicted in Fig. 5, which eliminates the false defective supply current detection. Thus, when the switches Φ_2 at the input are turned off, then the comparator output is disconnected by the output switch Φ_2 (controlled by the same clock signal as Φ_2 switches at the comparator input) and the previous state of the output is stored on the capacitance C_2. Additionally, an output buffer for minimal loading of this switch and capacitance C_2 is embedded in the comparator output circuitry (Fig. 5). A simple invertor stage has been used as the buffer since there are only two logic values of the output signal. As a result, the current sensor output signal is free of the undesired pulses due to working cycles of Φ_2 input switches (Fig. 4, upper curve).

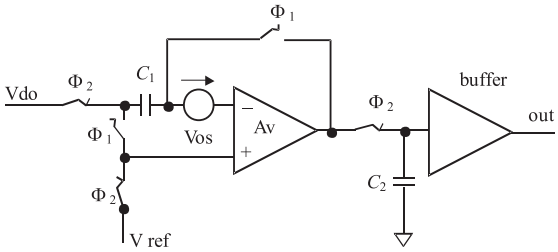

Fig. 5. The proposed current sensor with elimination of the false defect detection

The proposed current monitor distinguishes between two states of the DUT, based on a threshold nominal value of the supply current represented by the reference voltage V_{ref}. If the current flowing through the serial resistor R_S produces a voltage drop V_{do} higher then the reference voltage V_{ref}, then the output is in its high state. This indicates an elevated supply current value representing a defective DUT. Low state of the current sensor output represents a nominal supply current expected in the fault-free state of the DUT.

2.2 Non-overlapping clock

Switches Φ_1 and Φ_2, realized by NMOS transistors are controlled by two clock signals. There is a special timing requirement for these two clock signals due to the fact that the switches Φ_1 and Φ_2 are not supposed to be turned on simultaneously. Therefore, we designed a simple circuit to generate two non-overlapping clocks, as depicted in Fig. 6. Specific design of the invertors allows realization of the clock signals using only minimum number of circuit components.

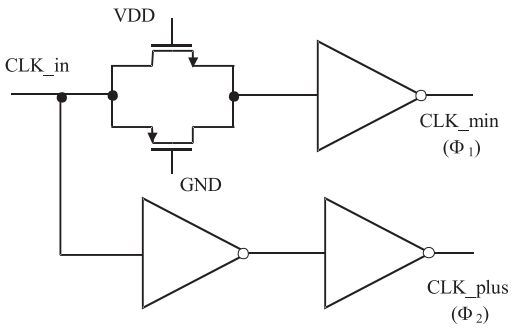

Fig. 6. Non-overlapping clock scheme

Specific transistor sizing shifts the threshold voltages of all the invertors in lines CLK_{min} and CLK_{plus} from the usual value of $V_{DD}/2$ to desired values providing the required timing. There are two outputs of the proposed non-overlapping clock generator: CLK_{min}, which controls the switches Φ_1, and CLK_{plus}, controlling the switches Φ_2. Signal CLK_{in} has a duty cycle 90 % because the offset cancellation phase (switches Φ_1 turned on and Φ_2 turned off) is supposed to be rather shorter (due to a shorter time needed to compensate the offset voltage) than the normal working phase, when the input signal is directly sensed, compared, evaluated, and sent to the current sensor output.

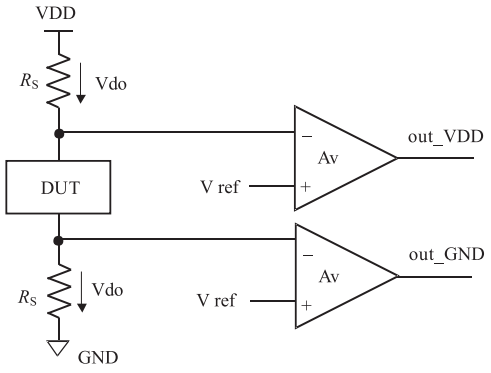

Fig. 7. Two sensors arrangement of current testing

2.3 Rail-to-rail Comparator

Since the voltage drop V_{do} across the current sensor is very small, the reference voltage V_{ref}, connected to the non-inverting input of the voltage comparator, is near to the supply voltage V_{DD}. For further considerations we

determine usage of a comparator with rail-to-rail inputs. This solution has also another advantage: such a current monitor might be inserted also in ground power supply line of the DUT, with minor changes needed in the sensor design. The only modification would be the value of the reference voltage selected near to GND.

In some test applications, one may use two current sensors — one connected in V_{DD} line and the other in GND line, as shown in Fig. 7. There are four possibilities of observed behavior:

- out_VDD GOOD, out_GND GOOD
- out_VDD GOOD, out_GND BAD
- out_VDD BAD, out_GND GOOD
- out_VDD BAD, out_GND BAD

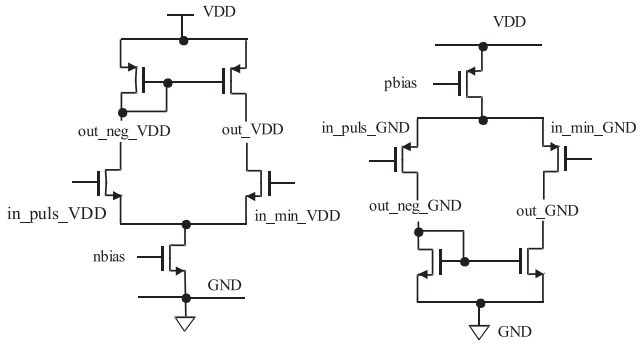

Fig. 8. Simple one-stage comparators

For example if the monitor placed in V_{DD} line indicates a defect present (BAD) in the DUT and monitor placed in GND line signalizes good circuit (GOOD), then it might mean that there is possible leakage current somewhere in the circuit.

A comparator with rail-to-rail input is needed because sensed voltages might be near to the supply potential. Since a simple topology for a minimal chip size is considered, a rail-to-rail comparator with two simple differential stages (Fig. 8) was used. The differential stage with PMOS input pair for a sensing the voltage close to the GND potential and the operational amplifier with NMOS input transistors for sensing the voltage near to the VDD potential are used. Both comparators are biased by current of $4\,\mu$A. The presented voltage comparator, composed of two differential stages, takes much smaller chip area than rather complicated rail-to-rail comparator topologies. However, small gain of one-stage differential comparator is a major disadvantage of this solution but as shown in Fig. 4, the output buffer formed by a simple CMOS inverter is employed that improves the output characteristics of the proposed current sensor.

2.4 Rail-to-rail Comparator

The feasibility of the approach and the main properties of the proposed current sensor were verified by simulations done in Cadence environment using AMS $0.35\,\mu$m CMOS technology with supply voltage of 3.3 V. The achieved results show that the most important feature, affecting the monitor performance significantly, is the sensing resistor R_S as its particular resistance value determines the operating range, in which the sensor gives the accurate current monitoring. Thus, the accuracy of the proposed current sensor in a particular working range is given by the input offset cancellation ability of the auto-zero based voltage comparator. Table 1 demonstrates the accurate operating ranges determined by the respective R_S value.

Selection of the proper working range is a compromise between the accuracy and the maximum voltage drop allowed across the current sensor. Typical simulated offset of the comparator was $1\,\mu$V, and the worst case offset result obtained by Monte-Carlo analysis was $5.2\,\mu$V even for high temperatures. Very high accuracy given by low offset is achieved for the current range from 10 mA to 100 mA. However, these results represent theoretical accuracy obtained only from simulations with the ideal reference voltage V_{ref}, which does not vary with temperature and the supply voltage fluctuations.

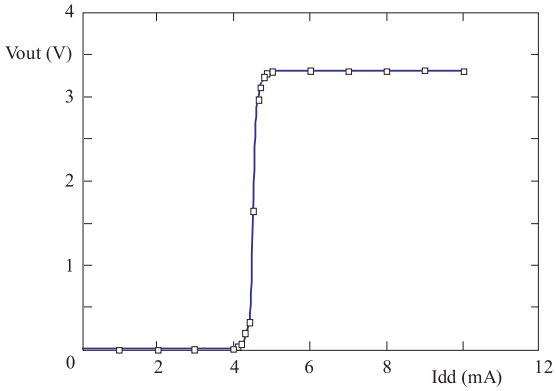

Fig. 9. Output of the proposed current sensor

Table 1. Accurate working ranges of the current sensor

RS (Ω)	Working range I_{DD}	V_{domax} (mV)	Accuracy (worst case)
2	$50\,\mu$A – $100\,\mu$A	0.2	10%
1	$50\,\mu$A – $100\,\mu$A	1	5%
1	$50\,\mu$A – $100\,\mu$A	1	0.5%
0.1	$50\,\mu$A – $100\,\mu$A	10	0.05%

The output signal of the monitor is shown in Fig. 9. The reference voltage was set to 4 mV and the value of the parasitic serial resistance was $1\,\Omega$. Low level of the output signal represents good state of the tested circuit while its high level indicates defective circuit.

Dynamic behavior of the proposed current sensor is shown in Fig. 10. The bottom curve displays the voltage drop on the resistive element, and the upper waveform represents the current sensor output. Time needed to transfer a fault appearance from the resistive element

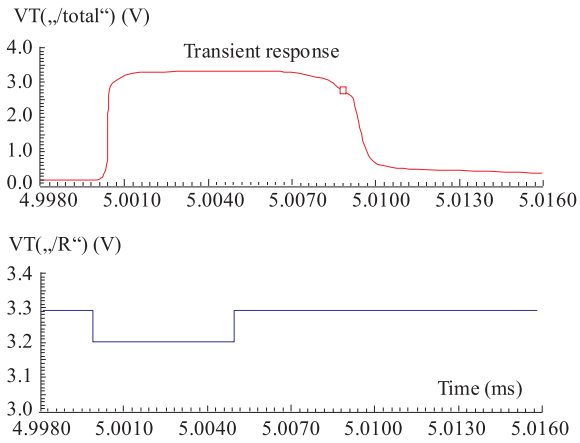

Fig. 10. Dynamic behavior of the sensor

to the buffer output is approximately $0.4\,\mu$s and it is called reaction time. Time needed for the output signal to recover from fault state to normal working state is called the recovery time and its achieved value is $4.4\,\mu$s. These two dynamic parameters play a dominant role in determining the maximum testing frequency.

In analog integrated circuits, the supply current consumption is usually not negligible and its waveform not uniform and easily predictable as it is in their digital counterparts. Therefore, an on-chip current monitor used for analog circuit testing should handle high currents and a wide range of supply currents. Since most of the known current sensors invoke unacceptable DUT performance degradation due to a significant voltage drop across the monitor itself, they are generally impractical for real test applications. The principle, proposed in this paper, minimizes the undesired voltage drop across the current sensor (even for very high supply currents to be measured) to the value commonly observed and caused by the parasitic serial resistance of the metal lines used. Thus, a slightly modified built-in current sensor can offer a wide range of possibilities and features useful for current testing of digital as well as analog and mixed-signal circuits.

3 DEFECTIVE PART LOCALIZATION CIRCUITRY AND EVALUATION RESULTS

A new approach to on-line localization of defective blocks in complex integrated circuits implemented in mixed technologies has been investigated. The basic idea is to divide the integrated circuit into smaller parts as it is shown in Fig. 11, which are tested using dedicated and efficient test techniques, and then the evaluation cyclic checking is performed to localize the defective part of the chip. Maximum testing frequency is determined by the technology used. The main advantage and contribution of this approach is reduction of the additional pins necessary for testing while it still provides information about the state of the tested circuit, and moreover, if there is a defect present, we know exactly which part of the chip might corrupt. Another benefit of this localization technique is versatility since it is not depended on a particular system architecture and technology used.

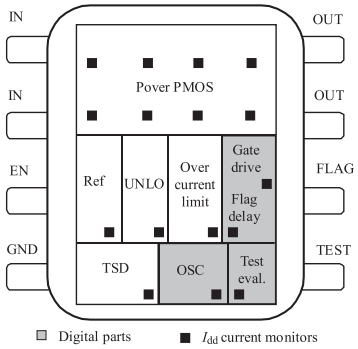

Fig. 11. Tested chip divided into smaller logical parts

Signals from all the system blocks, which indicate the state (GOOD or BAD) of locally tested parts are conveyed into a single evaluation circuit, shown in Fig. 12a. Digital inputs are cyclically switched by the multiplexer (MUX), which is under n-*bit* counter control. The n-*bit* round counter builds the address of the respective sensor, which is actually connected to the signal c. If signal c reaches value of logic one, this indicates that the circuit part currently evaluated is faulty and the address obtained localizes it.

Thus, signal c enables the parallel shift register, which converts parallel data coming from different blocks to a single serial output in order to minimize the number of additional pins as much as possible. From this consideration, if there is the n-*bit* counter used as the address generator it is possible to check cyclically 2^{n-1} input sensors. Address that includes only zeroes at the serial data output indicates the fault-free DUT. The input clock signal CLK is usually derived from system clock signal of digital part of the tested mixed-signal circuit.

The received evaluation waveforms in time domain are shown in Fig. 12b, where a defect at the output of the sensor number 3 has been detected, since there is the high state. Hence, when the sensor is addressed (time t_1 may take maximum n cycles of the counter) it generates logic one at signal c. Thus, serial data on the output of the register is delayed from rising fault about $n+1$ clock cycles (time t_2) because one clock cycle is needed to latch parallel data to the register and then n cycles for parallel to serial data conversion.

4 EXPERIMENTAL TEST VEHICLE — USB POWER DISTRIBUTION SWITCH

The USB high side power distribution switch was used as a mixed-signal device under test for proposed I_{DD} current sensor. This circuit (Fig. 13) was designed at the Department of Microelectronics, Slovak University

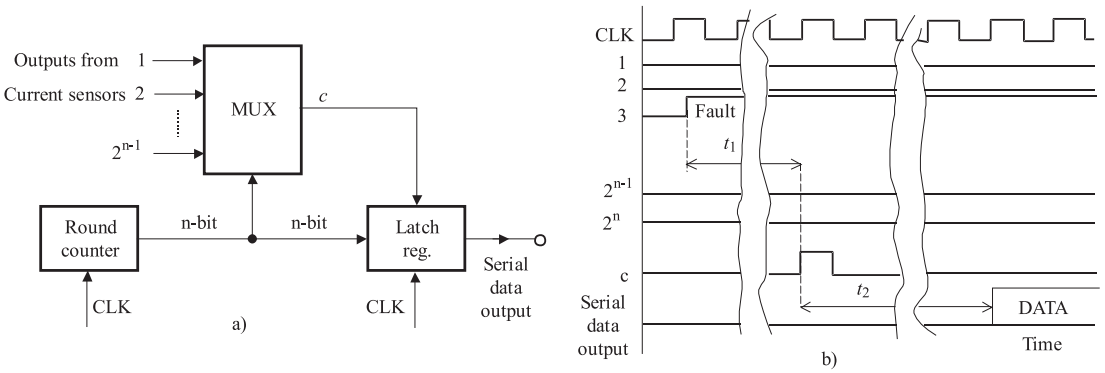

Fig. 12. Principal schematics of the proposed evaluation block a), time domain characterization b)

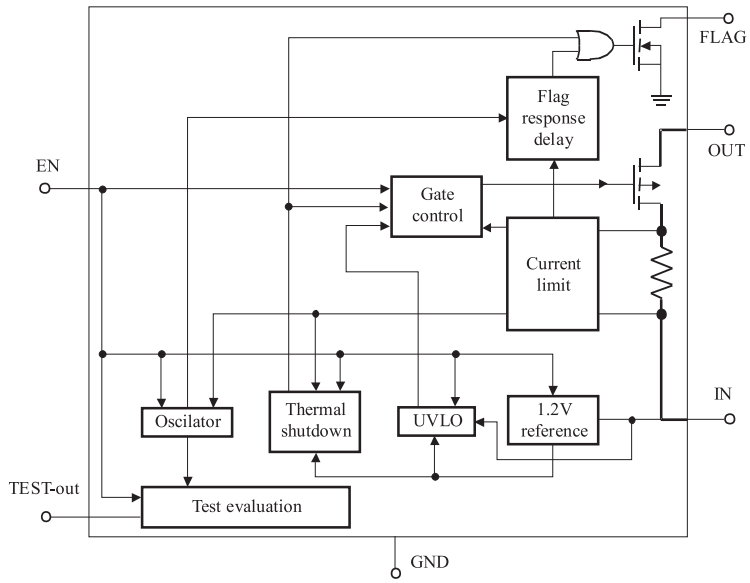

Fig. 13. Internal circuitry of DUT with implemented evaluation part

of Technology. It is mostly an analog circuit with power device but it also includes some digital parts. As it is shown in Fig. 11, the digital part consists of an oscillator, a flag delay circuit, and the part of gate driver. Analog part include a voltage reference circuit, a temperature shutdown (TSD) block, and an under-voltage lock-out circuit (UVLO).

From USB specifications, the switch has to supply current of 500 mA to the other devices connected at the output of the switch with maximal voltage drop of 100 mV. Therefore, a PMOS transistor, which takes approximately 70 % of the total chip size, was employed as the necessary power device. We use 16 current sensors all over for monitoring the supply current and defective part localization in the whole USB switch design. However, eight sensors provide the supply current monitoring of the PMOS power device itself. The switch has its own indicator of abnormal behavior that is formed by the flag output signal, indicating some problems within the switch (*eg* very high current at the output, chip overheat, high voltage drop and more). For our consideration this pin is very useful, since it provides information about the performance, behavior and specifications of the switch. Besides, if the current sensors and the localization circuit are placed on the chip, additional information about a possible defect present and its localization can be obtained simultaneously on the other pin (TEST). By this way, the reliability of the tested chip might be significantly enhanced.

5 CONCLUSIONS

A new on-chip dynamic current sensor for accurate measurement of the dynamic supply current in a wide current range is proposed. By employing the parasitic serial resistance of the metal line of VDD routing as a sensing element, the proposed current sensor does not cause undesired degradation of the DUT supply voltage. Thus, it is able to measure dynamic currents in the range from 50 μA to 100 mA without affecting the DUT performance. The proposed current monitor offers sensitive and accurate supply current measurement through either V_{DD} or GND metal line because of the rail-to-rail voltage

comparator being used. There is one-bit information generated at the sensor output indicating the actual state of the DUT, either good or defective. The developed monitor is dedicated primarily to testing of large mixed-signal circuits. Thus, the reference voltage V_{ref} necessary for the comparator threshold might be generated by a voltage reference circuitry usually present in the analog part of the whole tested design. On the other hand, the clock signal *CLK_in* for auto-zero based input offset cancellation circuit could be acquired from a digital part of the mixed DUT design. Modifying the current sensor in this way might simplify the sensor essentially, where no extra input pins or on-chip circuitry providing those signals would be needed. Current consumption of the whole sensor is $23\,\mu$A.

A new approach to on-line localization of defective blocks in complex integrated circuits has been proposed and investigated. The basic idea is to split the complex system into smaller parts, which are tested using the proposed current sensors described in this paper. Then the evaluation using cyclic checking the monitor outputs is performed in order to localize a defective part of the chip. The main contribution of this localization approach is reduction of the additional pins necessary for testing. Another benefit is the fact that this test methodology is versatile since it does not depend on the particular system architecture or technology used.

The proposed current sensing circuit has been implemented in $0.35\,\mu$m CMOS technology by Austriamicrosystems and it will be fabricated together with the experimental USB high side power distribution switch containing the localization circuit in the near future.

Acknowledgements

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