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A PRACTICAL APPROACH TO THE DESIGN AND IMPLEMENTATION OF SPEED CONTROLLER FOR SWITCHED RELUCTANCE MOTOR DRIVE USING FUZZY LOGIC CONTROLLER

Subramanian Vijayan [*] — **Shanmugam Paramasivam** [**] — **Rengasamy Arumugam** [*] — **Subhransu S. Dash** [*] — **Kittu J. Poornaselvan** [*]

This paper presents a speed control scheme of the Switched Reluctance Motor (SRM) using a novel fuzzy logic controller (FLC). The fuzzy logic speed controller is employed in the outer loop. The complete speed control scheme of the SRM drive incorporating the FLC is experimentally implemented using a digital signal processor board TMS320F2812 for a proto type 1.2 kW SRM. The performances of the proposed FLC based SRM drive is investigated experimentally at different dynamic operating conditions such as a change in the load under soft chopping mode with different rule bases. The experimental results show that the FLC is more robust and, hence, found to be a suitable replacement of the conventional controllers for the high-performance SRM drive applications.

K e y w o r d s: switched reluctance motor, fuzzy-logic controller, speed control and digital signal processor (TMS320F2812)

1 INTRODUCTION

The switched reluctance motor (SRM) is a doubly salient machine with independent phase windings on the stator and a solid laminated rotor. The stator windings on diametrically opposite poles are connected in series to form one phase of the motor. When a stator phase is energized, the most adjacent rotor pole-pair is attracted towards the energized stator in order to minimize the reluctance of the magnetic path. Therefore, by energizing consecutive phases in succession it is possible to develop a constant torque in either direction of rotation [1, 2]. Due to its attractive features of high efficiency, high power density and low maintenance cost, SRM is widely used in high performance servo applications, such as aerospace, industrial and robotics [1–10]. SRM cannot be run directly from the supply. It can be run only when the motor is integrated with power converter, controller and rotor position sensor. So it is essential to design a high performance digital controller for SRM to get the optimum performance in the presence of the parameters variations and load disturbances. Many papers have been reported on the performance simulation of SRM with experimental validation for different control strategies such as feed back linearization control, variable structure control, fuzzy logic control and four quadrant operation of SRM [11–16]. None of these papers has focused exclusively on settling time and Low N_{RMSE} under various operating conditions. This paper proposes a fuzzy logic speed controller for SRM. This controller employs the speed error and change in speed error to generate an equivalent control term. The designed fuzzy logic controller improves system performance particularly in steady state. This paper is organized as follows. Section 2 reviews the SRM description. Section 3 discusses the fuzzy logic controller implementation. Section 4 discusses the experimental setup. Section 5 discusses the results and discussion. Section 5 discusses the results. Conclusion is given in the last section.

2 SRM DESCRIPTION

A proto type SRM having 6 stator poles and 4 rotor poles is shown in Fig. 1. The prototype motor parameters are given in Appendix 1

Figure 2 shows an idealized inductance profile of an SR motor. The phase inductance is maximum when the rotor pole is aligned with the stator pole and is minimum when the rotor pole is aligned with the inter polar axis of the stator [1, 2].

$$L(\theta) = \begin{cases} L_{\min} & \theta_0 \le \theta \prec \theta_1\,, \\ L_{\min} + p\theta & \theta_1 \le \theta \prec \theta_2\,, \\ L_{\max} & \theta_2 \le \theta \prec \theta_3\,, \\ L_{\max} - p(\theta - \beta_r) & \theta_3 \le \theta \prec \theta_4\,, \\ L_{\min} & \theta_4 \le \theta \prec \theta_5\,. \end{cases} \tag{1}$$

here

$L(\theta)$ –inductance variation over one rotor pole pitch,
$L_{\min}$ –unaligned inductance (H),
$L_{\max}$–aligned inductance (H),
β_s –stator pole arc (rad),
β_r –rotor pole arc (rad),

$$\beta_r > \beta_s \text{ and } p = \frac{L_{\max} - L_{\min}}{\beta_s}\,.$$

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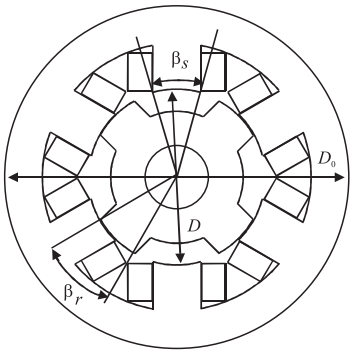


Fig. 1. 6/4 Pole proto type SRM.

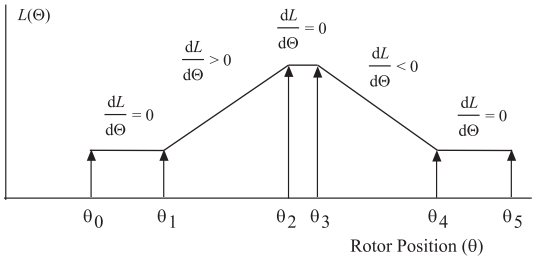


Fig. 2. Inductance (L) variation over one rotor pole pitch with constant current magnitude.

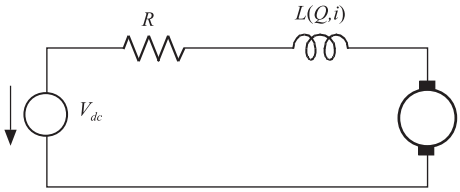


Fig. 3. Per phase electrical equivalent circuit of SRM.

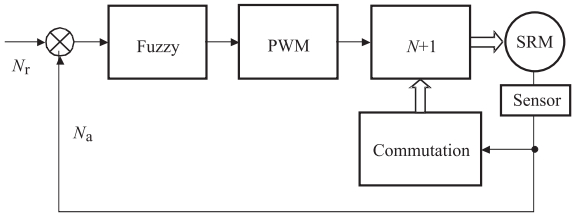


Fig. 4. Basic speed feed back control system.

The per phase equivalent circuit of the SRM can be drawn as shown in Fig. 3.

$$V(t) = Ri(t) + L(\theta, i)\frac{\mathrm{d}i}{\mathrm{d}t} + i\overline{\omega}\frac{\mathrm{d}L(\theta, i)}{\mathrm{d}\theta} \qquad (2)$$

where

V	is the voltage applied to the phase,
R	is the phase resistance,
$Ri(t)$	is the resistive voltage drop,
$L(\theta, i)\frac{\mathrm{d}i}{\mathrm{d}t}$	is the static voltage,
$i\overline{\omega}\frac{\mathrm{d}(\theta, i)}{\mathrm{d}\theta}$	is the speed voltage.

Equation (2) is applicable only when the mutual inductances are neglected. From the equation (2), it is understood that the speed voltage of each phase is proportional to the actual speed of the motor and rate of change of inductance with respect to rotor position [1, 2]. The instantaneous torque (T) produced in the SRM is given by the formula [1, 2]

$$T_d = \frac{1}{2}i^2\frac{\mathrm{d}L}{\mathrm{d}\theta}\,. \qquad (3)$$

From the above non linear equation, it is understood that motoring torque can be obtained only when the phase current is switched on during the rising period of phase inductance and braking torque can be obtained by switching the phase current during the decreasing period of phase inductance. It is obvious from Fig. 2. that in order to get optimum speed control, switching of phase currents must be done at appropriate rotor positions. This is why rotor position information is always important to operate an SRM drive. Rotor position information is fed back to the controller to determine the phase commutation sequence and instants. The proper choice of the turn-on and turn-off angles, determines the ultimate speed control of the SRM. In order to implement the control algorithm effectively, a high-speed digital controller has to be implemented. The basic block diagram of feedback speed control system of a SRM drive is shown in Fig. 4.

3 FUZZY CONTROLLER IMPLEMENTATION

Fuzzy logic controllers have experimentally shown excellent results, especially when faced with nonlinear control systems [17–20]. The complete block diagram of the fuzzy logic controller is shown in Fig. 5. The function of each block and its realization is explained below.

(a) Normalization:

Normalization performs the scale transformation, which maps the physical values of the speed (input) variable in to a normalized universe of discourse. In transient condition, the physical maximum range of speed error is taken as $\pm 1000\,\mathrm{RPM}$ and change in speed error as $\pm 100\,\mathrm{RPM}$ and the same are normalized to $\pm 1\,\mathrm{RPM}$ and $\pm 0.1\,\mathrm{RPM}$.

(b) Fuzzification:

The process of converting numerical measurements to grades of membership of fuzzy set members is called fuzzification. Hence fuzzification block matches the input data with the conditions of the rules to determine how well the condition of each rule matches that particular input instance. There is a degree of membership for each linguistic term that applies to that input variable.

Fuzzy controllers use different membership function for different applications. But here we used a Gaussian membership function for inputs and triangular membership function for output and its diagrammatic representation is shown in Figs. 6, 7 and 8.

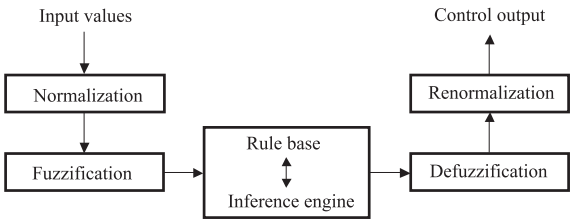


Fig. 5. Block Diagram of Fuzzy Logic.

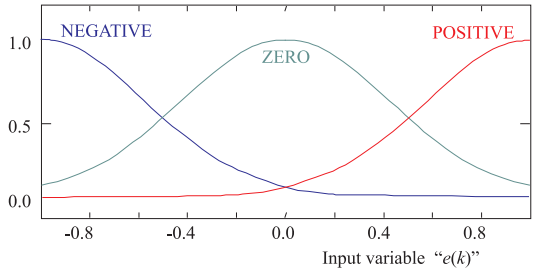


Fig. 6. Input member ship function for speed error $e(k)$.

Table 1. Rule structure and Rule matrix

Antecedent Block	Consequent Block
1. IF error=N and Change in Error=N	THEN output=VLS
2. IF error=N and Change in Error=Z	THEN output=LS
3. IF error=N and Change in Error=P	THEN output=MS
4. IF error=Z and Change in Error=N	THEN output=LS
5. IF error=Z and Change in Error=Z	THEN output=MS
6. IF error=Z and Change in Error=P	THEN output=HS
7. IF error=P and Change in Error=N	THEN output=MS
8. IF error=P and Change in Error=Z	THEN output=HS
9. IF error=P and Change in Error=P	THEN output=VHS

Change in Error \ Error	N	Z	P
N	VLS	LS	MS
Z	LS	MS	HS
P	MS	HS	VHS

The mathematical representation of a Gaussian membership and triangular membership functions are given as

$$\mu_e = \exp\Big[-\frac{(x-c)^2}{2\sigma^2}\Big] \tag{4}$$

$$\mu_\delta = \begin{cases} 0\,, & x \le a\,, \\ \frac{x-a}{b-a}\,, & a \le x \le b\,, \\ \frac{c-x}{c-b}\,, & b \le x \le c\,, \\ 0\,, & c \le x\,. \end{cases} \tag{5}$$

(c) Rule Base

Basically a rule base is a linguistic controller, which contains rules in the IF THEN format. In this research the fuzzy parameters of error $e(k)$ and change in error $e(k)-\big(e(k)-1\big)$ is modified by the adjectives "negative", "zero", and "positive". Here we used a 3-by-3 matrix, wherein the columns represent "negative error", "zero error", and "positive error" inputs from left to right and the rows represent "negative change in error", "zero change in error", and "positive change in error" input from top to bottom. This planar construct is called a rule matrix. It has two input conditions, "error" and "change in error" and one output response (at the intersection of each row and column). In this case there are nine possible logical product (AND) output response conclusions. All of them are given in Tab. 1.

(d) Inference Engine:

Figure 9 shows the rule viewer for the FLC wherein each of the nine rows refers to one rule. The first row says that if the error $e(k)$ is negative (N) and the change in speed error is negative (N) then the output should be low speed (VLS) (row 1, column 1). The rules corresponds the strategy that the control signal should be a combination of the error and the change in error, a fuzzy proportional-derivative controller. For each rule, the inference engine looks up the membership values in the condition of the rule. As the fuzzy logic controller receives inputs, the rule base is evaluated. The antecedent (IF $e(k)$ AND $e(k)-e(k-1)$) blocks test the inputs and produce decisions and the consequent (THEN Pulse width) blocks of some rules are satisfied while others are not. The final decisions are combined to form logical sums. These conclusions feed into the inference process where each response output member function's firing strength (0 to 1) is determined. From the Fig. 9, the input degree of membership can be written as

"error" $= -0.5:$ "negative" $= 0.5$ and "zero" $= 0.5$
and "change in error" $= -0.05:$ negative $= 0.5$
and "zero" $= 0.5\,.$

Once the input degree of membership is found, the "Error" selects rules 1 through 6 while "change in error" selects rules 1, 2, 4, 5, 7 and 8. "Error" and "change in error" for all rules are combined to get a logical product (AND, that is the minimum of either term). Out of the nine rules selected, wherein only four rules (1, 2, 4 and 5) are fired or have non-zero results and remaining rules have zero values. This leaves fuzzy output response magnitudes for only "very low speed (VLS)", "low speed (LS)" and "Medium speed (MS)" which must be inferred, combined, and defuzzified to return the actual crisp output. The rules with zero and non-zero values are given below.

1. IF error=N and Change in Error=N THEN VLS=0.5&0.5=0.5
2. IF error=N and Change in Error=Z THEN LS=0.5&0.5=0.5
3. IF error=N and Change in Error=P THEN MS=0.5&0.0=0.0
4. IF error=Z and Change in Error=N THEN LS=0.5&0.5=0.5
5. IF error=Z and Change in Error=Z THEN MS=0.5&0.5=0.5
6. IF error=Z and Change in Error=P THEN HS=0.5&0.0=0.0
7. IF error=P and Change in Error=N THEN MS=0.0&0.5=0.0
8. IF error=P and Change in Error=Z THEN HS=0.0&0.5=0.0
9. IF error=P and Change in Error=P THEN VHS=0.0&0.0=0.0

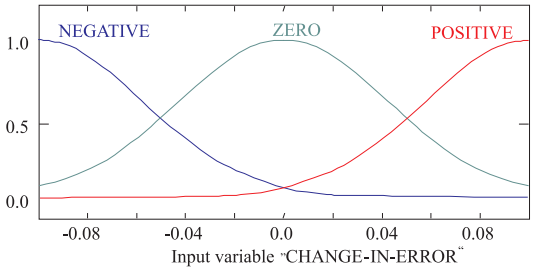


Fig. 7. Input membership function for change speed in error $e(k) - e(k-1)$.

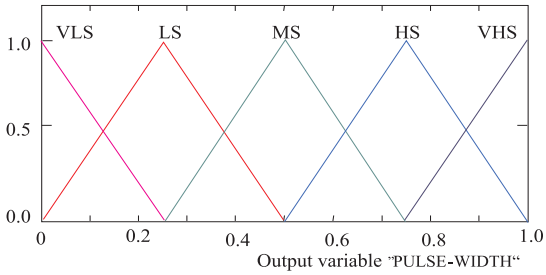


Fig. 8. Output membership function for duty ratio.

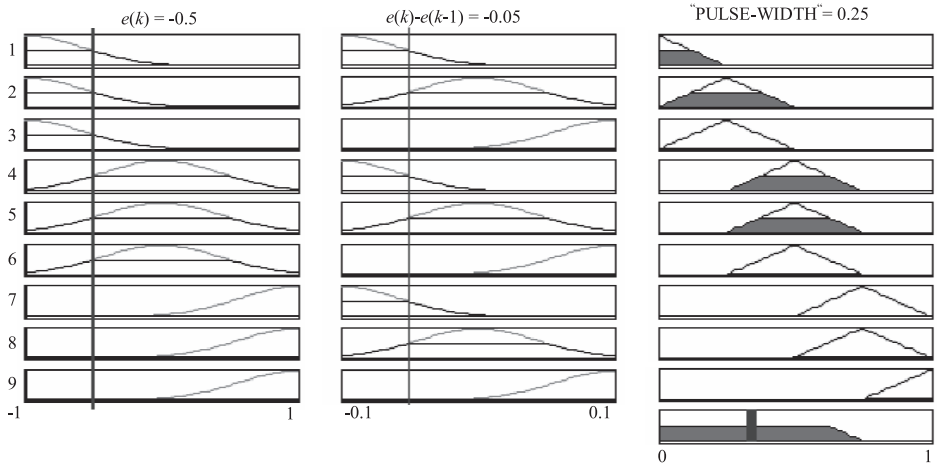


Fig. 9. Output membership function for duty ratio.

Table 2. Commutation Table for One Rotor Pole Pitch for Different Modes

Degrees	A	B	C	NORMAL			BOOST			ALD			BRAKE		
				1	2	3	1	2	3	1	2	3	1	2	3
0–7.5	1	1	0	0	0	1	0	0	1	0	1	0	1	0	0
7.5–15	0	1	0	0	0	1	0	1	0	0	1	1	1	0	0
15–22.5	0	1	0	0	0	1	0	1	0	0	1	1	1	0	0
22.5–30	0	1	1	0	1	0	0	1	0	1	1	1	0	0	1
30–37.5	0	1	1	0	1	0	0	1	0	1	1	1	0	0	1
37.5–45	0	0	1	0	1	0	1	0	0	1	0	1	0	0	1
45–52.5	0	0	1	1	1	0	1	0	0	1	0	1	0	0	0
52.5–60	1	0	1	1	0	0	1	0	0	1	0	0	0	1	0
60–67.5	1	0	1	1	0	0	1	0	0	1	0	0	0	1	0
67.5–75	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0
75–82.5	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
82.5–90	1	1	0	0	0	1	0	0	1	0	1	0	1	0	0

(e) Defuzzification

The RSS (Root Sum Square) method was chosen to include all contributing rules, since there are few member functions associated with the inputs and outputs. Figure 9 shows that error of -0.5 and a change in error -0.05 selects regions of the "Very low speed (VLS)", "low speed (LS)" and "Medium speed (MS)" output membership functions. The corresponding output membership function strengths are ranging from 0–1 from the possible rules (R1–R9) are given below

The strengths of each output membership functions are calculated as follows.

$$VLS\_strength = \sqrt{R_1^2} = 0.5\,,$$

$$LS\_strength = \sqrt{R_2^2 + R_4^2} = 0.707\,,$$

$$MS\_strength = \sqrt{R_3^2 + R_5^2 + R_7^2} = 0.5\,,$$

$$HS\_strength = \sqrt{R_6^2 + R_8^2} = 0.0\,,$$

$$VHS\_strength = \sqrt{R_9^2} = 0.0\,.$$

The defuzzification of the data into a crisp output can be obtained by combining the results of the inference process and then computing the "fuzzy centroid" of the area. The weighted strengths of each output member function is multiplied by their respective output membership function center points and summed. Consequently, this area is divided by the sum of the weighted member function strengths and the result is taken as the crisp output.

$$Crisp\_output = \frac{\begin{array}{r}(\text{VLS\_center*VLS\_strength}+\\ \text{LS\_center*LS\_strength}+\\ \text{MS\_center*MS\_strength}+\\ \text{HS\_center*HS\_strength}+\\ \text{VHS\_center*VHS\_strength})\end{array}}{\begin{array}{r}(\text{VLS\_center} + \text{LS\_strength}+\\ \text{MS\_strength}+\\ \text{HS\_strength} + \text{VHS\_strength})\end{array}} = 0.25\,.$$

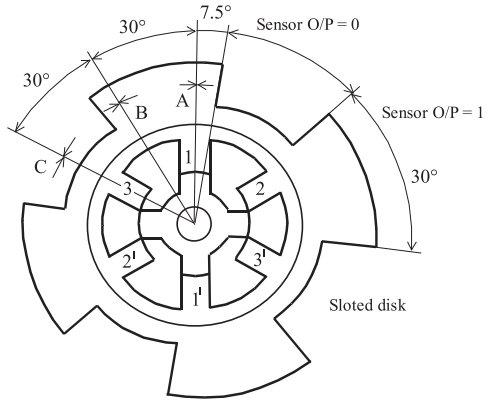


Fig. 10. Rotor Position sensor.

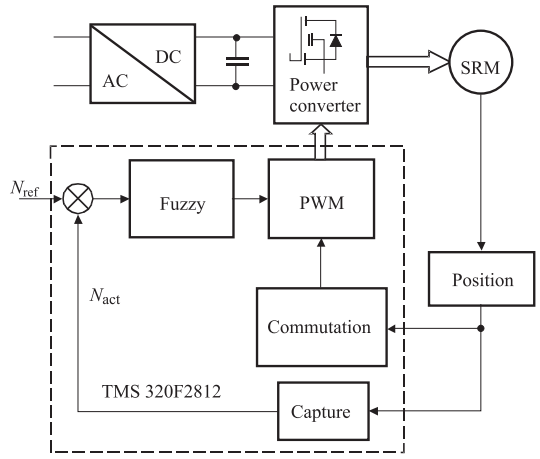


Fig. 11. Block diagram of the system setup.

Table 3. N_{RMSE} (Speed Root mean square error)

Sl.No	Rule base size	Speed root mean square error (RMSE)in rpm
1.	3×3	29.2
2.	4×4	17.9
3.	5×5	19.6
4.	6×6	11.8
5.	7×7	11.2
6.	8×8	10.8
7.	9×9	7.6
8.	10×10	8.7
9.	11×11	13.2

(f) Denormalization:

The crisp output of the fuzzy logic controller is normally in the range of 0 to 1. In order to get the desired pulse width, it is required to multiply the crisp output by 0xFFFF (maximum pulse width = 65535). The algorithm developed in the discrete time domain has been implemented through a high-speed digital signal processor (TMS320F2812)

4 EXPERIMENTAL SETUP

(1) HARDWARE

Figure 11 shows the block diagram of the system setup of the speed controller for Switched Reluctance Motor drive. The following describes the function of each block of the speed control of SRM drive.

(a) Rotor Position sensor

An aluminum disc is cut and sensors are fixed as shown in Fig. 10, wherein three position sensors are placed such that each is displaced by an angle of 30 degrees. The signals obtained form the sensors are tabulated and is given Table 1. Once rotor position information is available, it is possible to run the machine in different modes such as NORMAL, BOOST, ALD and BRAKING. Commutation logic for all the four modes are also tabulated in Tab. 2

(b) Power Converter:

The low cost converter with less number of switches for an N phase motor is the $N + 1$ converter topology, wherein $N + 1$ power switches and diodes with sensing circuit are shown in Fig. 12 [21]. The first step in designing the power converter is to select the power semiconductor devices. This consists of four main switches and four freewheeling diodes. The input to the system is fixed at 160 V DC and system is designed for an average load current of 16 A. Power MOSFETs (IRFP360, a 400 V and 23 A) and ultra fast freewheeling diode (MUR3060, 600 V, 30 A) was chosen as the main components for the converter. All the devices are mounted on the heat sink and the interconnections are made on a PCB.

MOSFETs. To turn the MOSFET ON, the input to the driver is OFF, thus turning the NPN Transistor ON, (which provides a positive gate voltage to the MOSFET and turn-OFF of the device) the gate is shorted to the source through R_g and PNP transistor. The drive circuit requires isolated dc power supplies. The output of the gate driver is connected across the gate and source of the power MOSFET. The source terminal of the upper MOSFET is floating and it can either be at 0V or at 160 V. As this is connected to the gate driver ground, this floating ground would generate lot of common mode noise. This would interfere with the normal operation of the circuit and it might malfunction. To avoid this situation, the ground of each gate driver output is isolated from the grounds of the other gate driver and also from the input stage ground. The input-output isolation is achieved by an opto-coupler HCPL 4503 to transfer the control signal from the input buffer stage to the gate driver stage. Further, an isolated DC/DC converter ensures that the grounds of each gate driver circuit are isolated from the each other. The complete gate driver and opto isolator circuit for one switch of the converter is given in Fig. 13.

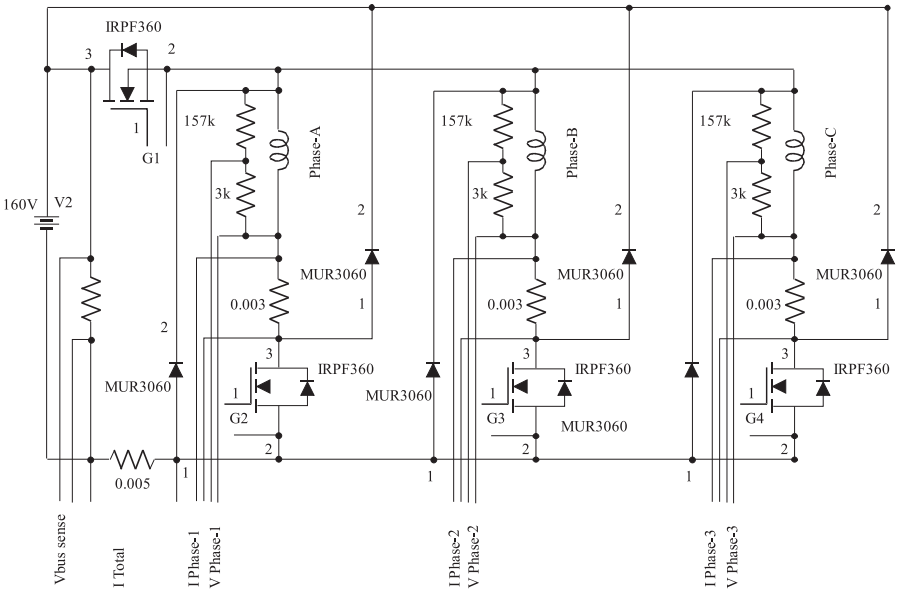


Fig. 12. "$N + 1$" SRM converter along with sensor arrangement.

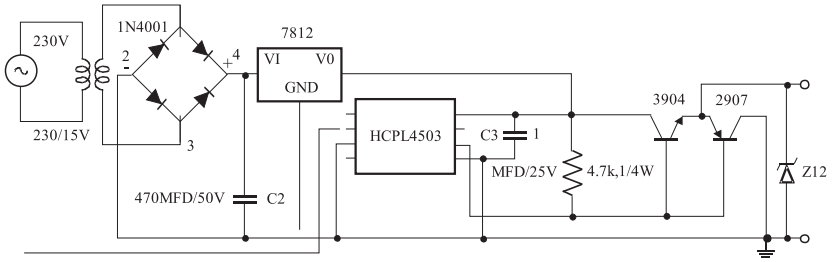


Fig. 13. Gate driver and opto isolator circuit for one switch of the converter.

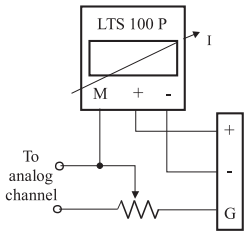


Fig. 14. Current sensing circuit.

(c) Current sensing circuit:

In order to maintain the current at desired value, the actual phase current is measured through current sensing circuit. The current sensing circuit is shown in Fig. 14.

(d) eZdsp F2812 Board

The eZdsp F2812 board is available from Texas Instruments as a development tool. The eZdsp kit provides a complete development environment, and includes the DSP board, power supply for the board, on-board JTAG compliant emulator, and an eZdsp specific version of the Code Composer Studio (CCS) integrated development environment (full featured, including debugger IDE, and ANSI C and C++ compliant compiler) [22]. The DSP board itself has nearly all-peripheral signals available on the board headers, making it easy to interface the board with other system hardware. The eZdsp board requires that pins 17 and 18 on header P9 be connected in order for the analog-to-digital converter (ADC) to function properly (*ie*, connect ADCLO to analog ground on the DSP). This connection was done manually on the board.

2 SOFTWARE

The entire SRM speed control system consists of system initialization, followed by a single interrupt loop (the ADC end-of-conversion interrupt), which implements Fuzzy Logic Control algorithm. GP Timer 1 is used to clock the PWM output at a 4 kHz switching frequency. The function main () performs CPU and peripheral initialization, and then enters an endless loop that waits for the ADC end-of-conversion interrupt. The controller itself is implemented in the ADC interrupt-service routine in the file DefaultIsr.c. The clock frequency of the DSP is 150 MHz. All timing calculations (*eg*, sample rates, PWM frequencies) have been performed based on this clock speed. The ADC sampling rate and PWM switching frequency can be changed using the constant sample period and PWM_period found in the file srm.h. The PWM is of the asymmetric type. The actual position information form one of the position sensors to the capture unit-1 is used to calculate the actual speed of the motor. Actual bus current and reference speed are fed to the ADC_chennal-0 and ADC_chennal-1. The values obtained from the ADC and Capture unit-1 will be an input to the FLC. The ADC channel used can be selected using the constant ADC_channel in the file srm.h.

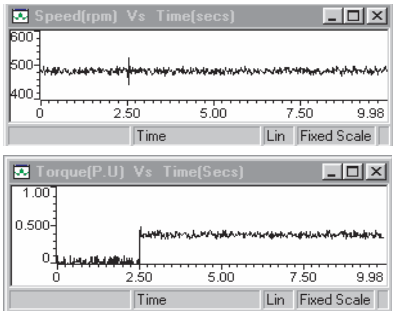


Fig. 15. Experimental results of (9×9 rule base) FLC, speed (top), torque (bottom), 0.4 *pu* Load, 480 rpm.

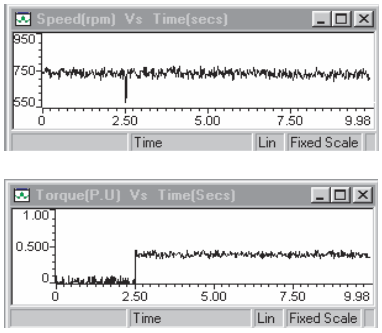


Fig. 16. Experimental results of (9×9 rule base) FLC, speed (top), torque (bottom), 0.4 *pu* Load, 750 rpm.

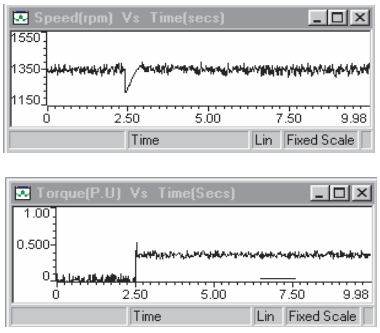


Fig. 17. Experimental results of (9×9 rule base) FLC, speed (top), torque (bottom), 0.4 *pu* Load, 1350 rpm.

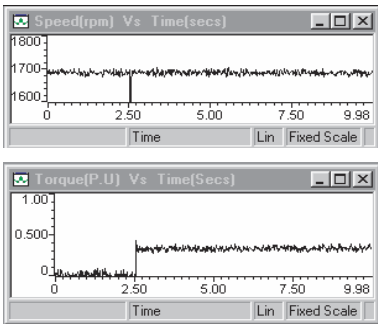
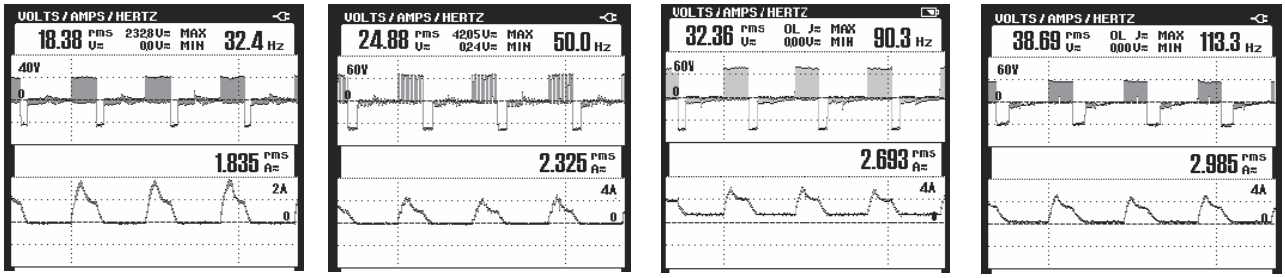


Fig. 18. Experimental results of (9×9 rule base) FLC, speed (top), torque (bottom), 0.4 *pu* Load, 1700 rpm.

The ADC_channel configuration uses the ADCINA0 and ADCINA1 channels. The speed reference value is from 0–3.0 volts, which corresponds 03000 rpm. This can be changed through ADCINA0. All of the variables pertaining to the SRM controller are contained in the structure SRM1 declared in the file GlobalVariableDefs.c. This structure is of type Fuzzy is defined in the file srm.h. The Fuzzy logic rules and constants related to the membership functions are assigned to the SRM1 structure in the function main (). In addition, the total controller output as well as the current control limit is independently assigned in main (). All of these values can be altered if desired. However, it was observed during experimentation that sampling the speed signal at the same time, the PWM switched either on or off induced noise in the converted actual speed-reading. To overcome this problem, it is desired to synchronize the triggering of the ADC (*ie*, GP Timer 2) with the PWM clock base (*ie*, GP Timer 1), and then adjusts the sampling instant such that the PWM is not switching at that moment.

5 RESULTS

The speed control systems was built and tested to evaluate the performance of a novel fuzzy logic control algorithm. A prototype MOSFET based classic bride converter was fabricated to energize the 6/4-pole SRM. The Fuzzy Logic based Digital controller is implemented through TMS320F2812 digital signal processor. Figs. 15–19 shows the experimental results of 9×9 rule base FLC based SRM drive. Fig. 15 through Fig. 18 show the experimental results of actual speed (rpm), torque (p.u) of the FLC based SRM drive for a load change at $t = 2.5$ secs under soft chopping mode. In all the cases the dwell angle is kept constant at 30 degrees. Figure 19 shows experimental results of Phase Voltage (top), Phase Current (bottom) at different operating conditions. Also, different combinations of rule base have been used to verify the effectiveness of fuzzy controllers, *ie* rule base are in the form of 3×3, $4 \times 4 \ldots 11 \times 11$. For illustration and simplicity, in this paper one 3×3 is explained. Among all, 9×9 rule base has minimum speed RMSE. From the above results, it is understood that by selecting suitable



(a) (b) (c) (d)

Fig. 19. Experimental results of (9×9 rule base) FLC, Phase Voltage (top), Phase Current (bottom), 0.4 *pu* Load, (a) 480 rpm, (b) 750 rpm, (c) 1350 rpm (d) 1700 rpm

combination of rule base, an effective and efficient Fuzzy Logic Controller can be designed.

6 CONCLUSION

In this paper, a robust speed controller for a switched Reluctance motor drive using a digital controller has been developed and implemented based on a three-phase $N + 1$ converter. The controller employs digital Fuzzy logic speed controller. Experimental results in this paper show that dc bus voltage can be used to effectively control a three-phase 6/4 pole switched reluctance motor drive system to obtain the desired speed and torque even under highly dynamic loads. It was found during experimentation in 9×9 rule based FLC that the N_{RMSE} (Speed Root mean square error) of the SRM under steady state was less than 7.6 rpm. It is shown that almost perfect robust speed holding could be achieved if the input dc voltage is increased up to 160 V (the rated voltage for the motor under test). Most importantly, the implementation of this high-performance speed controller needs a high speed DSP, a few logic IC's, and a single current sensor. There is no requirement for any power or voltage sensors. It is concluded that digital 9×9 rule base Fuzzy Logic Controller are effective in dealing with the highly nonlinear characteristics of the SRM drive system during steady state operation.

Appendix 1

PROTO TYPE SR MOTOR PARAMETERS

Power	: 1.2 KW
Voltage	: 160 V
Current	: 16 A
Stator outer diameter	: 162 mm
Stator core length	: 90 mm
Stator inner diameter	: 80 mm
Shaft diameter	: 25 mm
No of poles in the stator	: 6
No of turns/pole	: 75
Cross section of the conductor	: 1.7 mm^2
Stator pole arc	: 29 deg
Stator pole height	: 20 mm
No of poles in the rotor	: 4
Rotor pole arc	: 32 deg
Rotor Pole height	: 15 mm

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