

DYNAMIC PERFORMANCE OF A BACK–TO–BACK HVDC STATION BASED ON VOLTAGE SOURCE CONVERTERS

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The recent developments in semiconductors and control equipment have made the voltage source converter based high voltage direct current (VSC-HVDC) feasible. This new DC transmission is known as “HVDC Light” or “HVDC Plus” by leading vendors. Due to the use of VSC technology and pulse width modulation (PWM) the VSC-HVDC has a number of potential advantages as compared with classic HVDC. In this paper, the scenario of back-to-back VSC-HVDC link connecting two adjacent asynchronous AC networks is studied. Control strategy is implemented and its dynamic performances during disturbances are investigated in MATLAB/Simulink program. The simulation results have shown good performance of the proposed system under balanced and unbalanced fault conditions.

Key words: HVDC, voltage source converter (VSC), IGBT, SPWM, control design

1 NOMENCLATURE

U_L	the sinusoidal AC voltage in the AC network
$U_{V(1)}$	the fundamental line to line voltage (valve side)
X_L	the leakage reactance of the transformer
δ	phase shift between U_L and $U_{V(1)}$
I_V	source current
L, R	phase reactor inductance and resistance
C	DC side capacitance
ω	source voltage angular frequency
m	modulation index
P, Q	AC active, reactive power inputs
U_d, I_d, P_d	DC side voltage, current, power
α, β	stationary α - β axis
d, q	synchronous d - q axis
p, n	positive, negative components
*	reference value for controller

2 INTRODUCTION

The availability of the modern semiconductor devices such as the Insulated Gate Bipolar Transistor (IGBT) [1] has led to the development of a new generation of power electric converters. These devices, unlike the conventional thyristors which have no intrinsic turn-off ability, are of the fully controlled type. The most common converters, which employ the self commutating, high voltage, high current, and high switching frequency power electronic devices, are the Voltage Source Converters (VSC). A number of FACTS controllers which use VSC as their basic building block have been already in operation in various parts of the world. The most popular controllers

are: the STATCOM, the SSSC, the UPFC, and the voltage source converter based HVDC transmission (VSC-HVDC) [2, 3].

The VSC-HVDC system is the most recent HVDC technology. It consists of two VSC, one of which operates as a rectifier and the other as an inverter. The two converters are connected either back-to-back or joined by a DC cable, depending on the application. Its main function is to transmit a constant DC power from the rectifier station to the inverter station, with high controllability. The VSC-HVDC has several main advantages against the conventional HVDC based on thyristors. They are [4, 5]:

1. Independent control of the active and reactive power output from each terminal.
2. Reduced requirements for harmonic filters.
3. Improvements of the power quality and system stability.
4. Elimination of the requirement for a local power generation.

These features make the VSC-HVDC attractive for connection of weak AC system, island networks, and renewable energy sources, which may be located in remote area, to a main grid.

This paper presents the elements of back-to-back VSC-HVDC where the converter stations are located at the same site and transmission line or cable is not needed. The paper will first give a brief description about the VSC-HVDC transmission system and its terminal control functions. Following that, typical operating contingency scenarios are simulated in order to evaluate transient performance. The simulation results confirm that the control strategy has fast response and strong stability.

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3 PRINCIPLE OF VSC OPERATION

The fundamentals of VSC transmission operation may be explained by considering each terminal as a voltage source connected to the AC transmission network via a three-phase reactor. The two terminals are interconnected either back-to-back or through a DC link, as schematically shown in Fig. 1.

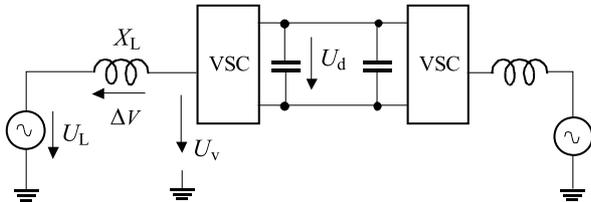


Fig. 1. Basic VSC transmission

The VSC converter can be represented as a variable AC voltage source where the amplitude, the phase and the frequency can be controlled independently of each other. It means that the VSC bridge can be seen as a very fast controllable synchronous machine with the instantaneous phase voltage (U_V in Fig. 1), as described by the following equation

$$U_V = \frac{1}{2}U_d m \sin(\omega t + \delta) + \text{harmonic_terms}. \quad (1)$$

Variables m and δ can be adjusted independently by the VSC controller to give any combination of voltage magnitude and phase shift in relation to the fundamental frequency voltage in the AC system. As a result, the voltage drop (ΔV shown in Fig. 1) across the reactor (X_L shown in Fig. 1) can be varied to control the active and reactive power flows.

The active power flow between the converter and the network can be controlled by changing the phase angle (δ) between the fundamental frequency voltage generated by the converter ($U_{V(1)}$) and the voltage (U_L) on the bus. The power is calculated according to equation (2) assuming a lossless reactor (X_L).

$$P = \frac{U_L U_{V(1)}}{X_L} \sin \delta. \quad (2)$$

The reactive power flow is determined by the amplitude of $U_{V(1)}$ which is controlled by the width of the pulses from the converter bridge. The reactive power is calculated according to equation (3). The maximum fundamental voltage out from the converter depends on the DC voltage.

$$Q = \frac{U_L(U_L - U_{V(1)} \cos \delta)}{X_L}. \quad (3)$$

4 SYSTEM UNDER STUDY

A 200 MW (± 100 kV DC) asynchronous interconnection is used to transmit power from a 230 kV, 2000 MVA, 60 Hz network having a SCR of 10 to 230 kV, 1000 MVA, 50 Hz network having a SCR of 5. As shown in Fig. 2, it consists of DC capacitors, two converters, passive high-pass filters, phase reactors, and transformers.

4.1 The AC systems

The AC networks, both at the rectifier and inverter end, are modeled as infinite sources separated from their respective commutating buses by system impedances. The impedances are represented as L-R/L networks having the same damping at the fundamental and the third harmonic frequencies. The impedance angles of the receiving end and the sending end systems are selected to be 80 degrees. This is likely to be more representative in the case of resonance at low frequencies [6].

4.2 The Converters

The converters are VSC employing IGBT power semiconductors, one operating as a rectifier and the other as an inverter. The rectifier and the inverter are three-level Neutral Point Clamped (NPC) VSC converters using close IGBT/Diodes. The two converters are connected either back-to-back connection (no DC cable).

4.3 The transformers and phase reactors

A 200 MVA converter transformer (Y_g/Δ) is used to permit the optimal voltage transformation. The 0.15 pu phase reactor with the 0.15 pu transformer leakage reactance permits the VSC output voltage to shift in phase and amplitude with respect to the AC system Point of Common Coupling (PCC) and allows control of converter active and reactive power output. The tap position is rather at a fixed position determined by a multiplication factor applied to the primary nominal voltage of the converter transformers. The multiplication factors are chosen to have a modulation index around 0.85 (transformer ratios of 0.915 on the rectifier side and 1.015 on the inverter side).

4.4 AC filters

To meet AC system harmonic specifications, AC filters form an essential part of the scheme. They can be connected as shunt elements on the AC system side or the converter side of the converter transformer. Since there are only high frequency harmonics, shunt filtering is therefore relatively small compared to the converter rating. The 40 Mvar shunt AC filters are 27th and 54th high-pass tuned around the two dominating harmonics.

4.5 DC capacitors

On the DC side there are two capacitor stacks of the same size (70 μ F). The objective for the DC capacitor is primarily to provide a low inductive path for the turned-off current and energy storage to be able to control the

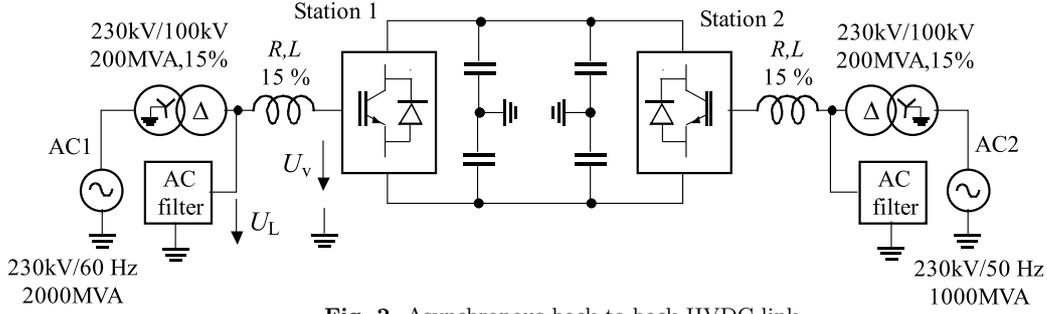


Fig. 2. Asynchronous back to back HVDC link

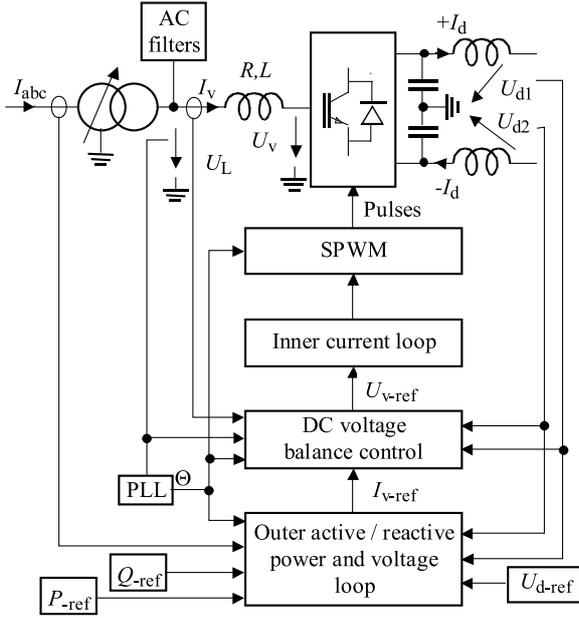


Fig. 3. Asynchronous back to back HVDC link

power flow. The capacitor also reduces the voltage ripple on the DC side.

5 CONTROL STRATEGY

For the convenience of the analysis, we have the following assumption: the station 1 controls both the active and reactive power exchanges between the AC system and DC link. The station 2 has the DC voltage and the reactive power as its control goals [7]. Figure 3 shows an overview diagram of the VSC control system and its interface with the main circuit. The converter 1 and converter 2 controller designs are identical. The two controllers are independent with no communication between them.

5.1 Phase locked loop

The phase locked loop (PLL) is used to synchronise the converter control with the line voltage and also to compute the transformation angle used in the $d-q$ transformation. The PLL block measures the system frequency and provides the phase synchronous angle Θ for the $d-q$

transformations block. In steady state, $\sin(\Theta)$ is in phase with the fundamental (positive sequence) of the α component and phase A of the point of common coupling voltage (U_{abc}).

5.2 Outer active and reactive power and DC voltage loop

The active power (at station 1) or the DC voltage (at station 2) is controlled by the control of δ and the reactive power is controlled by the control of the modulation index (m). The instantaneous active and reactive power of the inverter on the valve side can be expressed in terms of the dq component of the current and the voltage on the valve side as follows

$$p = \frac{3}{2} \text{Re}(\bar{u}_L^{dq} \bar{i}_v^{*dq}) = \frac{3}{2} (u_{Ld} i_{vd} + u_{Lq} i_{vq}), \quad (4)$$

$$q = \frac{3}{2} \text{Im}(\bar{u}_L^{dq} \bar{i}_v^{*dq}) = \frac{3}{2} (-u_{Ld} i_{vq} + u_{Lq} i_{vd}). \quad (5)$$

If the reference of the dq -frame is selected such that the quadrature component of the voltage is being very small and negligible ($u_{Lq} \approx 0$) then the equations (4) and (5) indicate that the active and the reactive power are proportional to the d and q component of the current respectively. Accordingly, it is possible to control the active power (or the DC voltage) and the reactive power (or the AC bus voltage) by control of the current components i_{vd} and i_{vq} respectively. The active and reactive power and voltage loop (shown in Fig. 4) contains the outer loop regulators that calculate the reference value of the converter current vector (I_{dq}^*) which is the input to the inner current loop.

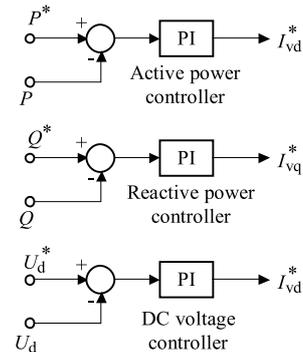


Fig. 4. Outer active and reactive power and DC voltage loop

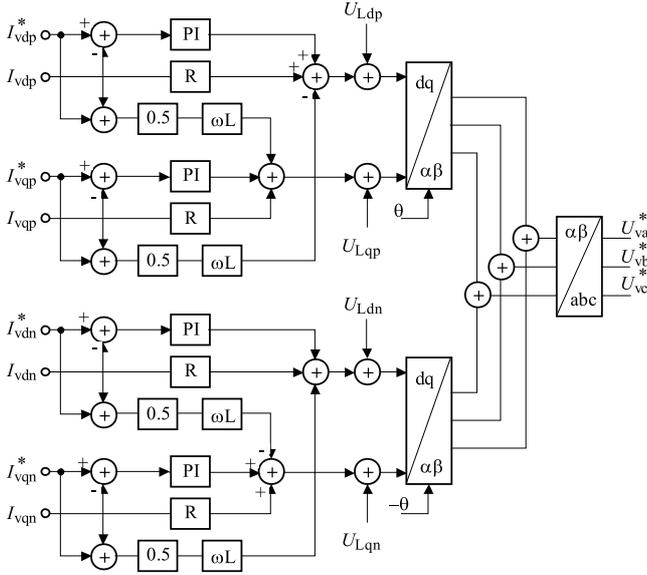


Fig. 5. Inner Current Controller

5.3 Inner current loop

For each of the phases we can write (Fig. 2)

$$U_L - u_v = L \frac{di_v}{dt} + Ri_v. \quad (6)$$

During unbalanced operation [8] the expression for the voltage drop over the reactor (R, L) holds for positive as well as for negative-sequence voltages and currents. The voltages drops are described by the differential equation

$$\frac{d}{dt} \begin{bmatrix} i_{vaX} \\ i_{vbX} \\ i_{vcX} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{vaX} \\ i_{vbX} \\ i_{vcX} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{vaX} \\ u_{vbX} \\ u_{vcX} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{LaX} \\ u_{LbX} \\ u_{LcX} \end{bmatrix}. \quad (7)$$

Where $X = (p)$ for positive sequence and (n) for negative sequence. Equation (7) can be transformed to the $\alpha\beta$ -frame. This gives for the voltages and currents:

$$\frac{d}{dt} \begin{bmatrix} i_{v\alpha X} \\ i_{v\beta X} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{v\alpha X} \\ i_{v\beta X} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{v\alpha X} \\ u_{v\beta X} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{L\alpha X} \\ u_{L\beta X} \end{bmatrix}. \quad (8)$$

Equation (8) can be further transferred into the rotating dq -frame:

$$\frac{d}{dt} \begin{bmatrix} i_{vdp} \\ i_{vqp} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ \omega & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{vdp} \\ i_{vqp} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{vdp} \\ u_{vqp} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{Ldp} \\ u_{Lqp} \end{bmatrix}. \quad (9)$$

and

$$\frac{d}{dt} \begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ \omega & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{vdn} \\ u_{vqn} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{Ldn} \\ u_{Lqn} \end{bmatrix}. \quad (10)$$

The positive and negative sequence voltages of the VSC side are obtained from (9) and (10):

$$u_{vdp} = u_{Ldp} - Ri_{vdp} + \omega Li_{vqp} - L \frac{d}{dt} i_{vdp}, \quad (11)$$

$$u_{vqp} = u_{Lqp} - Ri_{vqp} - \omega Li_{vdp} - L \frac{d}{dt} i_{vqp}, \quad (12)$$

and

$$u_{vdn} = u_{Ldn} - Ri_{vdn} - \omega Li_{vqn} - L \frac{d}{dt} i_{vdn}, \quad (13)$$

$$u_{vqn} = u_{Lqn} - Ri_{vqn} - \omega Li_{vdn} - L \frac{d}{dt} i_{vqn}. \quad (14)$$

The mean voltages over the sample period k to $k+1$ are derived by integrating (11), (12), (13) and (14) from kT_s to $(k+1)T_s$ and dividing by T_s (where T_s is the sampling time).

$$\bar{u}_{vdp} = \bar{u}_{Ldp} - R\bar{i}_{vdp} + \omega L\bar{i}_{vqp} - \frac{L}{T_s} \{i_{vdp}(k+1) - i_{vdp}(k)\}, \quad (15)$$

$$\bar{u}_{vqp} = \bar{u}_{Lqp} - R\bar{i}_{vqp} - \omega L\bar{i}_{vdp} - \frac{L}{T_s} \{i_{vqp}(k+1) - i_{vqp}(k)\}, \quad (16)$$

and

$$\bar{u}_{vdn} = \bar{u}_{Ldn} - R\bar{i}_{vdn} - \omega L\bar{i}_{vqn} - \frac{L}{T_s} \{i_{vdn}(k+1) - i_{vdn}(k)\}, \quad (17)$$

$$\bar{u}_{vqn} = \bar{u}_{Lqn} - R\bar{i}_{vqn} + \omega L\bar{i}_{vqn} - \frac{L}{T_s} \{i_{vqn}(k+1) - i_{vqn}(k)\}, \quad (18)$$

By assuming linear current and constant network voltage (the network voltage varies very little during a switching time period) during one sample period T_s we obtain from (15) through (18):

$$u_{vdp}(k+1) = u_{Ldp}(k) - \frac{R}{2} \{i_{vdp}(k+1) + i_{vdp}(k)\} + \frac{\omega L}{2} \{i_{vqp}(k+1) + i_{vqp}(k)\} - \frac{L}{T_s} \{i_{vdp}(k+1) - i_{vdp}(k)\}, \quad (19)$$

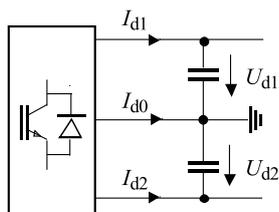


Fig. 6. DC Voltages and Currents of the Three-Level Bridge

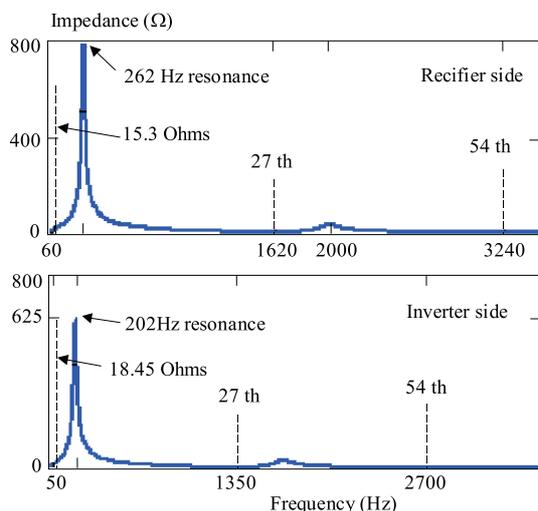


Fig. 7. Positive-Sequence impedances of the two AC networks

$$\begin{aligned}
 u_{vqp}(k+1) = & u_{Lqp}(k) - \frac{R}{2} \{i_{vqp}(k+1) + i_{vqp}(k)\} \\
 & - \frac{\omega L}{2} \{i_{vdp}(k+1) + i_{vdp}(k)\} \\
 & - \frac{L}{T_s} \{i_{vqp}(k+1) - i_{vqp}(k)\}, \quad (20)
 \end{aligned}$$

$$\begin{aligned}
 u_{vdn}(k+1) = & u_{Ldn}(k) - \frac{R}{2} \{i_{vdn}(k+1) + i_{vdn}(k)\} \\
 & - \frac{\omega L}{2} \{i_{vqn}(k+1) + i_{vqn}(k)\} \\
 & - \frac{L}{T_s} \{i_{vdn}(k+1) - i_{vdn}(k)\}, \quad (21)
 \end{aligned}$$

$$\begin{aligned}
 u_{vqn}(k+1) = & u_{Lqn}(k) - \frac{R}{2} \{i_{vqn}(k+1) + i_{vqn}(k)\} \\
 & - \frac{\omega L}{2} \{i_{vdn}(k+1) + i_{vdn}(k)\} \\
 & - \frac{L}{T_s} \{i_{vqn}(k+1) - i_{vqn}(k)\}, \quad (22)
 \end{aligned}$$

The control is based on (19), (20), (21) and (22), where the voltages and currents at time $(k+1)$ are thus equal to the reference values at time step (k) .

5.4 DC voltage balance control

The difference between the DC side voltages (positive and negative) are controlled to keep the DC side of the

three level bridge balanced (*ie*, equal pole voltages) in steady-state. Small deviations between the pole voltages may occur at changes of active/reactive converter current or due to nonlinearity or lack of precision in the execution of the pulse width modulated bridge voltage. Furthermore, deviations between the pole voltages may be due to inherent unbalance in the circuit components impedance. The DC midpoint current I_{d0} determines the difference U_{d0} between the upper and lower DC voltages (Fig. 6).

The DC midpoint current determines the difference between the upper and lower DC voltages, *ie*

$$I_{d0} = -(I_{d1} + I_{d2}) = -2C \frac{d}{dt} (U_{d1} - U_{d2}) = -2C \frac{d}{dt} U_{d0}. \quad (23)$$

By changing the conduction time of the switches in a pole it is possible to change the average of the DC midpoint current I_{d0} and thereby control the difference voltage U_{d0} . For example, a positive difference ($U_{d0} \geq 0$) can be decreased to zero if the amplitude of the reference voltage which generates a positive midpoint current is increased at the same time as the amplitude of the reference voltage which generates a negative DC midpoint current is decreased. This is done by the addition of an offset component to the sinusoidal reference voltage. Consequently, the bridge voltage becomes distorted, and to limit the distortion effect, the control has to be slow. Finally, for better performance this function should be activated in the station controlling the DC voltage.

6 SIMULATIONS RESULTS

The dynamic performance of the transmission system is verified by simulating the frequency response of the two AC systems and the following types of disturbances:

1. Steps on the regulators references,
2. Recovery from severe perturbations in the AC system.

6.1 Frequency response of the AC systems

Figure 7 demonstrates the magnitude, seen from the busbar where the filter is connected, of the combined filter and AC network impedance as a function of frequency.

Notice the two minimum impedances on the Z magnitudes of the AC systems, these series resonances are created by the 27th and 54th harmonic filters. They occur at 1620 Hz and 3240 Hz on the 60 Hz system (1350 Hz and 2700 Hz on the 50 Hz). The low principal natural frequency, coinciding with the parallel resonance at 262 Hz on the rectifier side and 202 Hz on the inverter side, is a determining factor in the development of overvoltages and interaction with the DC system.

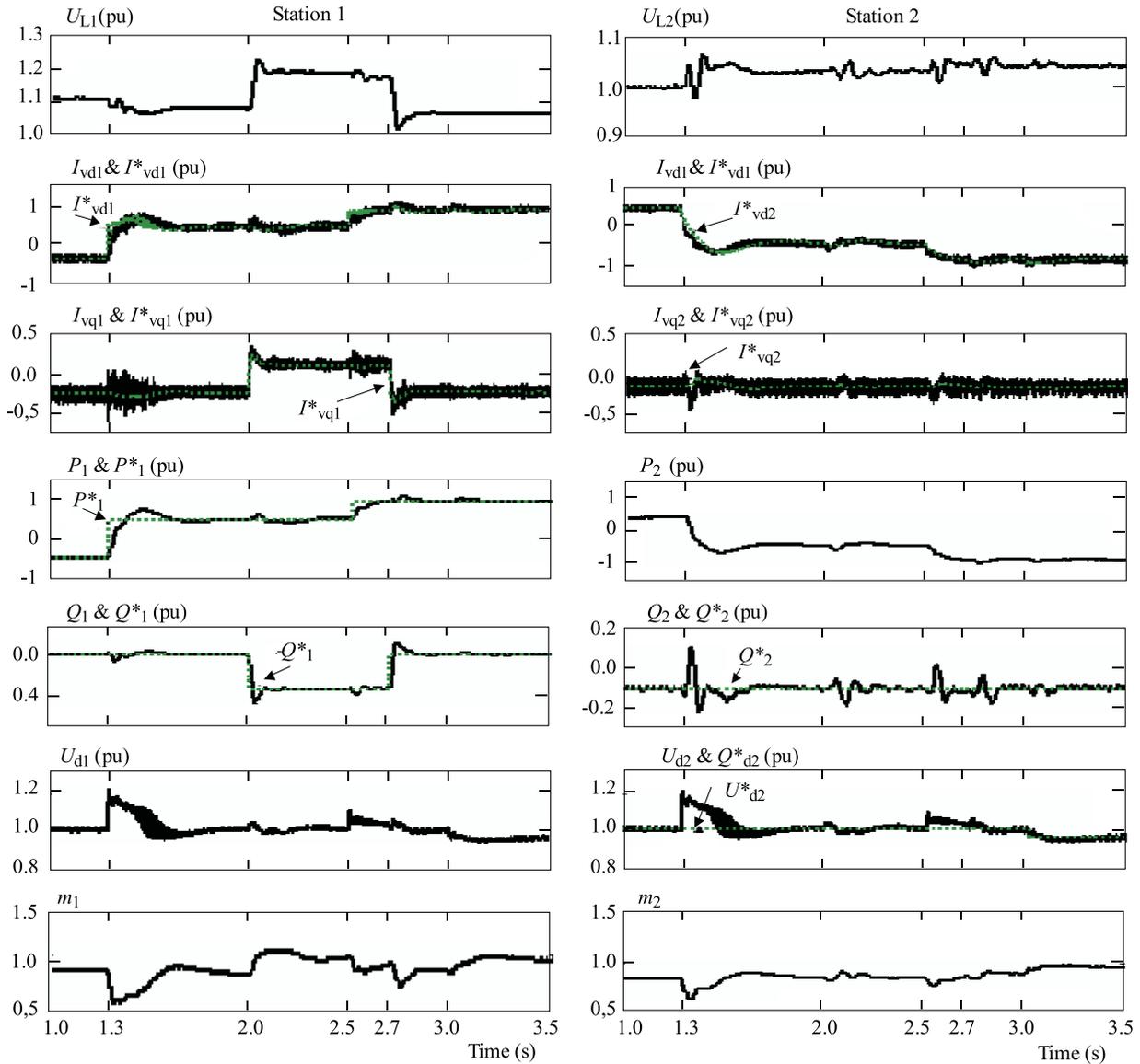


Fig. 8. Steps on the regulators references

6.2 Step responses

In order to test the dynamic responses of the VSC-HVDC regulators, three test cases have been studied:

- At $t = 1.3$ s the reference active power of converter 1 (P_1^*) is changed from -0.5 pu to $+0.5$ pu, and at $t = 2.5$ s from $+0.5$ pu to $+1.0$ pu
- From $t = 2.0$ s to $t = 2.7$ s the reference reactive power of converter 1 (Q_1^*) is changed from 0.0 pu to -0.4 pu.
- At $t = 3.0$ s the reference DC voltage of converter 2 is changed from $+1.0$ pu to $+0.095$ pu.

First the converter 1 active power reference value is changed from -0.5 pu to $+0.5$ pu and then set to 1.0 pu at $t = 2.5$ s. As can be seen from Fig. 8 the active power can track the reference of the active power.

The transferred active powers at both sides change the direction which causes transients on the DC voltage then returns to the reference value due to the DC voltage con-

troller. The AC voltages at the filter bus (U_{L1} and U_{L2}), can be kept constant except for some transients that occur when both the step changes are applied. The active power flow is adjusted to the new setting within 30 ms. At $t = 2.0$ s the reactive power step change is applied, this step change cause transients on the DC voltage, but, as expected, the step change of the active power causes a much higher transient than that with the change in reactive power. At $t = 2.5$ s the active power change to 1 pu, and later another step is also applied on the reference DC voltage of the inverter at $t = 3.0$ s. The reactive power and the DC voltage can track the references of the reactive power and the DC voltage. The active and reactive power responses are decoupled by the control design.

6.3 AC side perturbations

A remote three phase to ground fault was first applied at $t = 1.5$ s during 0.12 s (5 cycles on 60 Hz system) at

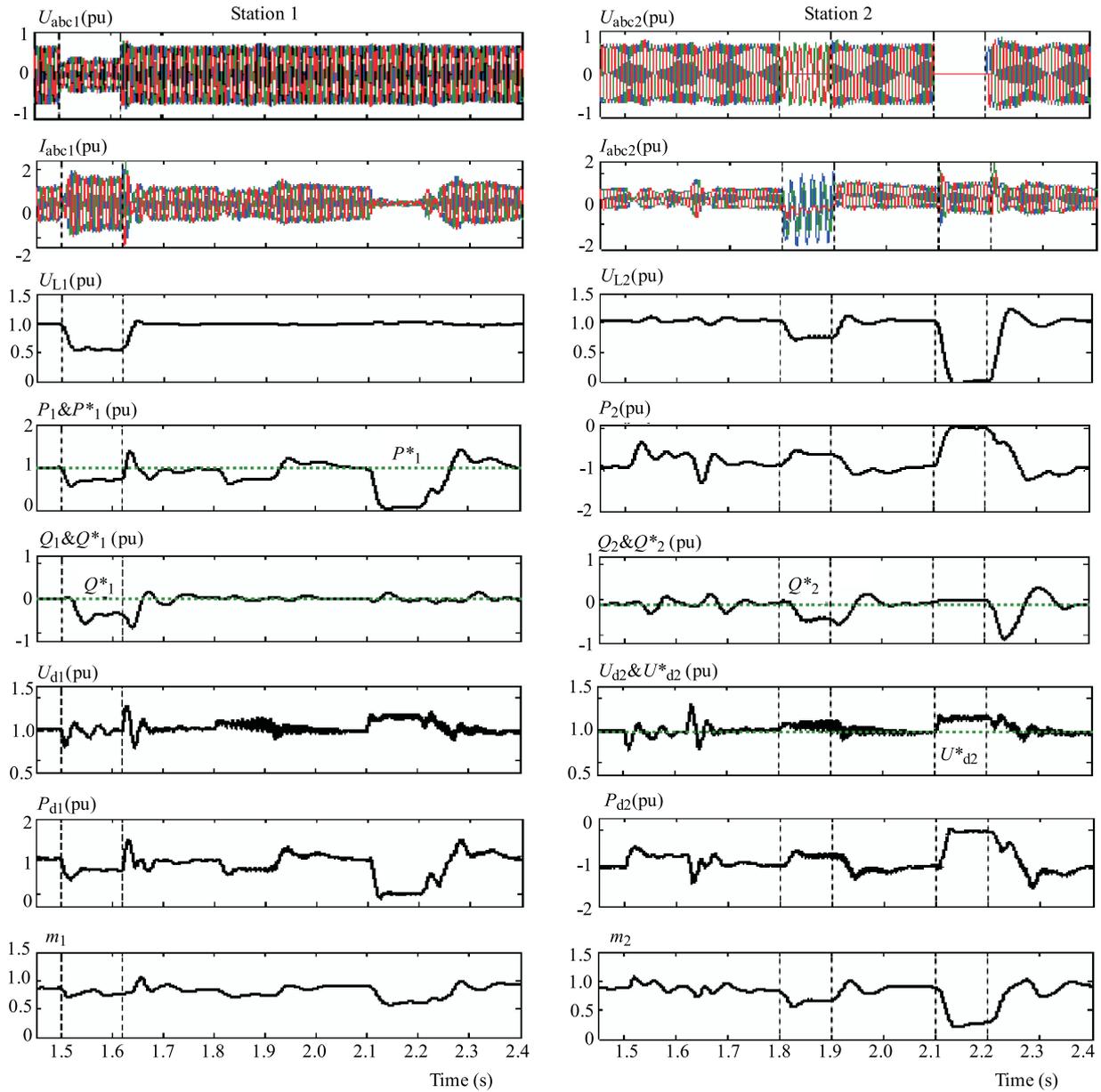


Fig. 9. AC side perturbations

station 1. A second perturbation follows. A single phase to ground fault was applied at $t = 1.8$ s during 0.10 s (5 cycles on 50 Hz system) at station 2 in order to investigate the behavior of VSC-HVDC during unbalanced faults. Then, a three-phase to ground fault is applied at station 2 at $t = 2.1$ s and is cleared at 5 cycles after the fault, *ie*, at $t = 2.2$ s. Figure 9 presents the simulation results. From the simulation, it can be noted that during the two first faults ($t = 1.5$ s at station 1 and $t = 1.8$ s at station 2), the active power flow is 1.0 pu, transmitted from converter 1 to converter 2, and is kept constant during the fault. The DC voltage drops and it contains an oscillation during the faults.

Consequently the transferred DC power contains also the oscillation. During these two faults the transmitted power can be kept constant except a small oscillation dur-

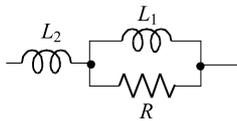
ing the fault. All oscillations in voltages and currents at both systems, means that the phase voltages and currents at both systems are unbalanced. During the severe three-phase fault at station 2 at $t = 2.1$ s, the AC voltage at station 2 side is decreased to 0.1 pu during the fault and recovers fast and successfully to 1.0 pu voltage after clearing the fault. The transmitted power flow is reduced to very low value during the fault and recovers to 1.0 pu after the fault. The DC voltage, which can be controlled to 1.0 pu during the fault, has some oscillations at the beginning of the fault and at clearing the fault, and its maximum transient value is about 1.2 pu. On the other hand, the phase currents at station 1 side decrease to low values to reduce the power flow.

6 CONCLUSION

In this paper, we have presented the steady-state and dynamic performances of an asynchronous back-to-back HVDC link based on voltage source converters, during step changes of the active and reactive powers, balanced and unbalanced faults. In all cases the proposed control strategy has been shown to provide fast and satisfactory dynamic responses of the proposed system. Besides controlling the through power flow, it can supply reactive power and provide independent dynamic voltage control at its two terminals. The two converters can be paralleled to double the reactive power capability supplied to one side or the other. Higher voltage designs can be used with transmission lines or cables to form point-to-point or multi-terminal transmission links. More sophisticated controls can be used to provide additional network benefits. From the simulation, it can be obtained that the VSC-HVDC can fulfil fast and bi-directional power transfers. It can be obtained also that during a single-phase fault the transmitted power can be kept constant except a small oscillation during the fault. However, during a three-phase fault; the decreased voltage at the converter terminals strongly reduces the power flow by the DC link. When the fault is cleared, normal operation is recovered fast.

APPENDIX

Data for the system model



Station 1:

The AC system 1 representing a strong system (2000 MVA, $SCR = 10$), consists of one source with an equivalent impedance of: $R = 13.79 \Omega$, $L_1 = 31.02 \text{ mH}$, $L_2 = 62.23 \text{ mH}$.

Station 2:

The AC system 2 representing a strong system (1000 MVA, $SCR = 5$), consists of one source with an equivalent impedance of: $R = 27.58 \Omega$, $L_1 = 62.04 \text{ mH}$, $L_2 = 124.46 \text{ mH}$.

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