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PAPERS

Design and implementation of a nano magnetic logic barrel shifter using beyond-CMOS technology

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Bit manipulation plays a significant role in high-speed digital signal processing (DSP) and data computing systems, and shift and rotation operations are crucial functions in it. In general, barrel shifters are used to perform these operations effectively. Nano magnetic logic circuits are among the promising beyond-CMOS alternative technologies for the design of high-speed circuits. Most of the existing circuits that have been developed using nano magnets are combinational circuits. In this work, a barrel shifter is implemented and realised using in-plane nano magnetic logic. The proposed design is the first of its kind nano magnetic logic circuit. The nano magnetic logic circuit implementation, layout generation, simulation, and validation were performed using the ToPoliNano and ModelSim tools. The logical equivalent design was synthesised and evaluated using the Synopsys Design Compiler tool. The proposed barrel shifter was realised using majority logic has 1769037 nano magnets with a boxing area of 481×13104 μm^2 and 3276 clock zones after optimisation with the Barycenter algorithm. The proposed barrel shifter realised using Boolean logic has 315276 nano magnets with a boxing area of 265×5028 μm^2 and 1257 clock zones after optimisation with the Barycenter algorithm. The proposed design results demonstrate that complex systems can be developed using nano magnetic logic by combining combinational and sequential circuits.

K e y w o r d s: barrel shifter, Boolean logic, beyond CMOS, majority logic, nano magnets

1 Introduction

Field-coupled devices appear to be a promising alternative to the rising demands of complementary metal oxide semiconductor (CMOS) scaling and its limitations [1-6]. The emerging interesting beyond-CMOS computational paradigms, such as quantum-dot cellular automata (QCA), have the ability to realise high-performance designs with higher packing densities, simplified interconnections, and very low power-delay products. Features such as low conversion efficiency, lower temperature of operation, device production yield, and decoherence hinder the practical realisation of such QCA circuits developed using metals. However, the deployment of nano magnets promises to realise high-performance circuits at room temperature [7,8]. These circuits transfer information by coupling single-domain nano magnet magnetisation states to their adjacent neighbours using magnetic dipole interactions. The lack of movement of current and non-volatile memory are the prime advantages of nano magnet-based circuit design.

Circuits developed using nano magnets and controlled field applications are called nano magnetic logic (NML) circuits. There are two types of NML: perpendicular NML (pNML) and in-plane NML (iNML). Several attempts have been made to design and validate NML circuits. Among the existing tools, the Torino politecnico nanotechnology (ToPoliNano) tool is widely recognised by researchers to validate NML circuits. The ToPoliNano tool designs iNML circuits and performs automatic layout generation and simulation. The circuits designed and validated by the tool in the literature are predominantly combinational circuits such as the half adder[9], full adder[10], multiplexer [11], demultiplexer [12], decoder [13], ripple carry adder [14], 32 bit Pentium-4 tree-Adder [15], ISCAS 85 benchmark [16], and systolic multiplier [17]. Sequential circuits have not been designed much in iNML.

Registers form key storage and processing elements in the digital system. A barrel shifter with the ability to perform both shift and rotation functions is widely used to perform complex arithmetic and logical operations. In this work, a barrel shifter NML circuit was designed using the and-or-inverter (AOI) logic and majority logic in ToPoliNano. The proposed barrel shifter is the first of its kind NML circuit realisation, and can be used to develop processors and other computational blocks. The logical equivalence of both circuits was verified, and the iNML realisation was performed in ToPoliNano.

2 Related background

2.1 Majority logic

In digital logic circuit designs, circuits are designed using Boolean logic. However, most emerging Beyond-CMOS technologies are based on majority logic. Majority logic circuits are developed using majority gates. For a majority gate, the number of inputs to the gate is odd,

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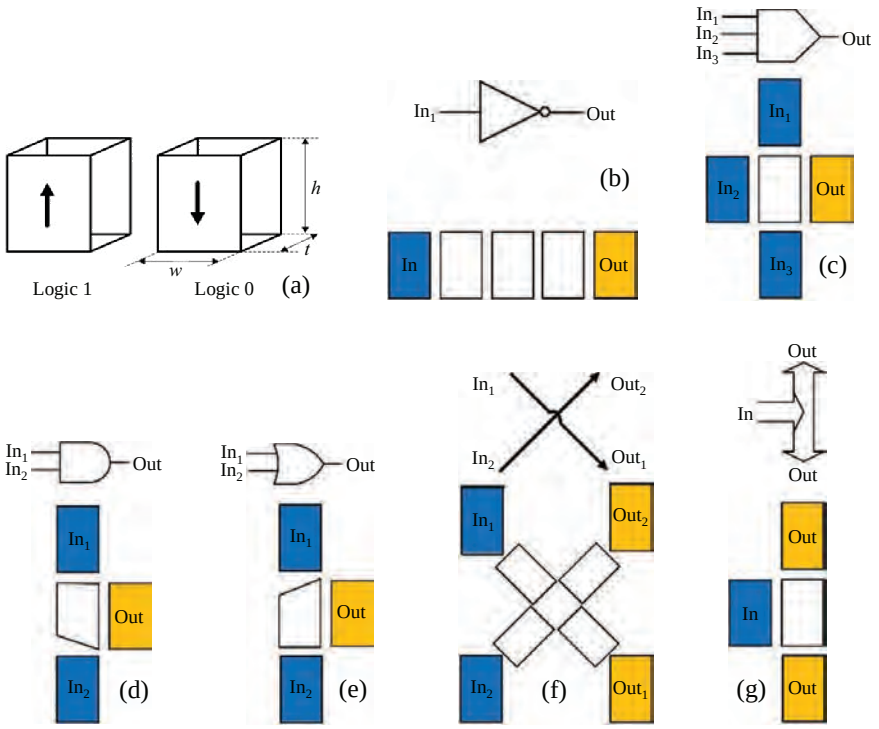
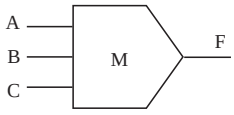


Fig. 1. iNML basic building blocks: (a) – logic, (b) – inverter, (c) – majority logic, (d) – AND gate, (e) – OR gate, (f) – wire crossing, and (g) – coupler

Table 1. Truth table of 3-input majority gate

A (fixed)	B	C	F	
0	0	0	0	AND Logic can be realized by fixing one input (A) as "0"
0	0	1	0	
0	1	0	0	
1	1	1	1	
1	0	0	0	OR Logic can be realized by fixing one input (A) as "1"
1	0	1	0	
1	1	0	0	
1	1	1	1	



and more than one input is applied to the gate. The most widely used majority gate in beyond-CMOS circuit design technologies is the 3-input majority gate, which has three inputs and one output. The output depends on the binary value that is predominantly present among the inputs. The majority gate functioning with three inputs and one output can be expressed using Boolean expressions

$$M(A,B,C) = AB + BC + AC. \tag{1}$$

The direct conversion of the Boolean expressions may increase the complexity of majority logic-based circuits. In the case of complex circuits, the majority logic can be optimised using optimisation algorithms available in the literature. The truth table of a 3-input majority gate is shown below: for Boolean logic realisation, the AND/OR gates are obtained from 3-input majority gates by fixing one input value. The majority gate can be made to function as a 2-input AND or 2-input OR gate by fixing any one of the inputs as logic "0" or logic "1", respectively, as given by (2-5).

For AND gate conversion

The Boolean expression is

$$Y = AB. \tag{2}$$

The majority logic expression is

$$Y = M(A,0,B). \tag{3}$$

For OR gate conversion

The Boolean expression is

$$Y = A + B. \tag{4}$$

The majority logic expression is

$$Y = M(A,1,B). \tag{5}$$

2.2 Nano magnetic logic (NML)

NML is a promising alternative to CMOS for the near future, as it can be used to develop various types of circuits and realised at room temperature [18-20]. A nano magnet can be encoded with binary data using its intrinsic magnetic nature. Single-domain magnets used to symbolise logic values in NML circuits are

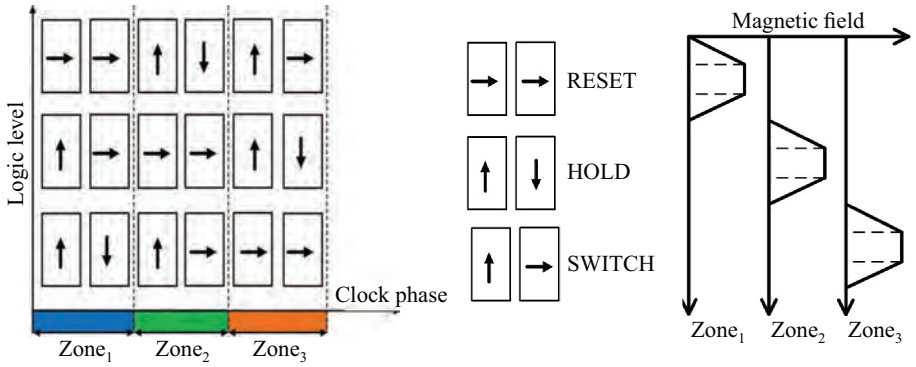


Fig. 2. iNML clock mechanism and phases

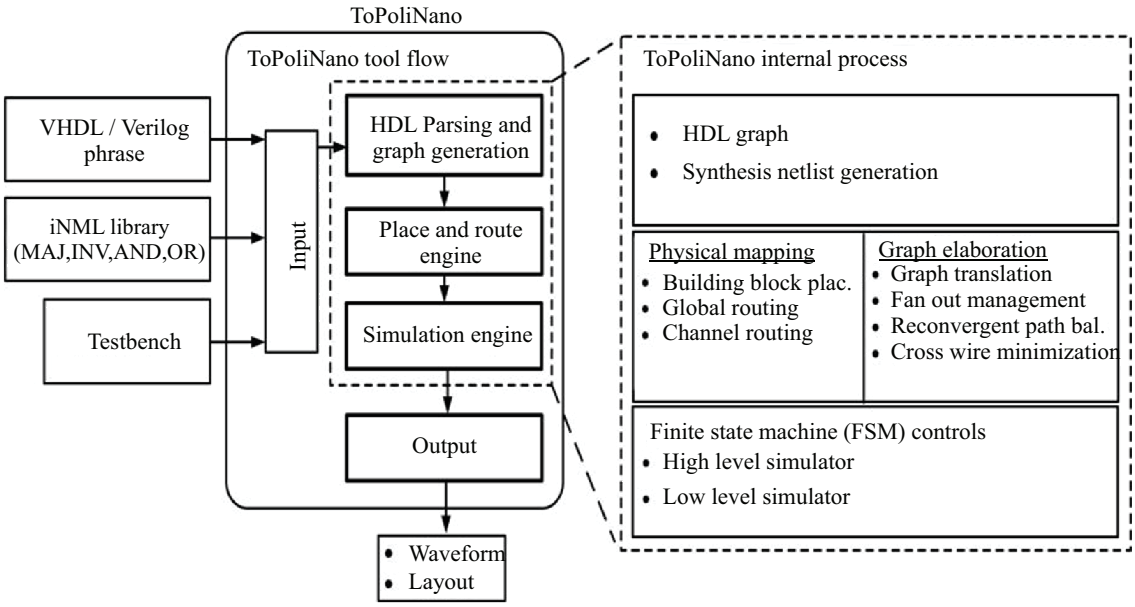


Fig. 3. iNML simulation work flow in ToPoliNano

shown in Fig. 1(a). These have two stable magnetisation states that are used to represent logic "0" and "1". Information propagation occurs between the nano magnets based on magneto-dynamic interactions. The magnets are physically realisable and can be used at room temperature owing to the shape anisotropy of rectangular magnets. The typical dimensions of the magnets height (h) × width (w) × thickness (t) considered for the realisation are $90\,\text{nm} \times 60\,\text{nm} \times 20\,\text{nm}$ and $100\,\text{nm} \times 50\,\text{nm} \times 20\,\text{nm}$, [21]. The NML circuits are classified into in-plane nano magnetic logic (iNML) and perpendicular nano magnetic logic (pNML). Boolean logic realisation can be achieved by the conversion of majority gates (MGs) to AND and OR gates as given in expressions (2-5). The realisation of the majority gates, AND gate, OR gate, coupler, wire crossing, and inverters using nano magnets are presented in Fig. 1(b) to (g). More detailed information about the fabrication of nano magnets and gates can be found in [22].

The direction of information propagation from one end to another is controlled by an external clock. Several clocking mechanisms have guaranteed correct information propagation in iNML circuits. The magnets are grouped into zones, with each clocked zone comprising four or six magnets. Each magnet can be in one of three possible states of operation depending on the clock and clock zone, as shown in Fig. 2, [23-25].

The NML circuit is separated into parts containing one or more nano magnets, and each of these areas, referred to as clock zones, receives the clock signal in varying clock phases. In the iNML circuit design, three clock zones were used with a minimum of two nano magnets in each zone.

The clock signal is applied along the horizontal direction of the nano magnets. When the clock signal drops to zero, the nano magnets will be in the SWITCH phase, and they tend to switch to their new logical states based on the state of the neighbouring nano magnets, which will be in the HOLD state. When the clock signal is zero, the nano magnets will be in the HOLD state and maintain

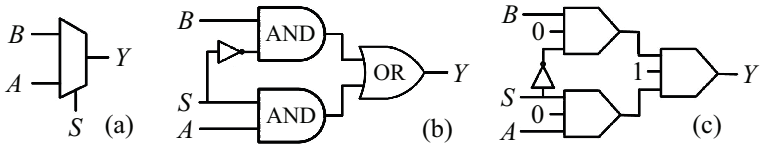


Fig. 4. Multiplexer 2×1 (a) – symbol, (b) – logic diagram of AOI gates, logic diagram of majority gates

their magnetic state. When the CLOCK signal increases from zero, the nano magnets enter the RESET mode. During the operation period, the clock zones will be in non-identical states, and they will change their state in accordance with the clock signal. By controlling the clock signal, the direction of the information flow can be controlled.

2.3 NML circuit design using ToPoliNano

The ToPoliNano tool is a widely used tool for validating iNML circuits, [26]. It has an automatic layout feature that imitates the top-down design process similar to CMOS circuit design technology. The software is capable of designing, simulating, and testing circuits based on emergent technologies. Figure 3 shows the basic flow of the tool.

The initial stage of the ToPoliNano mainstream is the parsing stage. The input VHDL files in the form of library components, VHDL descriptions, or VHDL test benches are transformed to their corresponding internal data structure. The structural VHDL description input files are synthesized using the four basic gates: inverter, and, or, and majority voter only. The synthesis tool preprocesses the behavioral VHDL description using fundamental iNML gates and extracts all necessary information. To generate the final layout, the design tool and optimisation algorithm can be selected according to the needs of the designer. The layout generation is initiated using the graph from the parser as input. The three possible iNML layout hierarchical styles in ToPoliNano are (i) – full, (ii) – flat, and (iii) – partial. To speed up the layout process, a fully hierarchical approach uses the available components in the user library.

The simulation algorithm is structured by a finite-state machine, and the information flow mechanism is controlled by a general switch algorithm. The hold, reset, and switch conditions of the clock zones are determined by the state's transition. To assess the magnetisation values, two simulation engines are available that can perform simulations at low and high levels. In the low-level simulator, dynamic relations involving two magnetic nanoparticles are expressed in accordance with the diminished Landau-Lifshitz-Gilbert (LLG) formulation equations, and the circuits' physical behaviour is characterised. In the high-level simulator, the logic behaviour of the circuit is verified. This works on the principle of ferromagnetic and antiferromagnetic interaction between nearby cells, which is limited to 8, and thereby carries out the weighted sum of the magnetisation contributions.

The layout constraints of the iNML technology are the I/O terminals located at the top and bottom boundaries of the circuit. The directionality of the signal flow from inputs to outputs is set by the adopted clock mechanism, and only a limited number of magnets can be cascaded in each clock zone. Because iNML is a planar technology, signal synchronisation and cross-wire minimisation are critical issues that can affect the performance and the final timing of the entire circuit.

3 Barrel shifter implementation

3.1 Boolean and majority logic based barrel shifter

The barrel shifter is a combinational circuit that shifts a data word by a specified number of bits in a distinct clock cycle using a control input. The important applications of barrel shifters include address decoding [27], data shifting and rotation for encryption and decryption processes [28], floating-point arithmetic for high precision, bit indexing, and variable length coding [29]. In general, barrel shifters are realised using a chain of multiplexers, with the output of one multiplexer becoming the input of the succeeding multiplexer, while maintaining a shift distance. For an n-bit word, $n \log_2 n$ multiplexers are required. Most emerging technologies use the majority logic for realisation. Nano magnets can also be used to realise majority-logic-based designs. To show that NML circuits can be used for both Boolean and majority logic-based designs, the proposed barrel shifter is realised using Boolean logic designed using and-or-inverter (AOI) gates and majority gates. To reduce the complexity of the implementation for majority logic NML realisation, Boolean expressions are converted to majority logic expressions for effective realisation.

The Boolean (AOI) expression for a 2 to 1 multiplexer is

$$Y = AS + B\overline{S}. \tag{6}$$

The equivalent majority logic expression for a multiplexer using a 3-input majority gate is

$$Y = M((A, 0, S), 1, M(B, 0, \overline{S})), \tag{7}$$

where, M represents the majority logic operation as described by (1). Figure 4 shows the difference in the realisation of the multiplexer using AOI and majority gates.

The barrel shifter can perform different operations as presented in Tab. 2.

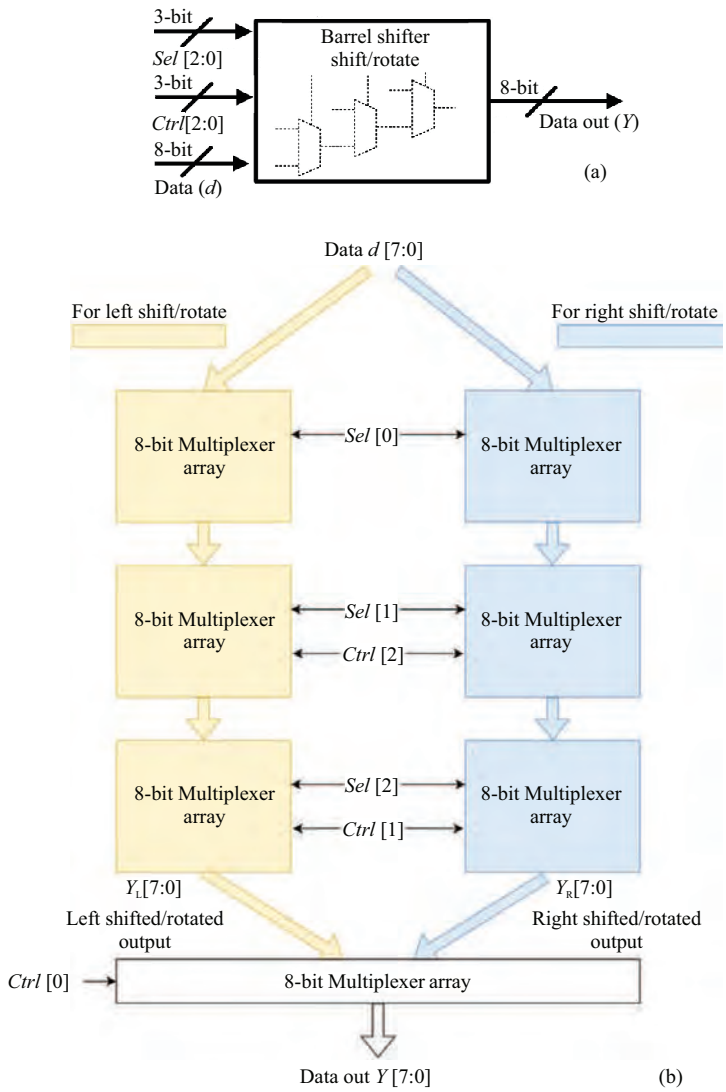


Fig. 5. 8-bit bidirectional barrel shifter (a) – input and output, (b) – block diagram

Table 2. Modes of Barrel shifter operations: A-aritmetic, L-logical, direction: R-right, L-left

Opcode/control input			
Direction (R/L) Ctrl (0)	Operation (rotate/shift) Ctrl (1)	Shift type A_s/L_s Ctrl (2)	Function
0 (right)	0	0	R shift L
		1	R shift A
	1	0	R rotate
		1	
1 (left)	0	0	L shift L
		1	L shift A
	1	0	L rotate
		1	

The $Ctrl[0]$ signal determines the selection of right/left rotated/shifted output. The $Ctrl[1]$ signal determines whether rotate or shift operation will be performed, and $Ctrl[2]$ determines whether the shift operation will be an arithmetic shift (A_s) or logical shift (L_s) operation.

The realisation of a barrel shifter operations, as discussed in Tab. 2, is performed using multiplexers. In this work, an 8-bit barrel shifter is realised using both the AOI and the majority gates. The general block view of the 8-bit barrel shifter with inputs and outputs is shown in Fig. 5(a). In general, a barrel shifter that shifts in only one direction will have "n" rows of multiplexer for a 2^n input barrel shifter. Each row of the multiplexer will be connected to one of the Sel lines and the output will depend upon the value of the Sel lines. The proposed 8-bit barrel shifter performs bidirectional shifting as well as rotate operation. Hence, two parallel blocks of 8-bit single directional blocks are used. The $d[7:0]$ is applied to both blocks. One block will perform the left shift/rotate operation. One block will perform the right shift/rotate operation. Each block has three rows of multiplexer and each row has 8 multiplexers in it. Three Sel lines $Sel[2:0]$ is used to control the shift amount and the inputs applied at the different rows of the multiplexer are controlled by the Ctrl signals. The $Ctrl[2:0]$ inputs determine the

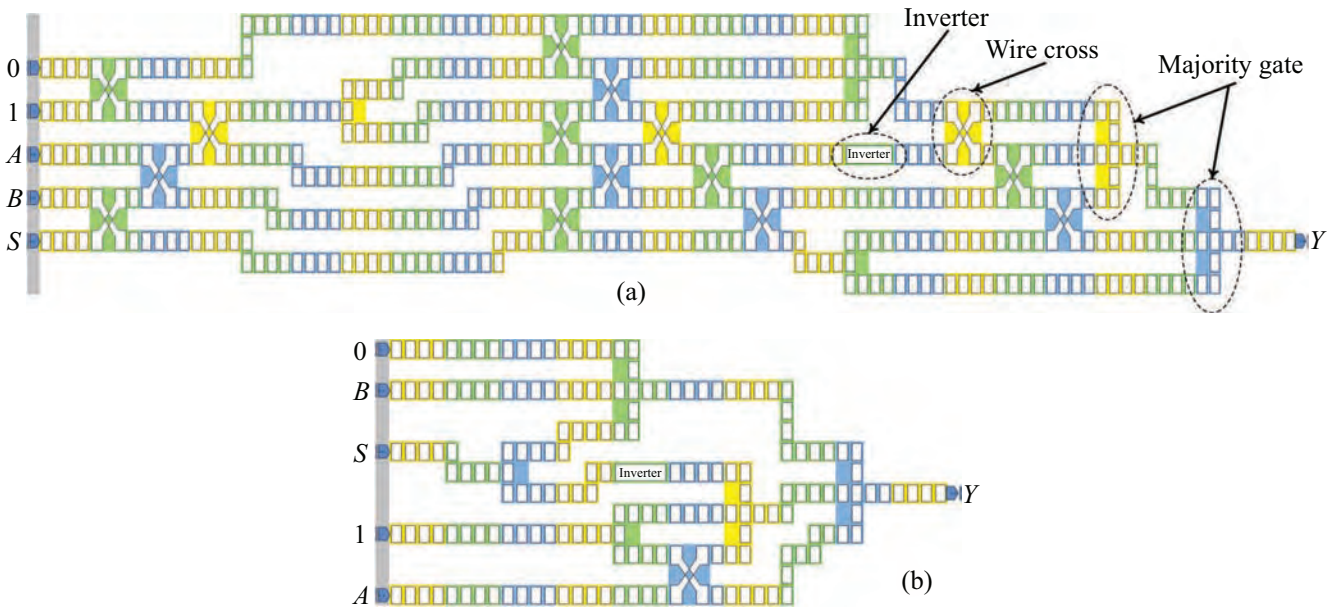


Fig. 6. iNML majority logic based multiplexer 2 × 1 (a) – fully hierarchy without algorithm, (b) – fully hierarchy with algorithm

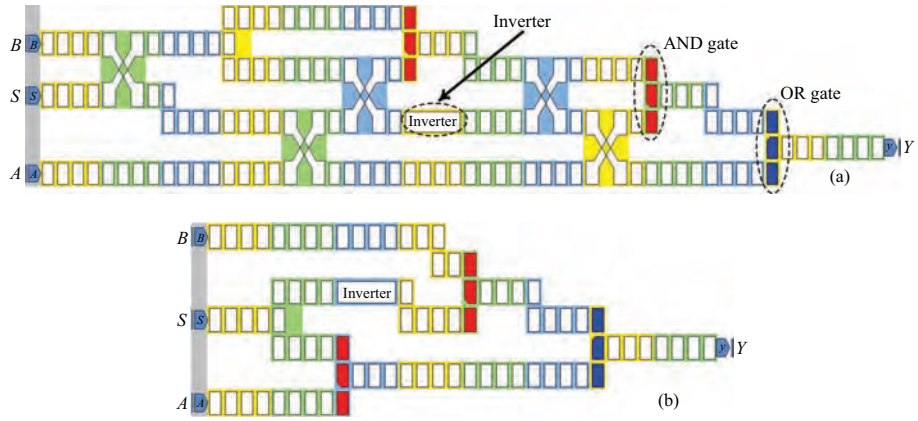


Fig. 7. iNML AOI logic based multiplexer 2 × 1 (a) – fully hierarchy without algorithm, (b) – fully hierarchy with algorithm

Table 3. Cross wire reduction algorithms for 8-bit barrel shifter, AOI and majority

Design methods		Barrel shifter-AOI layout fully hierarchical					Barrel shifter-majority logic layout fully hierarchical				
		-	BC	KL	BC-KL	KL-BC	-	BC	KL	BC-KL	KL-BC
Fan-out control	Before	214	214	214	214	214	216	216	216	216	216
	After	433	433	433	433	433	624	624	624	624	624
Reconvergent path balance		1115	1115	1115	1115	1115	2353	2353	2353	2353	2353
Number of crossings	Initial	9656	9656	9656	9656	9653	31842	31842	31842	31842	31842
	after BFS	-	4137	4137	4137	4137	-	18634	18634	18634	18634
	after BC	-	2647	-	2647	2506	-	13151	-	13151	13129
	after KL	-	-	4063	2521	4063	-	-	17609	12144	17609
height × width		252 × 5808	265 × 5028	364 × 6064	324 × 6460	309 × 4840	569 × 14756	481 × 13104	781 × 13024	508 × 12112	486 × 15732
Total no of magnets		388005	315276	407375	408454	298864	1957061	1769037	1792134	1571485	2200465
Clock zones		1452	1257	1516	1615	1210	3689	3276	3656	3028	3933

Table 4. Comparison of multiplexer and barrel shifter design in synopsys design vision using ToPoliNano QCA technology truth table of 3-input majority gate

Design		Multiplexer		Barrel shifter	
		AOI	Majority logic	AOI	Majority logic
Gates		2 AND 2 OR 1 inverter	3 majority gate 1 inverter	108 AND 78 OR 5 inverter	186 majority gate 5 inverter
Area (μm^2)		13509	84	837045	4650
Power (μW)	Internal	0	0	0	0
	Switching	0.375	0.375	44.05	4.4.05
Active power product (μm^2 mW)		5.07	0. 032	36871	205
Instance		5	4	191	191

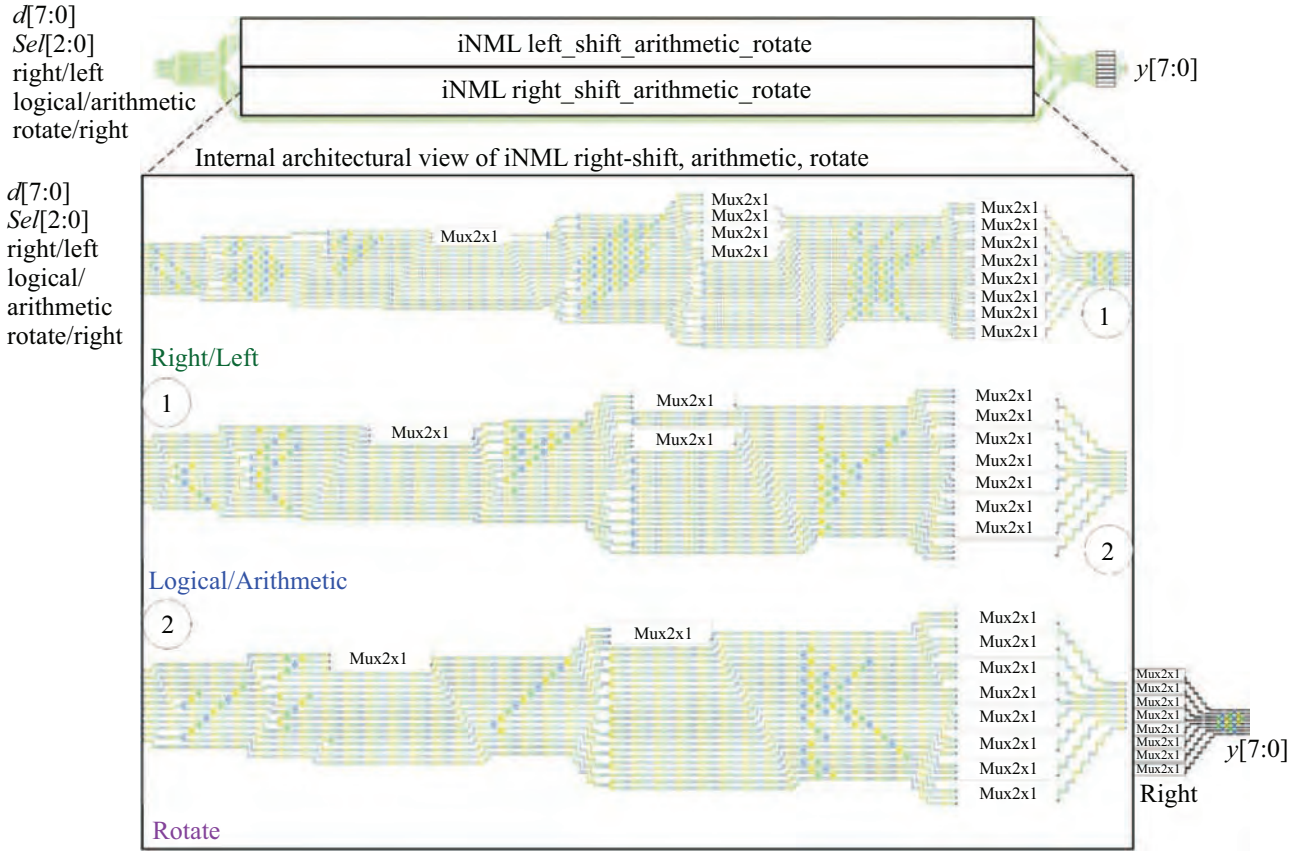


Fig. 8. iNML view of 8-bit bidirectional barrel shifter physical design

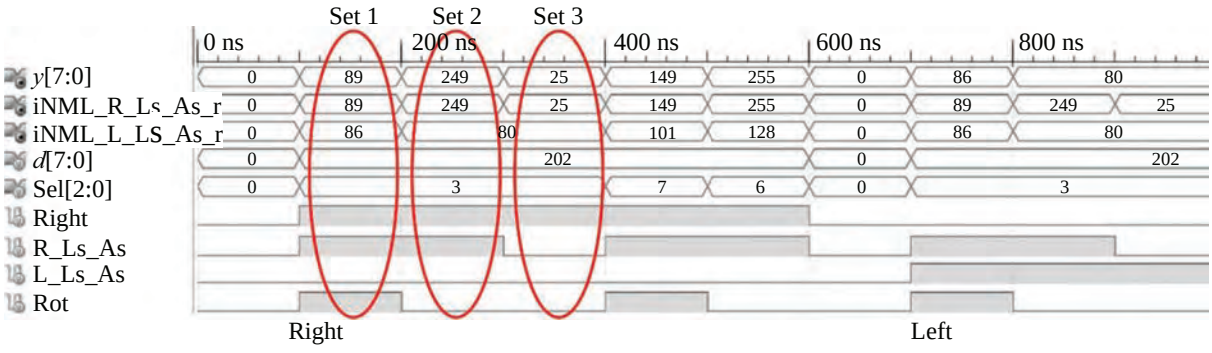


Fig. 9. 8-bit barrel shifter simulation results

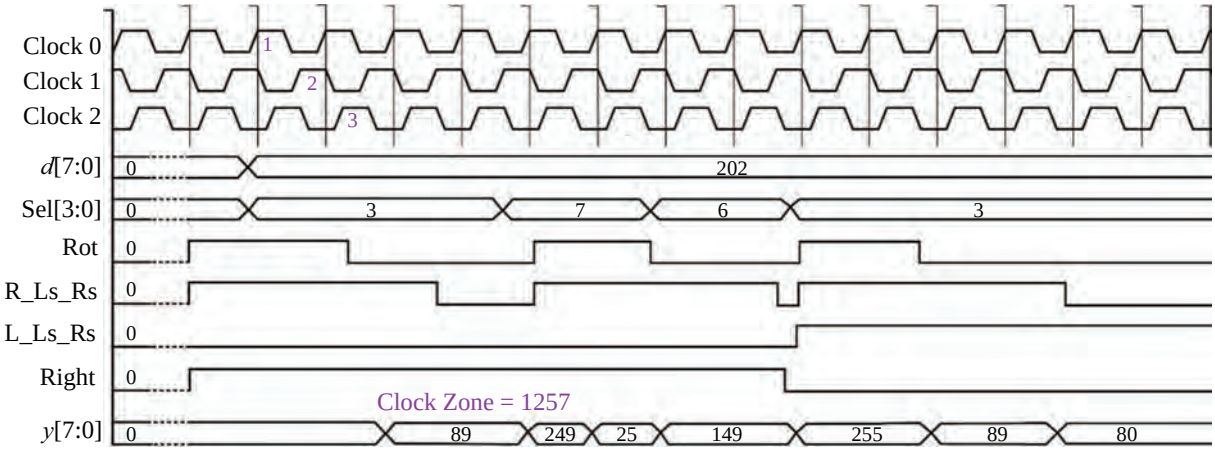


Fig. 10. 8-bit iNML AOI barrel shifter physical layout simulation results

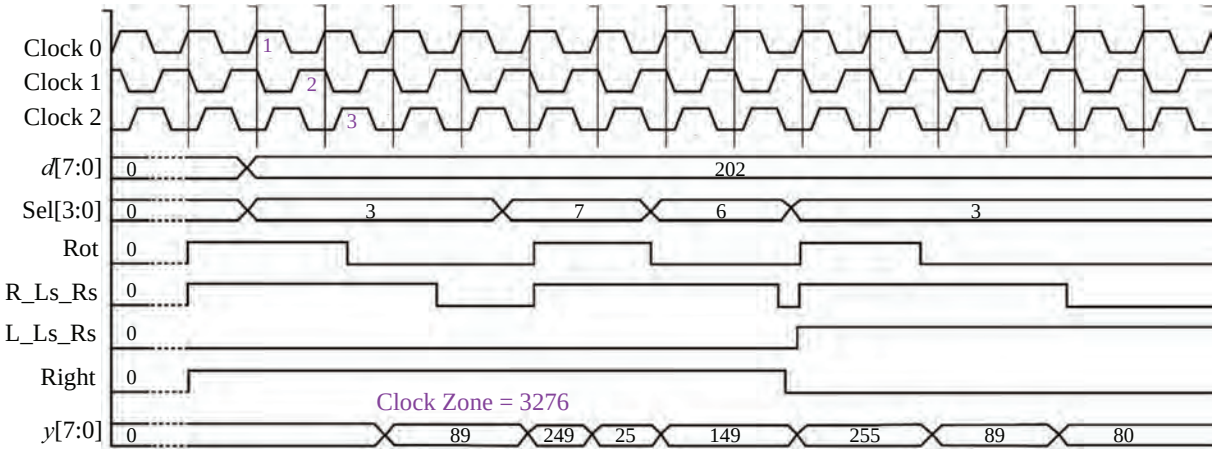


Fig. 11. 8-bit iNML majority logic based barrel shifter physical layout simulation results

direction, arithmetic shift, logical Shift and rotate operation as mentioned in Tab. 2. Compared to the single directional barrel shifter, the inputs applied to the multiplexers in each row of the multiplexer are controlled by the $Ctrl$ and Sel signals. The block diagram representing the operation of the proposed barrel shifter is presented in Fig. 5(b),

$$y[n] = \overline{Ctrl[0]}Y_R[n] + CtrlY_L[n]), \tag{8}$$

where, $YL[n]$ represents the output generated for the n-th bit based on the $Ctrl[1]$ and $Ctrl[2]$ signals with left shift/rotate operations.

3.2 Implementation

Typical dimensions of 90 nm × 60 nm × 20 nm were used in the proposed design realisation, using default simulation settings in ToPoliNano. Both the AOI and majority logic designs were designed and validated using the same design methodology. The physical layout of the multiplexer was realized using a full-hierarchy design approach. Both realisations were obtained with and without the wire-crossing optimisation algorithm available with ToPoliNano, and are shown in Fig. 6 and Fig. 7, which clearly show the area occupation and gates present in the layout. While implementing an algorithm-based approach, the number of clock zones and the size of the area boundaries are optimised, and the barrel shifters using AOI and majority logic are developed using the respective logic-based multiplexers. Figure 8 shows the iNML circuit realisation of the 8-bit bidirectional barrel shifter using majority logic.

4 Performance evaluation

The ToPoliNano tool and ModelSim tool were used to simulate and validate the proposed majority and AOI designs. The simulation results of an 8-bit bidirectional barrel shifter using majority gates are shown in Fig. 9. The first set of inputs for the simulation corresponds to $d[7:0] = 11001010(202)$; $Sel[2:0] = 011$, $right = 1$, $arithmetic = 1, rotate = 1$, and the output is product $Y[7:0] = 01011001(89)$. The second set of in-

puts corresponds to $Sel[2:0] = 011$, $right = 1$, $arithmetic = 1, rotate = 0$, and the output is product $Y[7:0] = 11111001(249)$. The third set of inputs corresponds to $d[7:0] = 11001010(202)$; $Sel[2:0] = 011$, $right = 1$, $arithmetic = 0, rotate = 0$, and the output is product $Y[7:0] = 00011001(25)$.

4.1 iNML physical results

To optimise the designs, different combinations of algorithms such as Kernighnan-Lin (KL) and Barycentre (BC) are available in ToPoliNano. The time complexity and other constraints are varied based on the bit size of the design. Better optimisation can be obtained by combining the breadth-first search (BFS) with various combinations of algorithms. Table 3 clearly shows the impact of the optimisation algorithms on the fan-out control, wire crossings, area, clock zones, and number of magnets used in the AOI and majority gate-based designs. To show that both the designs performed the same logical operations, the physical layout simulation results of the proposed barrel shifter using AOI and majority logic after applying the BC algorithm are presented in Fig. 10 and Fig. 11, respectively.

The post-layout simulation output depends on the optimization algorithm applied to the design. To ensure a fair comparison, the BC algorithm is applied to both the designs of the barrel shifter. From Fig. 10 and Fig. 11, it can be observed that the AOI and majority logic designs have identical outputs, but their delay varies owing to the difference in the logic, which can be found through the values presented in Tab. 3.

4.2 ASIC synthesis results

For a fair assessment, a 2-to-1 multiplexer and 8-bit bidirectional barrel shifter with AOI and majority were implemented on nano magnetic QCA technology in Synopsys EDA provided by ToPoliNano and compared in Tab. 4. The comparison was made for the number of gates used in the design, number of instances, area, power, and area-power product.

It can be observed from the table that the majority logic-based design consumes less area delay product compared to the AOI design. Furthermore, this proposed barrel shifter design would be widely useful for a variety of diversified applications in the field of electronics and communications.

5 Conclusion

The increasing difficulties in transistor fabrication have shifted the focus to beyond-CMOS technologies. Nano magnets are an attractive option for designing high-performance, beyond-CMOS circuits. Compared to combinational circuits, very few sequential circuits are realised using NML. In this work, a barrel shifter was designed using NML and validated using the ToPoliNano tool. The proposed design is the first of its kind in iNML realisation. To showcase the ability of nano magnets to support both AOI and majority gate-based logic, the Barrel shifter was realised using both AOI and majority logic. The iNML circuit developed in ToPoliNano was optimised using several optimisation algorithms. The functional equivalence of both designs was verified and validated after generating the layout. The proposed designs were also validated using the QCA library files developed by ToPoliNano in the synopsis EDA tool, to compare the performance of AOI and the majority logic-based barrel shifter design.

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