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PAPERS

An EMI susceptibility study of different integrated operational transconductance amplifiers

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This paper presents a comparative EMI susceptibility study of different integrated operational transconductance amplifier (OTA) topologies. We analyzed conventional well-known amplifier topologies based on the Miller OTA and folded cascode concepts with lower power consumption. The output dc voltage shifts induced by power supply and input common mode high frequency disturbances are presented. On top of the EMI susceptibility comparison, we discuss PSRR and CMRR within large and small excitation signal with a new simulation setup. Even more, the back-gate connections of differential MOS pair in OTA input stage are investigated for EMI susceptibility impact as well.

K e y w o r d s: CMRR, common mode, dc voltage shift, EMC, EMI, folded cascode, HF immunity, low power, Miller, operational transconductance amplifier, OTA, open loop gain, PSRR

1 Introduction

Many analog or mixed-signal integrated circuits (ICs) use integrated operational transconductance amplifiers (OTAs), such as the Miller OTA for example. The OTA transfers differential input voltage to output current and suppress input common mode voltage ideally independent of power supply, loading, temperature, and process variations. As an interesting fact, the abbreviation operational amplifier was firstly published in 1947 within electronic circuits for analysis of problems in flight dynamics of airplane [1]. The smaller size, lower power consumption, higher density when combined with the increasing advent of high-speed mixed-signal and radio frequency (RF) devices may result in serious EMC issues. For example, in electromagnetic emission (EME) and electromagnetic susceptibility (EMS), more attention needs to be paid [2]. In most cases, the main Achilles heel in an analog circuit could be the OTA from this perspective. We consider that influence analysis of EMI susceptibility on basic OTA topologies is a vital task. Many articles focus on fully differential and symmetrical operational amplifier topologies within different types of RF disturbances [3] - [7]. From these references, we can formulate that if the OTA is fully symmetrical and rectification effects are also symmetrical, then EMI effects will be suppressed. We decided to analyze symmetrical input to single ended output OTA topologies. Within the automotive requirements, the following criteria were selected for the analysis of the basic OTA topologies: open loop gain with circuit stability over wide temperature range from $-50\,°\mathrm{C}$ to $200\,°\mathrm{C}$, and low EMI susceptibility over wide high frequency (HF) range from 100 kHz to 1 GHz. The rest of this paper is organized as follows. The basic integrated OTA topologies are described in Section 2. Section 3 contains the investigation of integrated OTA topologies including simulation setups and results. Finally, Section 4 concludes the paper.

2 Integrated OTAs

The main principle of OTAs is to transfer input differential voltage to output current. The input common mode voltage is ideally completely suppressed. The following basic equation describes the OTA output current

$$i_{\mathrm{OUT}} = (v_{\mathrm{INP}} - v_{\mathrm{INN}})gm_{\mathrm{Diff}} + \frac{v_{\mathrm{INP}} + v_{\mathrm{INN}}}{2} gm_{\mathrm{CM}}, \quad (1)$$

where gm_{Diff} is a differential transconductance and gm_{CM} is a common mode transconductance which is ideally equal to zero. At the output of the OTA, we can see an output voltage due to OTA output resistance r_{OUT} as follows

$$v_{\mathrm{OUT}} = i_{\mathrm{OUT}} r_{\mathrm{OUT}}. \quad (2)$$

The OTA output resistance has ideally infinite value. In reality, the value is defined by the output resistance of the output transistors which forms an OTA output stage. We can say that the OTA has differential voltage amplification A_{Diff} and common mode voltage amplification A_{CM} which are described by the following equations

$$A_{\mathrm{Diff}} = r_{\mathrm{OUT}} gm_{\mathrm{Diff}}, \quad (3)$$

$$A_{\mathrm{CM}} = r_{\mathrm{OUT}} gm_{\mathrm{CM}}. \quad (4)$$

From above mentioned equations, we would like to maximize the gm_{Diff} and minimize gm_{CM} to obtain a

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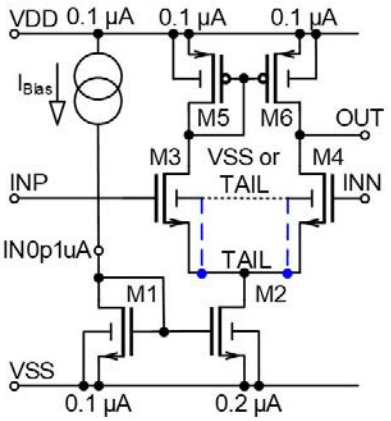

Fig. 1. Simple NMOS OTA

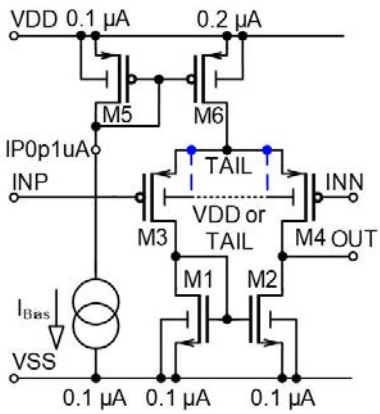

Fig. 2. Simple PMOS OTA

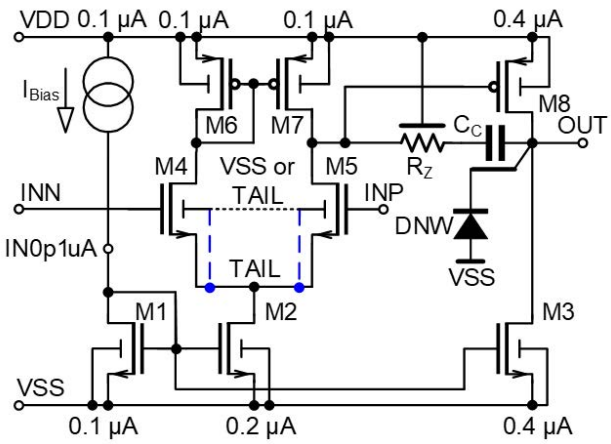

Fig. 3. Miller PPDAL OTA

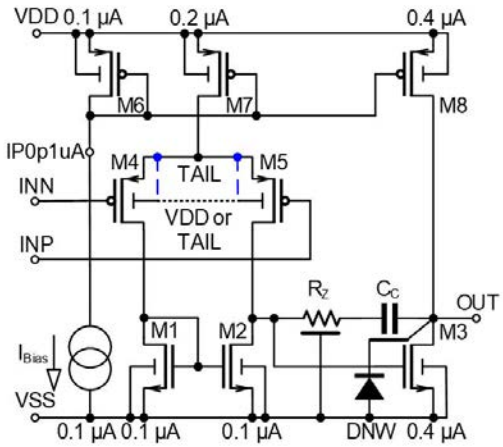

Fig. 4. Miller NPDAL OTA

nearly ideal OTA with high A_{Diff} gain in the design. We can achieve it by maximizing the intrinsic output resistance of a MOS transistor, which is given by the following equation

$$r_{\mathrm{OUT\_Mx}} = \frac{1}{\lambda I_{\mathrm{D\_Mx}}}, \tag{5}$$

where $I_{\mathrm{D\_Mx}}$ is the drain pinch-off current and λ is the channel length modulation factor. Within weak inversion, we can write the following equation for MOS drain current

$$I_{\mathrm{D\_Mx}} = \frac{W}{L} I_0 \exp\Big(\frac{V_{\mathrm{GS\_Mx}}}{nV_T}\Big). \tag{6}$$

In (6), W and L are width and length of MOS channel. The I_0 is a dc current when an aspect ratio W/L is equal to one and gate-source voltage $V_{\mathrm{GS\_Mx}}$ is equal to zero volts. The n is the subthreshold slope factor given by $1 + C_{\mathrm{D}}/C_{\mathrm{OX}}$, where C_{D} is the channel-bulk depletion capacitance and C_{OX} is the gate-oxide capacitance. Typical values of n are in the range from 1.3 to 1.5. The V_{T} is the well-known thermal voltage which is directly proportional to temperature T, $V_{\mathrm{T}} = kT/q$. From these equations, it can be seen that the drain current I_{D_Mx} is not dependent on the threshold voltage V_{TH} of the MOS transistor and temperature is an important design parameter in weak or moderate inversion circuits. Moderate inversion occurs when the effective voltage $V_{\mathrm{GS}} - V_{\mathrm{TH}}$ is less than 80 mV. Weak inversion occurs when the effective voltage is less than 20 mV. These two regions offer high gain with low power consumption, but they are not generally used due to low speed [8].

In this paper, we do not need high speed OTAs and therefore we are focusing on low speed, for all practical purposes, dc operation OTAs. We chose a bias current 100 nA with respect to leakage current that rises from 1 nA to tens of nA in the temperature range from 150 °C up to 200 °C. All proposed OTAs are designed in a 180 nm BCD technology.

2.1 Simple NMOS OTA

There are several well-known basic topologies for OTAs. The first chosen basic topology is a simple OTA with NMOS differential pair, which is shown in Fig. 1.

This simple OTA consists of NMOS differential pair, M3 and M4, based on the topology known since 1947 [9] with a PMOS current mirror, M5 and M6, which acts as an active load. The NMOS differential pair is supplied by an NMOS current mirror, M1 and M2, that sets an OTA operating point. Our study includes a connection

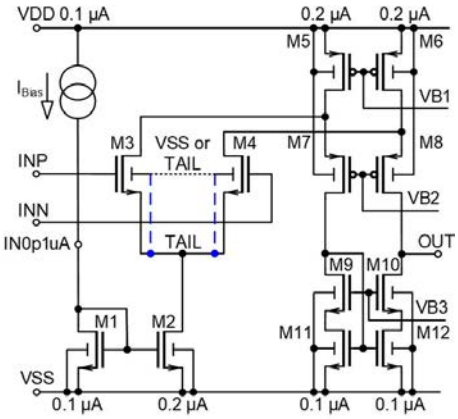

Fig. 5. Folded NMOS cascode OTA

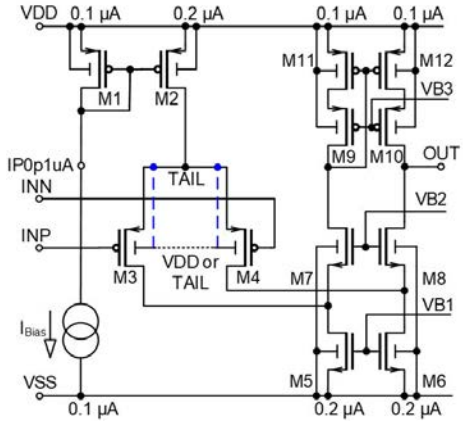

Fig. 6. Folded PMOS cascode OTA

effect of input differential pair back-gates where we expect influence on EMI susceptibility. Therefore, we depicted classical connection of the back-gates by pointed line and connection to TAIL node by dashed line in OTA circuits.

2.2 Simple PMOS OTA

The second chosen topology is the simple OTA with PMOS differential pair as opposite topology to the simple NMOS OTA. The OTA is shown in Fig. 2

This simple OTA consists of PMOS differential pair M3 and M4 with the NMOS current mirror M1 and M2 which acts as the active load. The PMOS differential pair is supplied by the PMOS current mirror M5 and M6 that sets the OTA operating point.

2.3 Miller PPDAL OTA

The third chosen topology is well-known Miller OTA with an output PMOS pass device loaded by active load (PPDAL). The Miller PPDAL OTA is shown in Fig. 3.

This Miller PPDAL OTA consists of two stages. The first stage is the NMOS differential pair M4 and M5 with the PMOS active load M6 and M7. The second stage consists of PMOS pass device M8 with active load M3 which is a part of the NMOS current mirror M1, M2 and M3. This current mirror sets operating points of both stages.

Due to two stages topology, there is a frequency compensation by an internal dominant pole. The internal dominant pole is set by a Miller capacitance, whose value includes the OTA second stage gain with a CC MOS type compensation capacitor placed in an N-type well. This well is depicted as a DNW diode. The same effect, which was firstly published by John M. Miller in 1920 [10] is used there. The C_{C} capacity is amplified by M8 and is a part of an input impedance of the OTA second stage. Additionally, there is an R_{Z} resistor with a higher value than $1/gm_{\mathrm{M8}}$ to maintain a frequency zero position on the left side of the Laplace complex plane which would result in a wanted signal phase.

2.4 Miller NPDAL OTA

The fourth chosen topology is Miller OTA with an output NMOS pass device loaded by active load (NPDAL) as opposite topology to the Miller PPDAL OTA. The Miller NPDAL OTA is shown in Fig. 4.

This Miller NPDAL OTA consists of two stages. The first stage is the PMOS differential pair M4 and M5 with the NMOS active load M1 and M2. The second stage consists of NMOS pass device M3 with active load M8 which is a part of the PMOS current mirror M6, M7 and M8. This current mirror sets operating points of both stages. There is the same internal frequency compensation as for the Miller PPDAL OTA in section 2.3.

2.5 Folded NMOS cascode OTA

The fifth chosen topology is well-known folded NMOS cascode OTA with NMOS input differential pair. This OTA is shown in Fig. 5

This folded cascode OTA consists of one stage even though it appears that there are two stages. The one stage includes the NMOS differential pair M3 and M4 with the PMOS active load M5 and M6 and cascode transistors M7 and M8 with its active load M9 - M12 as a cascoded current mirror. The NMOS differential pair is supplied by an NMOS current mirror M1 and M2 that sets an OTA operating point. The main advantages of this topology, besides high voltage gain, are frequency stability over wide frequency range without internal frequency compensation and symmetrical loading of the differential pair.

2.6 Folded PMOS cascode OTA

Finally, the sixth chosen topology is folded PMOS cascode OTA with PMOS input differential pair as opposite topology to Folded NMOS cascode OTA. The folded PMOS cascode OTA is shown in Fig. 6

This one stage folded PMOS cascode OTA includes the PMOS differential pair M3 and M4 with the NMOS active load M5 and M6 and cascode transistors M7 and M8 with its active load M9 - M12 as the cascoded current mirror. The PMOS differential pair is supplied by the

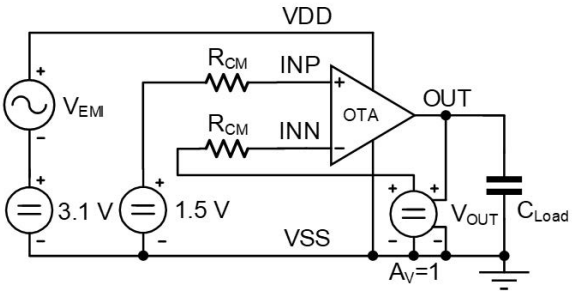

Fig. 7. The OTA supply EMI susceptibility simulation schematic with the isolated output

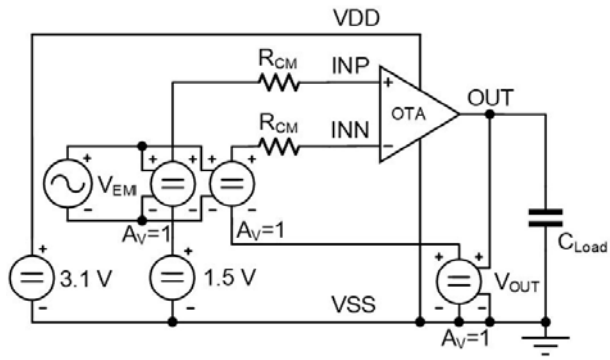

Fig. 8. The OTA input common mode EMI simulation schematic with the isolated output

Table 1. Typical basic parameters of all proposed OTAs

OTA topology	Offset 6σ (mV)	$A_{\text{Diff\_OL}}$ (dB)	f_{DP} (Hz)	UGBW (kHz)	PM (deg)
a) Simple NMOS	8.6	58.0	457.2	360.2	85.4
b) Simple PMOS	7.5	63.4	188.8	271.3	81.4
c) Miller PPDAL	7.8	121.9	0.1	132.7	61.8
d) Miller NPDAL	7.4	122.4	0.2	237.0	64.2
e) Folded NMOS*	8.4	111.7	0.9	360.7	71.5
f) Folded PMOS*	8.9	109.2	1.0	277.6	71.1

* cascode

Table 2. Variations of basic parameters of all proposed OTAs within 512 Monte-Carlo runs

OTA topology	$A_{\text{Diff\_OL}}$ 6σ (dB)	f_{DP} 6σ (%)	UGBW 6σ (%)	PM 6σ (%)
a) Simple NMOS	0.2	8.1	7.9	0.7
b) Simple PMOS	0.3	5.0	3.8	1.1
c) Miller PPDAL	0.4	17.9	14.7	10.6
d) Miller NPDAL	0.4	14.4	14.1	6.7
e) Folded NMOS*	0.7	5.8	7.2	2.3
f) Folded PMOS*	0.4	4.1	2.8	1.5

* cascode

Table 3. Variations of basic parameters of all proposed OTAs within junction temperature from -50 to 200 °C

OTA topology	$\Delta A_{\text{Diff\_OL}}$ (dB)	Δf_{DP} (%)	ΔUGBW (%)	ΔPM (%)
a) Simple NMOS	5.6	2.9	61.8	1.4
b) Simple PMOS	3.7	8.6	48.1	0.4
c) Miller PPDAL	7.4	16.6	63.7	2.7
d) Miller NPDAL	9.9	76.2	44.7	21.6
e) Folded NMOS*	9.0	43.3	62.3	4.6
f) Folded PMOS*	7.9	48.7	47.9	1.4

* cascode

PMOS current mirror M1 and M2 that sets the OTA operating point.

3 Investigations of the OTAs

The investigations of the chosen OTA topologies contain analysis of basic parameters. The analysis also includes dc output voltage shift and power supply rejection ratio (PSRR) induced by small and large supply EMI. Also included is the dc output voltage shift and input common mode rejection ratio (CMRR) induced by small and large signal input common mode EMI.

3.1 OTA basic parameters

We analyzed each of the chosen OTA structures for its ac open loop gain characteristic and input random offset. We chose C_{Load} load capacitor 1 pF representing on-chip load only. According to the OTA open loop gain simulation results, all OTAs are frequency stable with sufficient open loop gains. Table 1 and Tab. 2 show basic parameters of all proposed OTAs under typical conditions: $V_{\text{DD}} = 3.1\,\text{V}$, temperature $= 27\,°\text{C}$.

All OTAs presented have acceptable random input offset less than 10 mV and UGBW higher than 100 kHz. Additionally, the mismatch and process Monte-Carlo simulation with 512 runs shows low variations. The simple NMOS and PMOS OTAs have small open loop gains which impact a systematic input offset. The Miller PPDAL, Miller NPDAL, folded NMOS and PMOS cascode have much higher open loop gains, which results in a low input differential voltage and better linearity. If we considered that the input differential voltage can be 1 mV for 1.5 V output voltage within OTA as the voltage follower, then the open loop gain shall be higher than

$$A_{\text{Diff\_OL}} = 20 \log \frac{v_{\text{OUT}}}{v_{\text{DiffIN}}} = 63.5\,\text{d}B. \tag{7}$$

We also investigated the basic parameters for all proposed OTAs in the junction temperature range from -50 to 200 °C. Table 3 shows the temperature variations.

The temperature variation of open loop gain is higher than its mismatch and process variation because the weak inversion of a MOS transistor is more temperature dependent than the strong inversion, which is generally more sensitive to process variation. The resulting temperature dependencies are not critical for a dc application.

3.2 The OTA supply EMI susceptibility

We analyzed the OTA supply EMI susceptibility by using the simulation schematic shown in Fig. 7.

We chose the OTA connection as a non-inverting voltage follower with 1.5 V dc input voltage and 3.1 V dc supply voltage. The V_{EMI} is a sine wave voltage source with a sweeping frequency f for EMI susceptibility investigations. The R_{CM} input common mode resistors are chosen with a value of 100 kOhm as ideally IC internal impedances. It must be noted that the C_{Load} load capacitor is 1 pF representing the on-chip load like for the simulations of the OTA basic parameters. We performed EMI susceptibility simulations with a 1 V peak sine wave, especially as transient envelope analysis with the Cadence Spectre RF simulator. After circuit settling, all simulation results are post-processed for the dc shift and the first ac harmonic for each OTA cell. We performed standard small signal ac simulation as well.

3.3 Power supply rejection ratio

We also analyzed large and small signal power supply rejection ratio (PSRR) of each OTA cell within the supply EMI susceptibility simulations. We calculated the output PSRR of each OTA from the first harmonic voltage amplitude using the following equation

$$PSRR = 20 \log \frac{\Delta V_{\mathrm{VDD}}}{\Delta V_{\mathrm{OUT}}}, \tag{8}$$

where ΔV_{VDD} is a change of the VDD supply and ΔV_{OUT} is a change of the output voltage. We consider these changes as the first harmonic voltage amplitude as in [11].

3.4 The common mode EMI susceptibility

We analyzed the OTA input common mode EMI susceptibility by using the simulation schematic shown in Fig. 8.

We used the same OTA connection as in the supply EMI susceptibility analysis (see section 3.2) with an input common mode ac excitation as in [12]. This excitation has the R_{CM} input common mode resistors with the value of 100 kOhm as ideally IC internal impedances. It must be noted that the C_{Load} load capacitor is 1 pF representing on chip load only. We performed input common mode EMI susceptibility simulations with 1 V peak sine wave, especially as transient envelope analysis by the Cadence Spectre RF simulator. After circuit settling, all simulation results are post-processed for the dc shift and the first ac harmonic for each OTA cell. We performed standard small signal ac simulation as well.

3.5 Input common mode rejection ratio

We analyzed large and small signal input common mode rejection ratio (CMRR) of each OTA cell within input common mode EMI susceptibility simulations. The CMRR of each OTA is calculated from the first harmonic voltage amplitudes using the following equation

$$CMRR = 20 \log \frac{\Delta V_{\mathrm{INCM}}}{\Delta V_{\mathrm{OUT}}}, \tag{9}$$

where ΔV_{INCM} is a change of the input common mode and ΔV_{OUT} is a change of the output voltage. We consider these changes as the first harmonic voltage amplitudes as in chapter 3.3.

3.6 EMI susceptibility results

The achieved results of the OTA EMI susceptibility simulations are shown as graphs (Fig. 9 to Fig. 32) in the following pages. We chose these graph arrangements for clear comparison reasons. It is possible to easily compare the simple NMOS OTA with the simple PMOS OTA, the Miller PPDAL OTA with the Miller NPDAL OTA and the folded NMOS cascode OTA with the folded PMOS cascode OTA.

The simple NMOS OTA and the simple PMOS OTA graphs (Fig. 9 to Fig. 16) show that the simple NMOS OTA with classically connected back-gates of the input differential NMOS pair has lower supply EMI susceptibility. On the other hand, the simple PMOS OTA with back-gates connected to differential TAIL node of the input differential PMOS pair has lower supply EMI susceptibility as well. The classical back-gate connection of the PMOS input differential pair to VDD supply shows higher supply EMI susceptibility due to supply EMI coupling to the simple PMOS OTA input stage. The classical back-gate connection of the NMOS input differential pair to VSS ground shows lower supply and input common mode EMI susceptibilities due to the higher EMI decoupling effect in the simple NMOS OTA input stage. The small and large signal PSRRs of the simple NMOS OTA are nearly identical, but the small and large signal CMRRs are different especially in the low frequency range up to 100 MHz. The small and large signal PSRRs of the simple PMOS OTA are different due to input stage operating point change which is not seen for the ac small signal analysis within frequency domain, but the change can be seen for analysis in the time domain with a large signal. We do not show changes in OTA operation points such as changes of bias currents due to the intended scope of this paper. The Miller PPDAL OTA and the Miller NPDAL OTA graphs (Fig. 17 to Fig. 24) show supply EMI susceptibility weakness of the Miller PPDAL OTA due to the coupling effect of the C_{C} compensation capacitor with R_{Z} resistor (see Fig. 3) of the output PMOS pass device. There is partial coupling supply EMI via a well of R_{Z} resistor and partially via C_{C} capacitor. Even more, the C_{C} capacitor makes an ac short between output and input of the PMOS pass device which acts like a diode in a dedicated frequency range. If we put the well of the R_{Z} resistor from VDD supply to VSS ground, then the supply EMI susceptibility is slightly lower and maximum dc output shift decreases from 99% to 25% for example. On the other hand, the Miller NPDAL OTA with back-gates

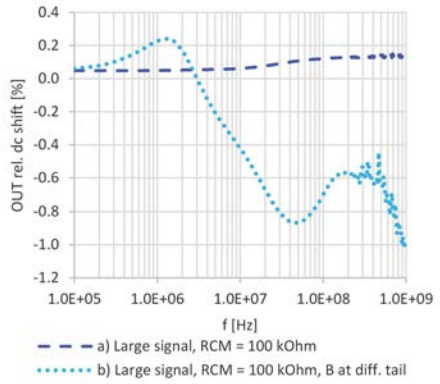

Fig. 9. Simple NMOS OTA VDD EMI susceptibility

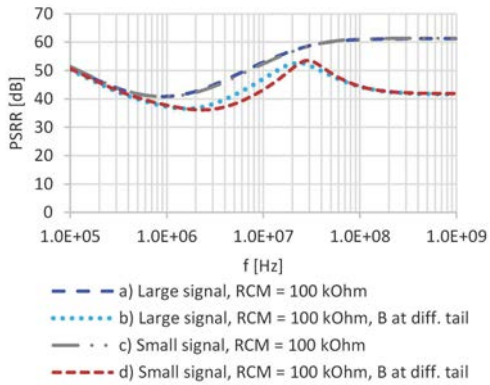

Fig. 10. Simple NMOS OTA PSRR

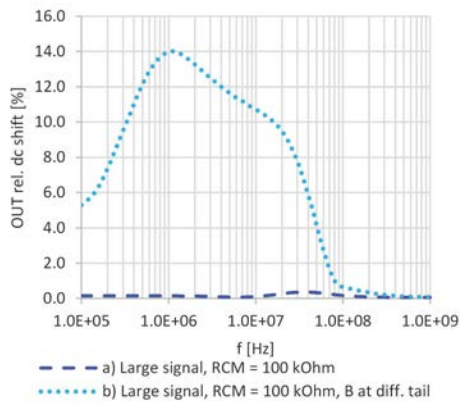

Fig. 11. Simple NMOS OTA CM input EMI susceptibility

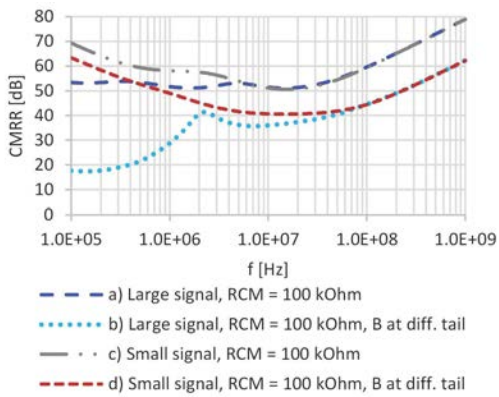

Fig. 12. Simple NMOS OTA CMRR

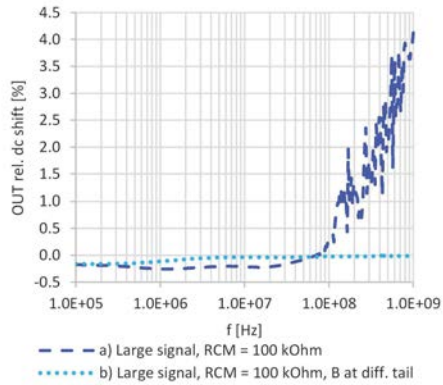

Fig. 13. Simple PMOS OTA VDD EMI susceptibility

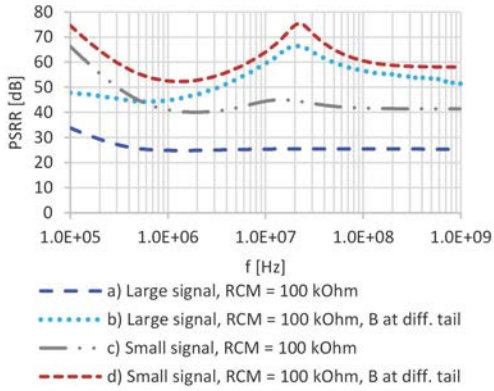

Fig. 14. Simple PMOS OTA PSRR

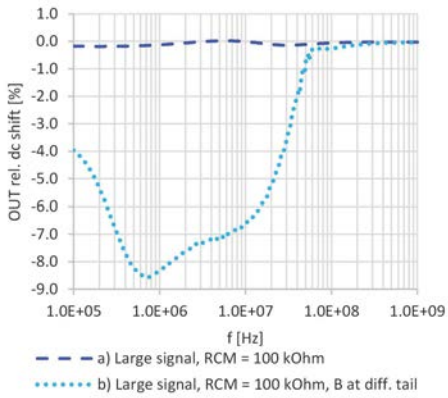

Fig. 15. Simple PMOS OTA CM input EMI susceptibility

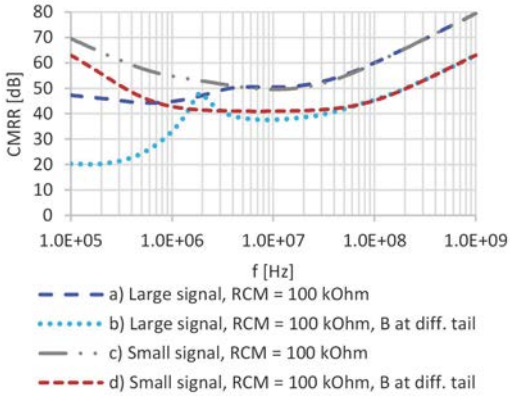

Fig. 16. Simple PMOS OTA CMRR

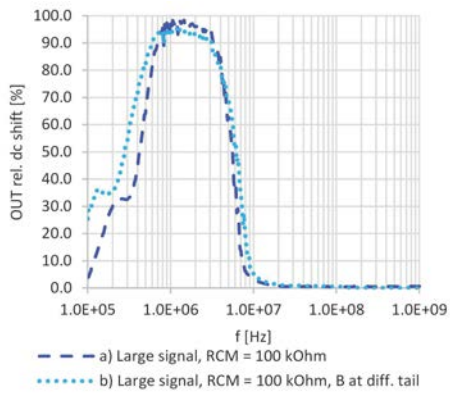

Fig. 17. Miller PPDAL OTA VDD EMI susceptibility

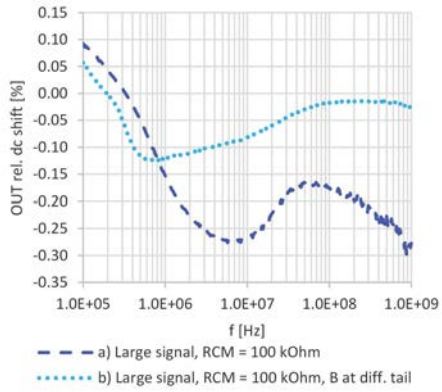

Fig. 21. Miller NPDAL OTA VDD EMI susceptibility

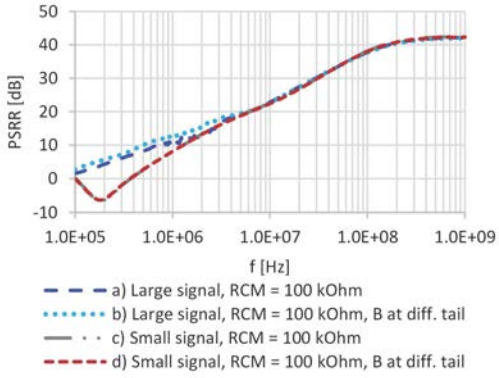

Fig. 18. Miller PPDAL OTA PSRR

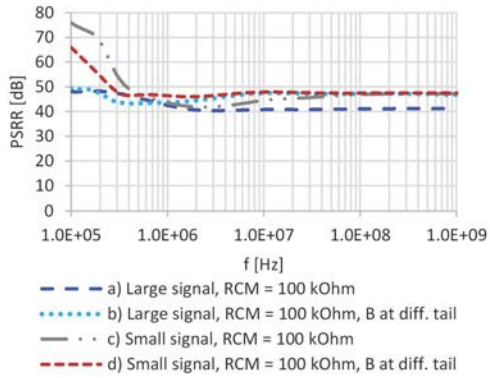

Fig. 22. Miller NPDAL OTA PSRR

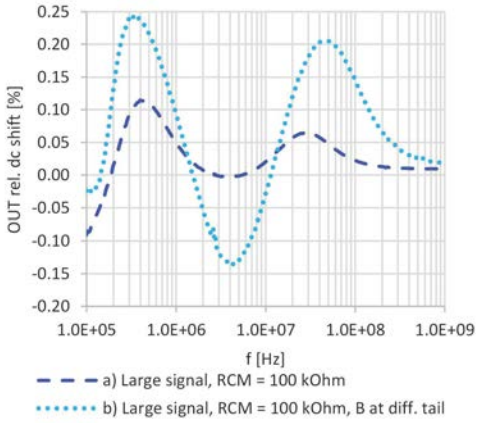

Fig. 19. Miller PPDAL OTA CM input EMI susceptibility

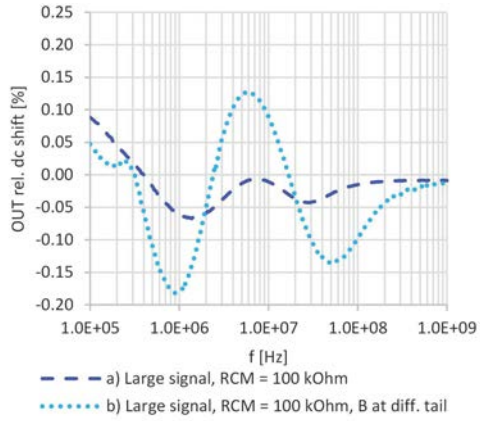

Fig. 23. Miller NPDAL OTA CM input EMI susceptibility

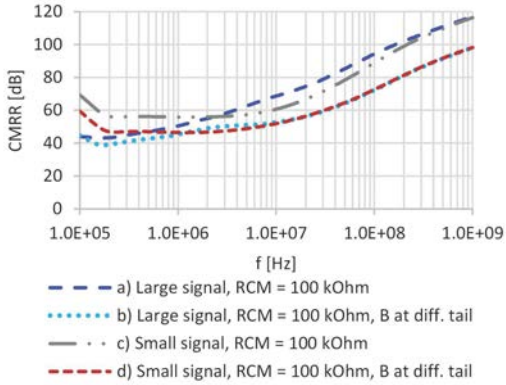

Fig. 20. Miller PPDAL OTA CMRR

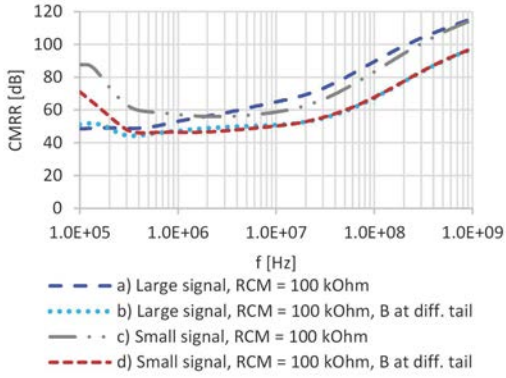

Fig. 24. Miller NPDAL OTA CMRR

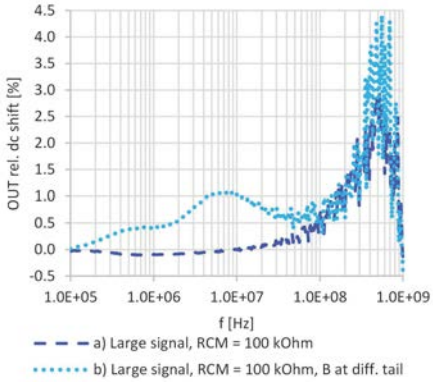

Fig. 25. Folded NMOS cascode OTA VDD EMI susceptibility

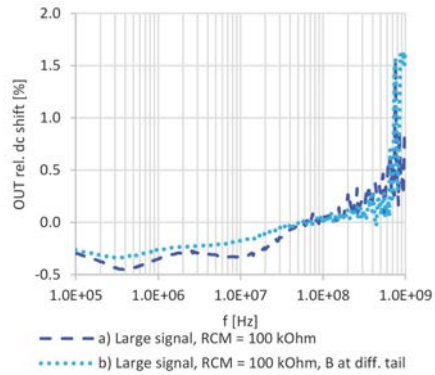

Fig. 29. Folded PMOS cascode OTA VDD EMI susceptibility

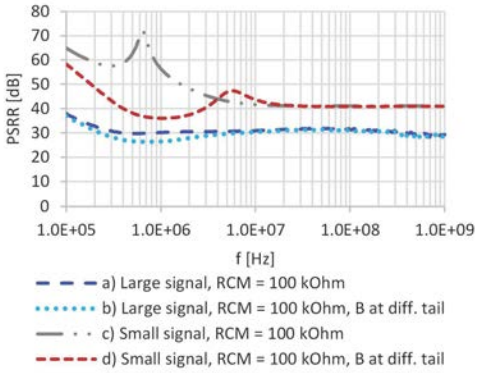

Fig. 26. Folded NMOS cascode OTA PSRR

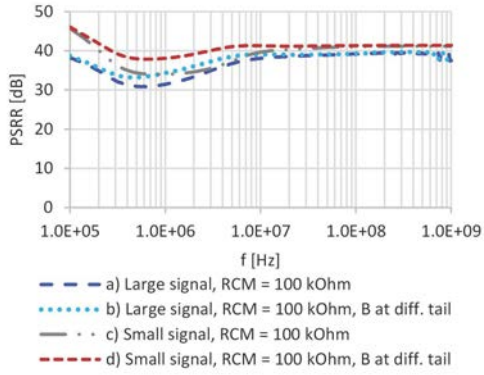

Fig. 30. Folded PMOS cascode OTA PSRR

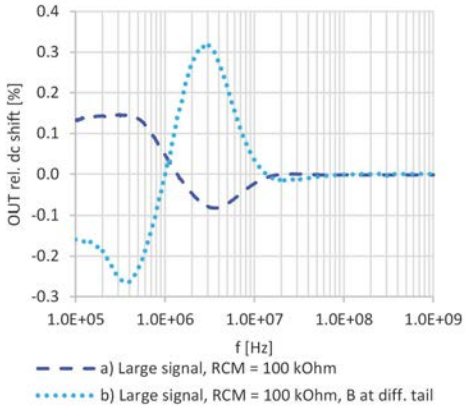

Fig. 27. Folded NMOS cascode OTA CM input EMI susceptibility

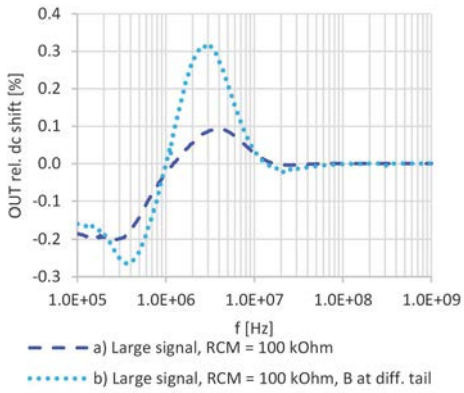

Fig. 31. Folded PMOS cascode OTA CM input EMI susceptibility

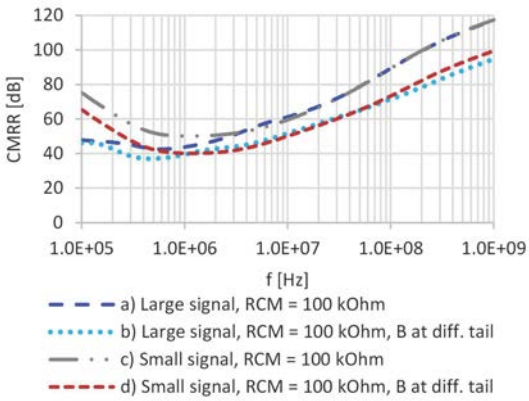

Fig. 28. Folded NMOS cascode OTA CMRR

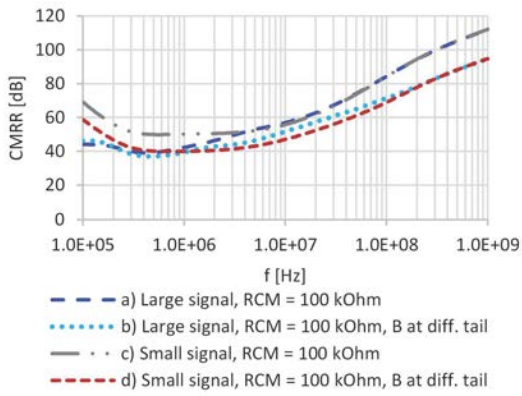

Fig. 32. Folded PMOS cascode OTA CMRR

of the PMOS input differential pair connected to differential TAIL node has excellent supply EMI susceptibility.

Nevertheless, the Miller NPDAL OTA with classically connected back-gate of the input differential pair has lower input common mode EMI susceptibility. We see the similar small and large signal PSRRs and CMRRs as for the simple NMOS OTA.

The folded NMOS cascode OTA and the folded PMOS cascode OTA graphs (Fig. 25 to Fig. 32) show that the folded PMOS cascode OTA with classically connected back-gates of the input PMOS differential pair has low supply EMI susceptibility. On the other hand, the folded NMOS cascode OTA with classically connected back-gates of the input NMOS differential pair has low input common mode EMI susceptibility. We see the similar small and large signal PSRRs and CMRRs as for the simple OTAs.

3.7 Summary tables

All results within EMI susceptibility analysis of the proposed OTAs are in Tab. 4 and Tab. 5. Table 4 shows EMI susceptibility results of the OTAs with classically connected back-gates of the input differential MOS pair. Table 5 shows EMI susceptibility results of the OTAs with back-gates of the input differential MOS pair connected to differential TAIL node. We see large differences between small and large signal simulations for some cases in both tables that lead us to give a recommendation for PSRR and CMRR simulations. If we consider a large disturbance signal then we recommend that one should use the time domain analysis rather than the ac frequency domain analysis in order to avoid skewed results because, for example, the ac analysis does not take into account nonlinearity effects.

4 Conclusion

This paper presents comparative study of six different integrated OTA topologies. In addition to presented and discussed EMI susceptibility comparison results, the study also contains new supply and input common mode EMI susceptibility simulation setups with defined input common mode impedances. The EMI simulation results within large and small excitation signals in time and frequency domains were discussed as well as the impact of the back-gate connections of the input differential MOS

Table 4. EMI susceptibility of the proposed OTAs (NA* - not available due to the ac analysis)

EMI signal	Small (ac)				Large (1 V peak)			
EMI for	VDD supply		Input CM		VDD supply		Input CM	
OTA topology	OUT max dc rel. shift (%)	PSRR min. (dB)	OUT max dc rel. shift (%)	CMRR min. (dB)	OUT max dc rel. shift (%)	PSRR min. (dB)	OUT max dc rel. shift (%)	CMRR min. (dB)
a) Simple NMOS	NA*	40.8	NA*	50.6	0.2	40.8	0.4	51.1
b) Simple PMOS	NA*	40.1	NA*	49.6	4.1	24.9	0.2	44.3
c) Miller PPDAL	NA*	0.0	NA*	55.8	98.6	1.5	0.1	43.0
d) Miller NPDAL	NA*	41.8	NA*	56.0	0.3	40.4	0.1	48.6
e) Folded NMOS cascode	NA*	41.1	NA*	50.1	2.91	28.3	0.1	42.5
f) Folded PMOS cascode	NA*	34.0	NA*	49.9	1.5	30.8	0.2	39.1

Table 5. EMI susceptibility of the proposed OTAs with back-gates of input MOS pairs at TAIL node (NA* - not available due to the ac analysis)

EMI signal	Small (ac)				Large (1 V peak)			
EMI for	VDD supply		Input CM		VDD supply		Input CM	
OTA topology back -gates of input MOS pairs at TAIL node	OUT max dc rel. shift (%)	PSRR min. (dB)	OUT max dc rel. shift (%)	CMRR min. (dB)	OUT max dc rel. shift (%)	PSRR min. (dB)	OUT max dc rel. shift (%)	CMRR min. (dB)
a) Simple NMOS	NA*	36.5	NA*	40.6	1.0	36.1	14.0	17.4
b) Simple PMOS	NA*	52.3	NA*	41.0	0.2	44.3	8.6	20.0
c) Miller PPDAL	NA*	0.1	NA*	46.4	95.4	2.7	0.2	38.9
d) Miller NPDAL	NA*	46.0	NA*	46.0	0.1	43.2	0.2	44.1
e) Folded NMOS cascode	NA*	36.1	NA*	40.1	4.4	26.3	0.3	37.0
f) Folded PMOS cascode	NA*	37.9	NA*	39.9	1.6	33.2	0.3	37.0

pair in the proposed low power OTAs. We presented that the back-gate connection can help to decrease OTA EMI susceptibility in some cases (see Tab. 4 and Tab. 5).

References

[1] J. R. Agazzini, R. H. Randall, and F. Rusell, "Analysis of Problems in Dynamics by Electronic Circuits", *Proceedings of the IRE*, vol. 35, no. 5, pp. 444-452, doi: 10.1109/JRPROC.1947.232616.

[2] L. Fu, Y. Zhaowen, F. Changshun and S. Donglin, "Extraction and analysis on Conducted Electromagnetic Susceptibility Elements of Integrated Circuits", *IEEE Access*, p. 149125-149136 doi: 10.1109/ACCESS.2021.3125051.

[3] A Richelli, L. Colalongo, M. Quarantelli and Z. M. Kovacs-Vajna, "Robust Design of Low EMI Susceptibility CMOS OpAmp", *IEEE Transactions on Electromagnetic Compatibility*, vol. 46, no. 2, pp. 291-298 doi: 10.1109/TEMC.2004.826874.

[4] O. Aiello and J. M. Redouté, "Design of a Neural Recording Amplifier Robust to EMI", *Proceedings 2013 Asia-Pacific Symposium on Electromagnetic Compatibility* (APEMC), Australia, May, pp. 1-4 doi: 10.1109/APEMC.2013.7360665.

[5] M. Magerl, Ch. Stockreiter and A. Baric, "Influence of RF Disturbance Phase on Amplifier DPI Characteristics", *2017 International Symposium on Electromagnetic Compatibility – EMC EROPE*, France, November, pp. 1-5 doi: 10.1109/EMCEurope.2017.8094756.

[6] T. Hino and H. Watanabe, "Analysis of RF Noise in LDO and Establishment of Noise Immunity", *2019 International Symposium on Electromagnetic Compatibilty – EMC EUROPE*, Spain, September, pp. 508-512 doi: 10.1109/EMCEurope.2019.8872083.

[7] A. D. Grasso, S. Pennisi, G. Scotti, and A. Trifiletti, "0.9-V Class-AB Miller OTA in 0.35-m CMOS With Threshold-Lowered Non-Tailed Differential Pair", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 7, pp. 1740-1747 doi: 10.1109/TCSI.2017.2681964.

[8] B. N. Aiyappa, M. Madhusudan, B. Yashaswini, R. Yatish, and M. Nithin, "Amplifier Design in Weak Inversion and Strong Inversion – A Case Study", *2017 International Conference on Communication and Signal Processing* (ICCSP), India, pp. 1227-1231 doi: 10.1109/ICCSP.2017.8286575.

[9] F. F. Offner, "Balanced Amplifiers", *Proceedings of the IRE*, vol. 35, no. 3, pp. 306-310 doi: 10.1109/JRPROC.1947.232277.

[10] J. M. Miller, "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit", *Scientific Papers of the Bureau of Standards*, vol. 15, pp. 367-385, retrieved from http://nvlpubs.nist.gov.

[11] D. Krolak and P. Horsky, "An EMC Susceptibility Study of Integrated Basic Bandgap Voltage Reference Cores", *Radioengineering*, vol. 31, no. 3, pp. 413-421 doi: 10.13164/re.2022.0413.

[12] P. E. Allen, "Lecture 240 - Simulation and Measurements of OP AMP", (Reading: AH - 310-323) [*Online*], http://pallen.ece.gatech.edu/Academic/ECE_6412/Spring_2003/L240-Sim&Measof OpAmps(2UP).pdf.

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