Journal of ELECTRICAL ENGINEERING, VOL 74(2023), NO1, 57–63

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PAPERS

Delay analysis of mixed CNT bundles as global interconnect for nanotechnology nodes

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This paper presents modeling of high current capability of mixed carbon nanotube (CNT) bundle interconnects depending upon the type of constituent CNT materials and their orientations. With different arrangements, one category of novel mixed CNT bundles formed by the combination of multi-walled/multi-shell CNT and double-shell CNT bundles (MDCB) are proposed and compared with the mixed CNT bundles (MSCB) formed with multi-shell CNT and single-walled CNT bundles. A time-domain analysis is performed for these structures to analyse the effect of delay and power dissipation. It has also been observed that MDCB structures give better performance ($\approx$ 30%) than MSCB structures in terms of power-delay product at the global length of interconnect for nano-regime technology nodes. Also, MDCB structure formed by placing multi-walled CNTs along the periphery and double-walled CNTs in the centre of structure yields the best result against all proposed mixed CNT bundled structures and can be employed for future interconnect applications.

K e y w o r d s: carbon nanotube (CNT), single-walled CNT (SWCNT), multi-walled CNT (MWCNT), double-walled CNT (DWCNT), multi-walled and double-wall CNT bundles (MDCB), multi-walled and single-wall CNT bundles (MSCB), power-delay product (PDP), mean-free path (MFP)

1 Introduction

Earlier, gate delays monopolized interconnect delay but at nano-regime nodes, the study of interconnect is becoming very important due to associated parasitic such as capacitances and inductances which play a crucial role in determining circuit's performance. On the basis of length, interconnects can be distinguished into local, intermediate and global interconnects [1]. The local interconnect links localized nodes and is of shorter length, intermediate interconnects work for intermediate length and the global interconnects are the longest in length that is used to connect many nodes on the chip like for clock lines or ground.

With the increased pace of scaling of integrated circuits, copper showed an increase in resistance and there is a need to introduce an alternative material like carbon nanotube (CNT) to give outstanding performance beyond 45nm technology node to overcome reliability concerns of metallic interconnects [2-4]. This led to finding a suitable interconnect material for future scaled nodes. Carbon nanotubes (CNTs) have attracted the VLSI industry due to remarkable unique properties like good current carrying capability, good thermal stability and mechanical strength. CNTs are developed in a cylindrical shape by rolling up graphene sheets. Depending upon the direction of the rolled graphene sheet, chiral indices (n,m) decides the structure of CNT. For n=m, CNT exhibits armchair structure and for n or m=0, CNT can exhibit zigzag structure [5]. For the case (where i is an integer), n-m=3i armchair CNTs are metallic in nature and on the other side, zigzag CNTs can be metallic or semiconducting in nature. Preferably, metallic CNTs are useful for interconnect applications. Depending upon the chirality, nanotubes can be metallic or semiconducting in nature. CNTs can be fabricated through CVD, arc-discharge or laser ablation methods. When a single sheet of graphene is rolled, single-walled CNT (SWCNT) is formed and when multiple sheets are rolled up with a common centre, CNT with many walls *ie* , MWCNT is formed [6]. Double-walled CNT (DWCNT) is a special and unique kind of MWCNT in which only two sheets are rolled up concentrically. Bundled CNT structure is developed by placing the number of CNTs together and helps to aid high resistance. Due to excellent properties, CNTs have occupied a special place in the areas of nanoelectronics, material science, and optics, biological and mechanical fields. Especially in the field of electronics, CNTs are employed as energy conversion devices, energy storage devices, nanometre semiconductor transistors, electrostatic discharge (ESD) protection, nano-electromechanical systems (NEMS), as passives and interconnects.

Copper faced certain issues like electromigration and surface-scattering beyond 45 nm technology node. Different comparisons have been made between copper and different types of CNTs that concluded that CNTs can easily outperform copper at global lengths in terms of the propagation delay of the interconnect [1,2]. Significant work on different parameters like length, diameter and temperature has been done in the literature on SWCNTs and MWCNTs to determine their performance [7-10]. Work has been done on mixed CNT bundle interconnects comprising of MWCNTs and SWCNTs formed with the help of equivalent single conductor (ESC) models of MWCNTs

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https://doi.org/10.2478/jee-2023-0007, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

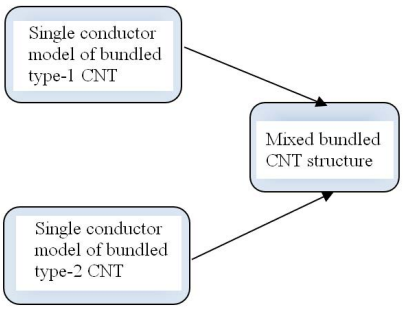

Fig. 1. Hierarchical model of mixed bundled CNT structure

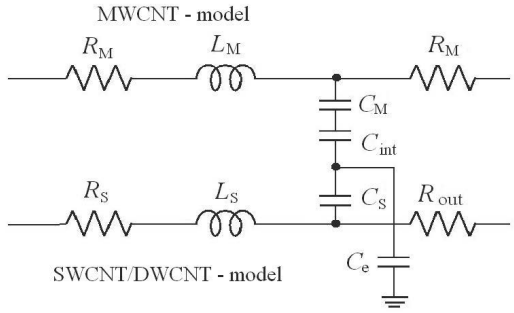

Fig. 2. Electrical equivalent circuit of mixed CNT interconnect

and SWCNTs. It has been observed that the mixed bundle interconnect parasitic gets better by maximizing the width and diameter of CNTs [11-18]. Little work has been done on analysing delay considering the consequences of crosstalk of mixed CNT structures [19, 20]. It has been concluded that this mixed CNT bundle interconnect gives better performance than only MWCNTs and only SWCNTs bundled structure. But still, not much work is done on the mixed CNT bundle formed with MWCNT and DWCNT. This research paper introduces the modelling of different types of mixed CNT bundle structures. Depending upon the arrangements of MWCNTs, SWCNTs and DWCNTs, different structures of mixed CNT bundle structures are proposed. Performance of the latest mixed CNT bundle *ie* , MDCB structures is compared with MSCB structures considering the effect of temperature at three nano-regime technology nodes.

The layout of this research paper is described as follows. Section 2 proposes a description of the formation of different types of mixed CNT bundle structures. Different types of MDCB and MSCB structures are formed by changing different positions of constituent CNT materials. Section 3 presents the simulation setup used for the time domain analysis of mixed CNT bundle structures. Section 4 presents the detail of simulation results in terms of interconnects delay, the power dissipated and PDP. The values obtained from simulation are compared for all mixed CNT bundle structures. Finally, section 5 draws the conclusion of this paper.

2 Mixed CNT bundle structures

The hierarchical and electrical equivalent complicated structure of different mixed CNT bundle structures is formed with the help of equivalent single conductor models of different types of constituents *ie* , MWCNTs, DWCNTs and SWCNTs as shown in Fig. 1 and Fig. 2 below [11,12].

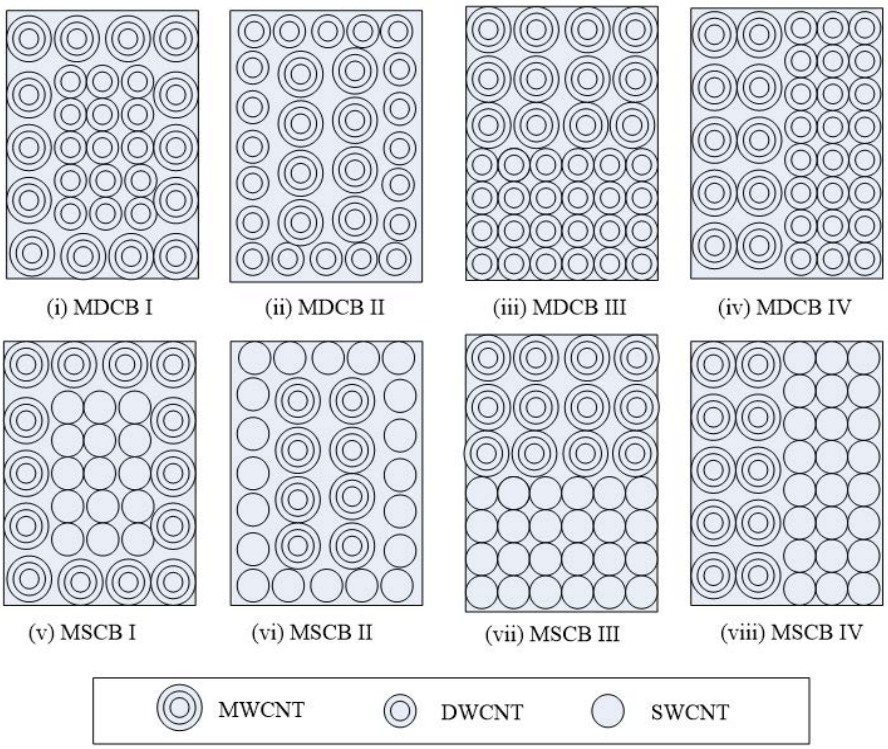

Fig. 3. Different types of Mixed CNT Bundled structures

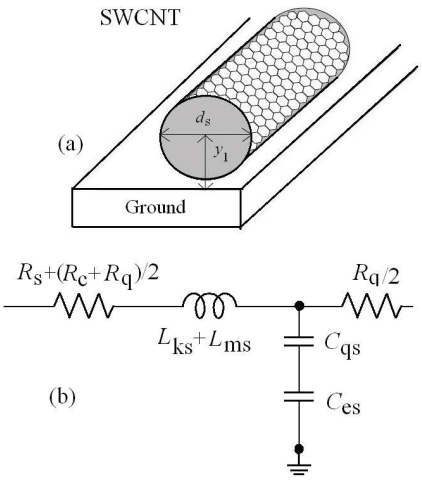

Fig. 4. (a) – the physical structure of CNT, and (b) – electrical equivalent structure of SWCNT

With different arrangements of the constituent CNTs, various types of mixed CNT bundled structures are developed as shown in Fig. 3.

The optical absorption and emission give rise to scattering which further plays an important role in determining mean free paths (MFP) of carbon nanotubes. At the low-temperature range, acoustic scattering in CNTs is given by

$$\lambda_{\mathrm{A}} = \lambda_{\mathrm{A},300}\frac{300}{T}, \tag{1}$$

where $\lambda_{\mathrm{A},300}$ is nearly 1600 nm. Electrons are agglomerated by the electric field and attain sufficient kinetic energy to reach the optical phonon state at higher temperatures [8]. The optical phonon occupation is expressed by, [7].

$$N_{\mathrm{O}}(T) = \left[\exp\left(h\Omega/k_{\mathrm{B}}T\right)-1\right]^{-1}, \tag{2}$$

where k_{B} is the Boltzmann constant and $h\Omega = 0.16 - 0.2\,\mathrm{eV}$. The optical absorption length with $\lambda_{\mathrm{O},300} = 15\,\mathrm{nm}$ is

$$\lambda_{\mathrm{OA}}(T) = \lambda_{\mathrm{O},300}\frac{N_{\mathrm{O}}(300)+1}{N_{\mathrm{O}}(T)}. \tag{3}$$

Beyond the threshold level, after getting more energy, electrons cause inelastic optical field emission

$$\lambda^{\mathrm{F}}_{\mathrm{OE}}(T) = \frac{h\Omega_{\mathrm{O}} - k_{\mathrm{B}}T}{qV/L} + \lambda_{\mathrm{O},300}\frac{N_{\mathrm{O}}(300)+1}{N_{\mathrm{O}}(T)+1}. \tag{4}$$

Electrons travel certain distance before emitting phonons gives optical field absorption and is expressed by

$$\lambda^{\mathrm{A}}_{\mathrm{OE}}(T) = \lambda_{\mathrm{OA}}(T) + \lambda_{\mathrm{O},300}\frac{N_{\mathrm{O}}(300)+1}{N_{\mathrm{O}}(T)+1}. \tag{5}$$

The sum of optical field emission and absorption gives the net optical inelastic emission

$$\lambda_{\mathrm{OE}} = \left[\frac{1}{\lambda^{\mathrm{F}}_{\mathrm{OE}}} + \frac{1}{\lambda^{\mathrm{A}}_{\mathrm{OE}}}\right]^{-1}. \tag{6}$$

The sum of elastic acoustic scattering λ_{A}, inelastic optical emission λ_{OE} and inelastic absorption scattering λ_{OA} gives the final temperature-dependent effective mean free path

$$\lambda_{\mathrm{eff}} = \left[\frac{1}{\lambda_{\mathrm{A}}} + \frac{1}{\lambda_{\mathrm{OE}}} + \frac{1}{\lambda_{\mathrm{OA}}}\right]^{-1}.$$

2.1 Single-walled CNT bundle as interconnect

With diameter of SWCNT d_{s} and the height of SWCNT from the centre when placed over the ground plane as y_1, the physical structure of single-walled CNT is shown in Fig. 4(a). The equivalent circuit diagram employed to determine its impedance parameters for its performance as an interconnect material is shown in Fig. 4(b).

The resistance of isolated SWCNT is about 6.45 kΩ. The imperfect metal-CNT contacts introduce contact resistance which depends upon the growing process and is neglected in this paper. The scattering resistance R_{s} is encountered if the tube length (L) becomes more than MFP (L_0), and shows an increase with the increase in the length of CNT. The quantum resistance R_{q} is equally distributed between the two end contacts, hence the resistance R_{B} of n bundled SWCNT interconnect is calculated as

$$R_{\mathrm{s}} = R_{\mathrm{q}}\frac{L}{L_0}, \quad R_{\mathrm{q}} = \frac{h}{4e^2}, \quad R_{\mathrm{B}} = \frac{\dfrac{h}{4e^2}\dfrac{L}{L_0}}{n}, \tag{7}$$

with h being the Planck's constant and e being electron charge, [5].

The disadvantage of large value of resistance (7 k − 100 kΩ) of isolated SWCNT is fought by forming a dense bundle of CNTs by packing and placing identical single-walled carbon nanotubes in parallel fashion [17].

Nanotube stores a certain charge when it is placed at a distance from the ground, [6], exhibiting the electrostatic capacitance C_{e}. The electrostatic energy stored when current flows in the nanotube results in effective quantum capacitance C_{q} to get the effective bundle capacitance C_{B}

$$C_{\mathrm{e}} = \frac{2\pi\varepsilon}{\ln\dfrac{y_1}{d_{\mathrm{s}}}}, \quad C_{\mathrm{q}} = \frac{8e^2}{hv_F}, \quad C_{\mathrm{B}} = \frac{C_{\mathrm{es}}C_{\mathrm{qs}}}{C_{\mathrm{es}}+C_{\mathrm{qs}}}, \tag{8}$$

where, v_F is the Fermi velocity of electrons in CNT, and we consider four such channels.

The magnetic energy due to the flow of current in the nanotube gives magnetic inductance L_{m}, and the stored kinetic energy in each channel of the nanotube carrying current contributes to the kinetic inductance L_{k}, while the parallel addition of n isolated CNTs yields total L_{B} inductance of a bundle

$$L_{\mathrm{m}} = \frac{\mu}{2\pi}\ln\frac{y_1}{d_{\mathrm{s}}}, \quad L_{\mathrm{k}} = \frac{h}{2e^2v_{\mathrm{F}}}, \quad L_{\mathrm{B}} = \frac{L_{\mathrm{m}}+L_{\mathrm{k}}}{n}, \tag{9}$$

where μ is the magnetic permeability of free space.

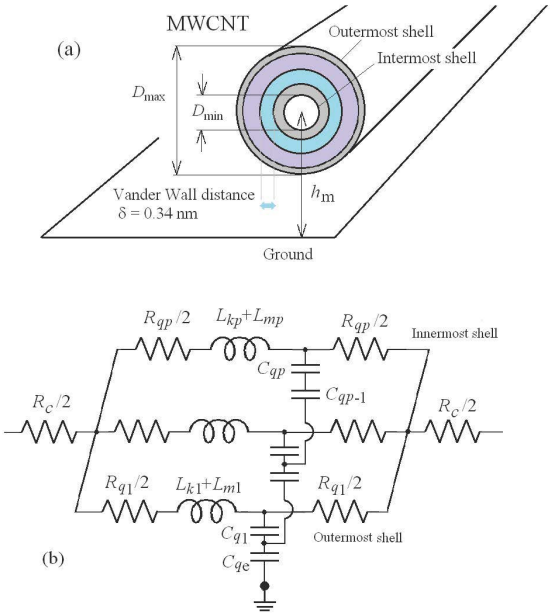

Fig. 5. (a) – Physical structure of MWCNT, and (b) – electrical circuit of MWCNT interconnect

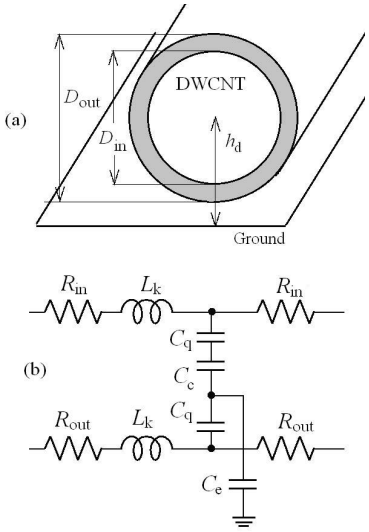

Fig. 6. (a) – Physical structure of MWCNT, and (b) – RLC circuit of the proposed DWCNT interconnect

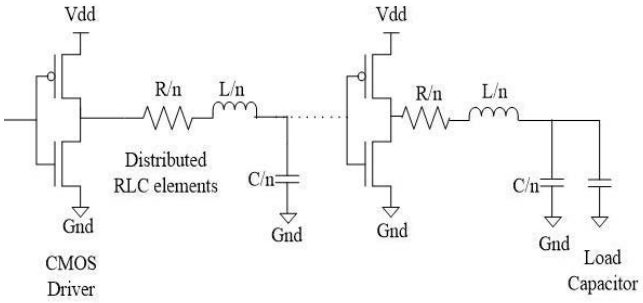

Fig. 7. Set-up used for simulation

2.2 Multi-walled CNT bundle as interconnect

MWCNT, as shown in Fig. 5(a), is formed by placing concentric hollow shells of graphene at a height h_{m} above the ground from the centre [18].

The diameter of the exterior most and interior shell is taken as $D_{\max}$ and $D_{\min}$. The equivalent RLC circuit of MWCNT is viewed in Fig. 5(b). The number of shells p and the diameter of each shel can be determined as

$$p = 1 + \frac{D_{\max} - D_{\min}/2}{2\delta}, \quad D_i = D\big(2\delta[i-1]\big)_{\max}. \quad (10)$$

The value of i ranges from 1 to p. The number of conducting channels can be expressed by

$$N_i = aD_i + b, \quad (11)$$

these values are $a = 0.0612\,\mathrm{nm}^{-1}$ and $b = 0.425$. Each shell of the MWCNT has different diameters as given by equation and each conducting channel in a shell has different temperature-dependent MFPs [16]. The net resistance of the MWCNT is given by

$$R = R_{\mathrm{c}} + R_{\mathrm{q}i} + R_{\mathrm{s}i} = \frac{1}{n}\Big[R_{\mathrm{c}} + \frac{h}{4e^2}\big(1 + \frac{L}{\lambda_{\mathrm{eff}}}\big)\Big]. \quad (12)$$

The magnetic inductance of each MWCNT shell can be expressed as

$$L_{\mathrm{m}i} = \frac{\mu}{2\pi}\cosh^{-1}\frac{2h_{\mathrm{m}}}{D_i}, \quad (13)$$

while the kinetic inductance is $L_{\mathrm{k}i} = L_{\mathrm{k}}$.

The electrostatic capacitance of the MWCNT structure is $C_{\mathrm{e}i} = C_{\mathrm{e}}$ and $C_{\mathrm{q}i} = C_{\mathrm{q}}$.

Each shell of MWCNT possesses a different potential, therefore shell to shell capacitive coupling is

$$C_{si} = \frac{2\pi\varepsilon}{\ln\dfrac{D_{i+1}}{D_i}}. \quad (14)$$

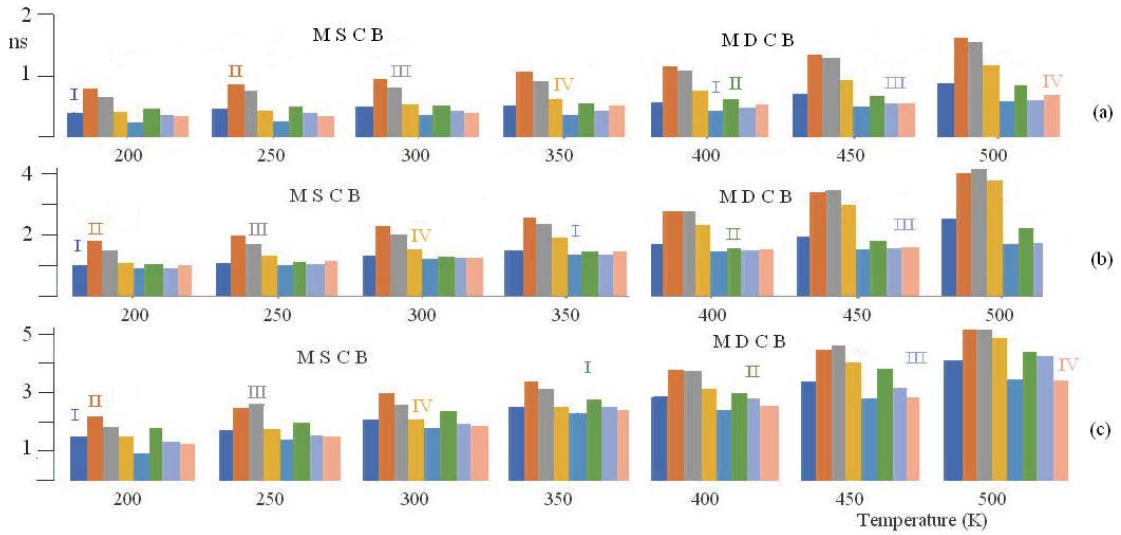

Fig. 8. Temperature-dependent propagation delay in ns for MSCB and MDCB bundle structures at different technology nodes: (a) – 32 nm, (b) – 22 nm, and (c) – 16 nm

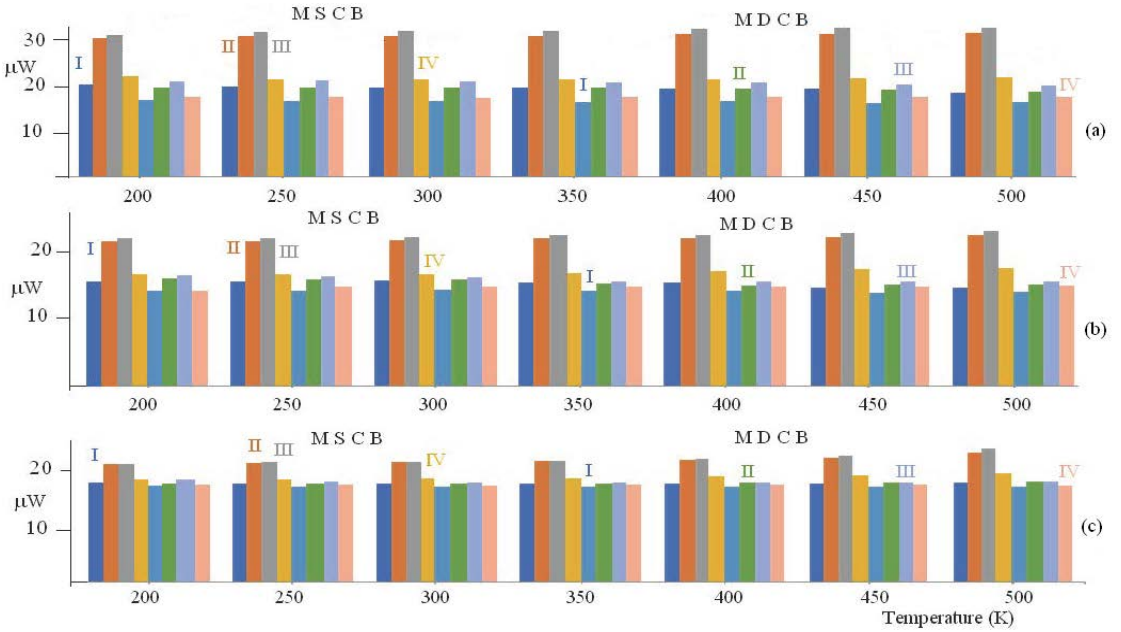

Fig. 9. Temperature-dependent power dissipation in mW for MSCB and MDCB bundle structures at different technology nodes: (a) – 32 nm, (b) – 22 nm, and (c) – 16 nm

2.3 Double-walled CNT bundle as interconnect

The physical structural diagram and equivalent electrical circuit of DWCNT are shown in Fig. 6. Compared to SWCNT, DWCNT gives the lesser value of resistance due to the parallel sum of the inner and outer shell, [20].

The input is taken as a pulsed waveform and 1 pF capacitor is acting as the load for the simulation of 1000 μm interconnects length. The aspect ratio of the transistors is assumed as 60. The time consumed by the waveform to reach 90% of its maximum amplitude is called rise time, and the time utilized by the waveform to drop to its 10% value is defined as fall time. Transient analysis is done to estimate the performance *ie* delay, the power dissipated and PDP of the circuit.

3 Circuit diagram

This section presents the distributed circuit diagram in Fig. 7 having CMOS driver and is employed for the transient analysis of mixed CNT bundled interconnects.

The input is taken as a pulsed waveform and 1 pF capacitor is acting as the load for the simulation of 1000 μm interconnects length. The aspect ratio of the transistors is assumed as 60. The time consumed by the waveform to reach 90% of its maximum amplitude is called rise time, and the time utilized by the waveform to drop to its 10% value is defined as fall time. Transient analysis is done to estimate the performance *ie* delay, the power dissipated and PDP of the circuit.

4 Results

SPICE simulations to analyse propagation delay, the power dissipated and PDP of the circuit are performed on tanner tool for global interconnect length of 1000 μm using ITRS technology parameters [23,24]. Fig. 8 shows propagation delay of various mixed CNT bundle structures at the temperature range from 200-500K for 32 nm, 22 nm and 16 nm technology, respectively. The delay of the circuit shows an increase with the rise in temperature due to scattering and decreased MFP of the electrons. It is evident from the results that MDCB structures formed with MWCNT and DWCNT yield lesser delay than MSCB structures. Also, MDCB I structure formed with MWCNT on the periphery and DWCNT at the centre of the structure (which helps in providing good conductivity due to double-shell structure) gives the least delay among all MDCB and MSCB structures at all nano regime technology nodes.

It has been observed that delay tends to double itself for mixed bundles while switching from 32 nm to 2 nm to 16 nm technology node. This trend further enhances at higher temperature range due to abrupt increase in temperature dependent resistance and decrease in effective mean free path of electrons. Fig. 9 shows the power dissipation of the circuit for different MDCB and MSCB structures for 1000 μm interconnect length at an elevated temperature range from 200-500K for 32 nm, 22 nm and 16 nm technology nodes, respectively.

Due to the negligible effect of change in temperature on capacitance, because of the dominance of inter-shell capacitance over temperature dependent capacitance, the electrostatic capacitance of outer most shell of CNT with ground plays a very important role. So, the structures formed by placing MWCNT at the peripheral boundary shows the least capacitive effect, therefore minimum power dissipation in the circuit. Power parameter shows almost constant relation with temperature. Also, DWCNTs give less capacitance than SWCNTs. As a result, MDCB structures yields less power than MSCBs. However, on comparing all mixed CNT structures, the MDCB I structure offers minimum power dissipation for all three technology nodes due to decreased capacitance offered by MWCNTs placed on the edges of bundle. The net performance of interconnect is determined by studying values of the figure of merit, *ie* a power-delay product that combines and considers the effect of both power and delay parameters in one parameter. It is analysed from Fig. 10 that the MDCB I structure yields the lowest PDP value among all eight mixed bundled structures for 1000 μm, thus giving excellent performance and making its appropriate place in VLSI industry.

It is clearly observed from the temperature-dependent simulated results of global interconnect length at different technologies that MDCB structures give fairly good performance with regard to delay, power dissipation and PDP than MSCB structures attributable to the presence of DWCNT with double-layer structure thereby yielding better conductivity than SWCNT. Also, among all mixed CNT bundle structures mentioned in this paper, MDCB I structure formed by placing DWCNT in the centre and MWCNT along the peripheral edge gives the least delay, power dissipation and PDP. So, MDCB I structure can possibly be used as VLSI interconnect material for global lengths at future generation nodes.

5 Conclusion

A range of novel and different types of mixed CNT bundles are developed using MWCNT, SWCNT and

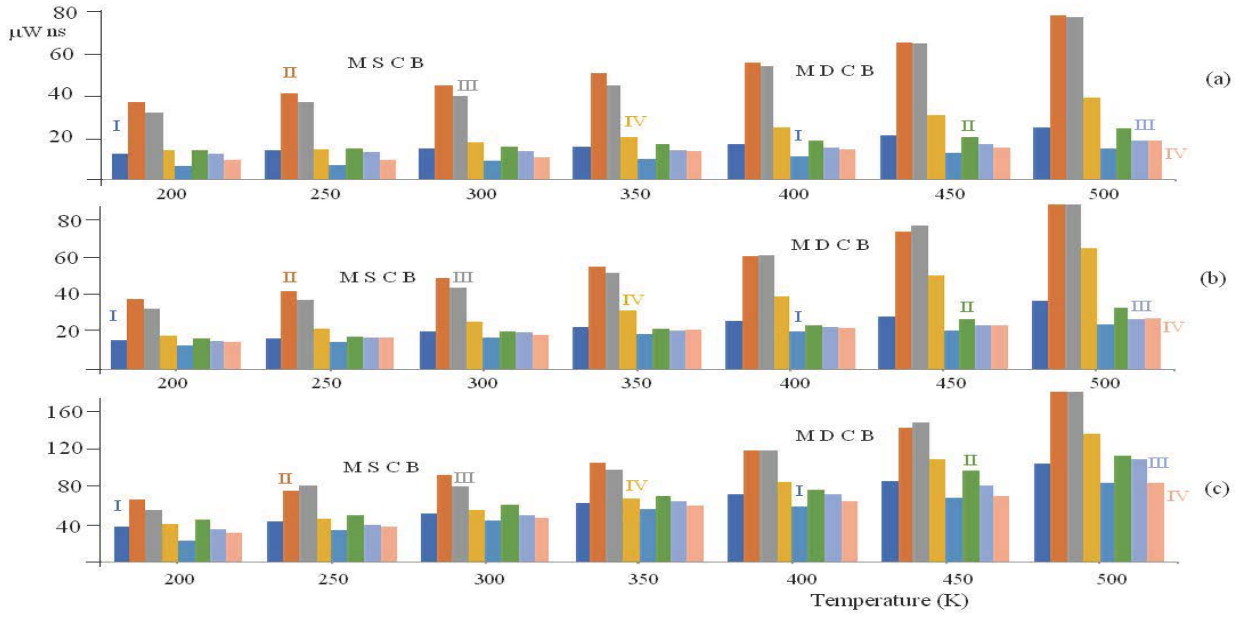

Fig. 10. Temperature-dependent PDP in mW ns for MSCB and MDCB bundle structures at different technology nodes: (a) – 32 nm, (b) – 22 nm, and (c) – 16 nm

DWCNT. Their electrical equivalent RLC models are simulated over a temperature range from 200-500 K.

The performance of all the proposed structures for interconnect applications is compared on the basis of parameters like delay, the power dissipated in the circuit and power-delay product (PDP) for 1000 μm interconnect length. MDCB structures overrule all MSCB structures at all temperatures and at every technology node for all the parameters because of the presence of double-shelled CNT *ie* DWCNT instead of SWCNT in the mixed bundle along with MWCNT which gives better parasitic results. Also, it has been observed that MDCB I interconnect structure in which MWCNTs are planted along the outer edge and DWCNTs are put at the centre of the structure yielded the unbeatable performance against all eight structures for nano-regime technology nodes.

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Received 21 January 2023

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