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PAPERS

# Integrable emulation of a floating incremental/decremental inverse memristor for memristor bandwidth extension

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The article explores the compact emulation of the inverse memristor through a circuit-based approach. It introduces a floating emulator architecture that incorporates a dual output OTA (Operation Transconductance Amplifier) and DVCC (Differential Voltage Current Conveyor), along with two grounded passive elements, to achieve the emulation of an inverse memristor. The utilization of grounded resistance allows for tunability over the realized behaviour. A key contribution of this research is the novel application of the inverse memristor to extend the operating frequency range of any memristor emulator circuit. Validation of the proposed emulator circuit, in both incremental and decremental modes, along with its application, is conducted using PSPICE-generated simulation results in the 0.18 μm TSMC CMOS technology. Additionally, an inverse memristor emulator configuration employing the IC LM13700 is presented, and its functionality is tested through a breadboard implementation.

Keywords: dual output OTA, DVCC, inverse memristor, LM13700, memristor

## 1 Introduction

The discovery of the memristor, the primary member among memristive elements, dates back almost half a century to 1971 [1]. While other elements have recently entered the discussion, those displaying pinched hysteresis loop (PHL) characteristics can be considered memristive elements [2]; however, not all qualify as true memristors. Various mathematical and experimental studies, as outlined in references [3-6], have been consulted by the authors to gain a comprehensive understanding of ideal memristor properties. The inverse memristor, classified as a non-ideal memristor [7], diverges from following all three fingerprints described for memristors [5]. Functioning as a non-linear voltage/current-controlled inductor, it exhibits shoelace-like characteristics in the transient *v-i* plane akin to a memristor, as demonstrated in referenced works [8]. These transient *v-i* characteristics arise from the application of a bipolar signal across the device. However, due to its dependency on input signal differentiation, the inverse memristor lacks any inherent storage property, eliminating its applicability in various known memristive applications. Consequently, circuit designers and theorists have shown little interest in exploring its properties and potential realization approaches. Nevertheless, literature does document some circuit configurations [9-14] for the inverse memristor emulator, as detailed in Table 1.

Table 1 vividly demonstrates the superior design of the proposed floating inverse memristor emulator compared to existing counterparts. In contrast to inverse memristor emulators cited in [10-12], the presented emulator achieves a floating architecture without the need for any floating elements, distinguishing it from [9, 11, 12]. Moreover, the reported emulator eschews reliance on external voltage multipliers, such as the AD633 IC, rendering it more area-efficient than emulators in [11, 12]. Notably, the maximum operating frequency of the provided inverse memristor surpasses all existing emulator circuits, exhibiting satisfactory frequency response in both incremental and decremental cases – a feature lacking in emulators from [10, 13].

Furthermore, this work introduces innovation by presenting a promising application of the inverse memristor to enhance the operating frequency range of a flux-controlled memristor. The operating frequency range holds paramount importance in analog and digital memristor applications, determined by the maximum frequency limit for obtaining a satisfactory hysteresis response. Particularly in switching applications, it is crucial that the desired memristor response is sustained at higher operating frequencies. Otherwise, with a limited operating frequency range, the memristor reverts to acting as a conventional (linear) resistance only at lower frequencies. Unfortunately, many existing memristor emulators suffer from restricted operating frequency ranges, preventing them from fulfilling their true purpose of mimicking physical memristors.

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**Table 1.** Summary of the previously reported inverse memristor emulators along with the proposed one

| Ref. no. | Number of blocks | Type of inverse memristor | Employment of multiplier IC | Number of passive elements Grounded/Floating | Operating frequency range | Frequency response | Potential application example |
|---|---|---|---|---|---|---|---|
| [9] | 1 LM13700<br>1 TL084 | F | 0 | 1G/7F | 300 Hz<br>to 900 Hz | Satisfactory | Not demonstrated |
| [10] | 2 BJTs | G | 0 | 2G | 10 Hz<br>to 200 Hz | Not Satisfactory | Demonstrated |
| [11] | 2 CCIIs<br>2 BJTs | G | 1 | 3G/1F | 10 Hz<br>to 250 Hz | Satisfactory | Not demonstrated |
| [12] | 2 CCIIs,<br>2 BJTs | G | 1 | 3G/1F | 10 Hz<br>to 250 Hz | Satisfactory | Demonstrated |
| [13] | 2 modified VDCCs | F | 0 | 3G | 10 kHz<br>to 30 kHz | Not Satisfactory | Not demonstrated |
| [14] | 2 VDTAs | F | 0 | 1 G | 10 kHz<br>to 100 kHz | Satisfactory | Not demonstrated |
| **Proposed** | 1 DVCCs<br>1 DO-OTA | F | 0 | 2 G | up to 2 MHz | Satisfactory in both incremental and decremented modes | Demonstrated in memristor bandwidth extension |

## 2 The notion of inverse memristor

In the case of an ideal memristor, a distinctive property is the presence of a pinched hysteresis loop with a cross-over at the origin in a transient *v-i* plot. Furthermore, the span of the *v-i* contour plotted must decrease with an increase in the operating signal frequency [5]. Figure 1 illustrates the ideal memristor characteristics for sinusoidal signal applications using the commonly employed linear memductance model. However, some researchers have noted a similar pinched hysteresis loop (PHL) *v-i* contour in various elements, such as filaments, non-inductor/capacitor components, batteries, etc., when subjected to sinusoidal signals [7]. Nevertheless, certain elements exhibiting this PHL type of *v-i* contour may not display the ideal frequency-related fingerprints defined for a memristor. The inverse memristor is one such element, with its *v-i* curve demonstrating an inverse relationship in the area (in comparison to an ideal memristor) concerning the input signal frequency.

A simplest mathematical model of an element with such characteristics can be defined as

$$i = b_0 v + b_1 \left(\frac{dv}{dt}\right) v \,. \tag{1}$$

Therefore, due to the absence of all three fingerprints of the memristor, the inverse memristor cannot be used as a worthy element in various memristor-related applications. But due to its unique frequency dependence characteristics, it can be used to control and enhance the performance of an ideal memristor as described below. The characteristic of an inverse memristor can be utilized by connecting it in parallel to an ideal memristor. For the shunt connection of an ideal memristor (M) and inverse memristor (M'), the overall current $I_{\text{parallel}}$ flowing through the connection will be the sum of memristive and inverse memristive current as

$$I_{Parallel} = a_0 v_m \sin(\omega t) + \\ + \frac{{v_m}^2 a_1}{\omega}(1 - \cos(\omega t)) \sin(\omega t) + b_0 v_m \sin(\omega t) + \\ + {v_m}^2 \omega b_1 \cos(\omega t) \sin(\omega t)\,, \tag{2}$$

where the first two terms represent memristive current components (with $a_0$ and $a_1$ being the coefficients) and the last two are corresponding to the inverse memristor for the input signal $v_m \sin(\omega t)$ Now, to demonstrate the effect of connecting M' with ideal memristor M, the area enclosed under the lobes of the composite structure plays an important role. The expression given in Eqn. (2) can be useful to find the area enclosed under any *v-i* curve.

$$A = \int_0^{T/2} i \frac{dv}{dt} dt \tag{3}$$

For the only memristor ($G_M = a_0 + a_1\phi$) case, the area can be given as

$$A_{\text{mem}} = -\frac{2a_1 {v_m}^2}{3\omega}\,. \tag{4}$$

Similarly, for the shunt connection, it can be found by using Eqns. (2 and 3) as

$$A_{\text{mem-inv}} = \frac{2}{3}\left(-\frac{a_1 {v_m}^2}{\omega} + \omega b_1 {v_m}^2\right). \tag{5}$$

By using Eqn. (5), we can plot the area ($A_{\text{mem-inv}}$) *versus* frequency (ω) response for the shunt circuit, which is shown in Fig. 1. From this response, it can be observed that controlling the coefficient of inverse memristor, we can alter the frequency dependency of the lobe area. Therefore, we can conclude, that by connecting inverse memristor in shunt with memristor, we can achieve better controllability over memristor performance in the *v-i* plane.

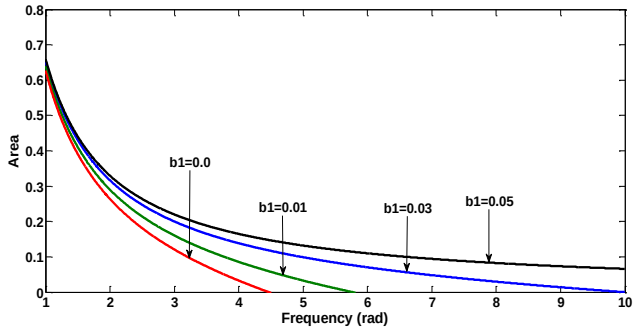



**Fig. 1.** Response of area to frequency for different values of coefficient $b_1$

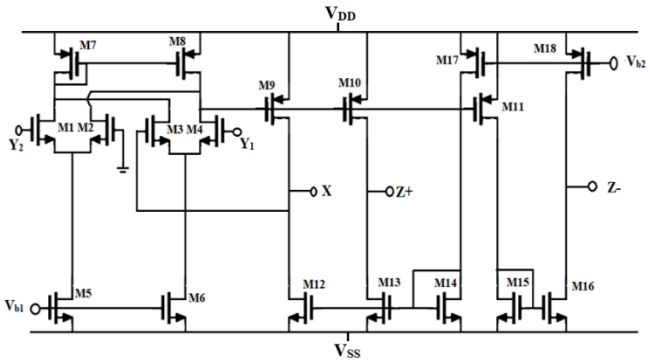



**Fig. 3.** Realization of DVCC using CMOS transistors

## 3 Used active building blocks (ABBs)

Two ABBs have been used in the proposed circuit emulator: A dual output OTA (operational transconductance amplifier) and a DVCC (differential voltage current conveyor). The OTA is a popular differential input transconductance amplifier IC with output currents given as $I_{\pm}=g_m(V_+ - V_-)$, where $V_+$ and $V_-$ are voltages applied at the + and – input terminals respectively and $g_m$ represents the transconductance gain. Following is the description of the employed configuration of the DVCC.

The DVCC was presented as a modified current conveyor in [15]. It has a long history as an analog circuit block and is mostly used in analog filter networks and higher-order oscillators, due to the different operations taking place at its input [16-18]. The diagrammatic depiction of the DVCC is given in Fig. 2 and the related admittance matrix is mentioned in Eqn. (6).

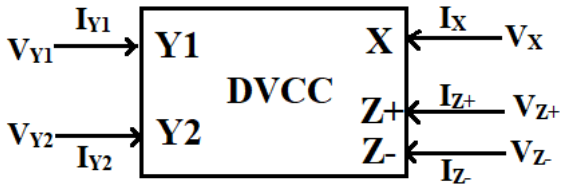



**Fig. 2.** The scheme of DVCC

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix} \quad (6)$$

There are several CMOS realizations exist in the available pieces of literature. In this work, we have used the standard DVCC implementation which was given in [19]. This CMOS implementation is presented in Fig. 3.

## 4 Proposed inverse memristor emulator circuit

The circuit schematic of the proposed inverse memristor emulator has been depicted in Fig. 4. It consists of a dual output OTA, DVCC, a grounded capacitor $C_1$, and a grounded resistor $R_1$. Capacitor $C_1$ is connected across the X port of the DVCC and the grounded resistor $R_1$ has been connected to the biasing terminal of the OTA. By using switch $S_1$, resistor $R_1$ can be switched between ports $Z_+$ and $Z_-$.

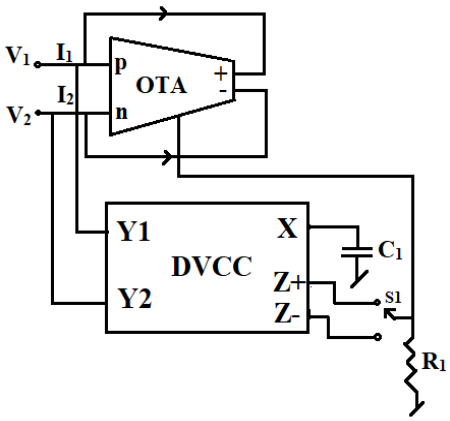



**Fig. 4.** Circuit connections of the proposed DVCC-OTA memristor emulator

After performing the respective circuit analysis by using Eqn. (6), we get the required current-voltage expression for the inverse memristor

$$I_{in} = k(V_1 - V_2)\left(R_1 C_1 \frac{d(V_1 - V_2)}{dt} - V_{ss} - V_{th}\right) \quad (7)$$

and $(I_1 = -I_2 = I_{in})$.

The equivalent flux-dependent conductance is obtained as

$$G(\varphi) = k\left(\pm R_1 C_1 \frac{d(V_1 - V_2)}{dt} - V_{ss} - V_{th}\right). \quad (8)$$

The "±" sign in Eqn. (8) corresponds to the incremental and decremental configuration of the realized inverse memristor. On connecting the grounded resistance $R_1$ to DVCC ports $Z_+$ and $Z_-$, the realized emulator

can be switched from the incremental to the decremental mode of operation. Also, it can be deduced from Eqn. (8) that resistance $R_1$ can be used to control the behaviour of the inverse memristor realized by the circuit.

## 5 Simulation results

To validate the provided inverse memristor emulator, a PSPICE simulation environment is utilized with 0.18 µm CMOS technology. The CMOS-implemented differential voltage current conveyor (DVCC) and dual output operational transconductance amplifier (DO-OTA) employ supply voltages of $V_{DD,SS} = \pm 0.9$ V. The chosen width/length (W/L) ratios of the CMOS transistors used in the DVCC and OTA implementations are detailed in Tables 2 and 3.

**Table 2.** Aspect ratios of MOS transistors employed in DVCC implementation

| Transistors | W/L ratio (µm/µm) |
|---|---|
| M1-M4 | 3.06/0.72 |
| M7-M8 | 9/0.72 |
| M9-M11 | 14.4/0.72 |
| M12-M16 | 0.72/0.72 |
| M5-M6, M17-M18 | 3.6/1.8, 3.6/0.072 |

**Table 3.** W/L ratios of CMOS transistors employed in the dual output OTA

| Transistors | W/L (µm/µm) |
|---|---|
| $M_1$-$M_2$, $M_9$- $M_{13}$ | 4/0.36 |
| $M_3$-$M_8$ | 13/0.36 |

Now, the functionality of the proposed inverse memristor can be scrutinized by subjecting it to a bipolar signal and observing the transient *v-i* plots. For this evaluation, a sinusoidal signal with a peak amplitude $V_P$ of 0.125 V is selected, and circuit para-meters are set as follows: $R_1$=10 kΩ and $C_1$=0.04 nF. Additionally, a biasing voltage of $V_{BS}$=0.8 V is applied to both terminals of the DVCC relative to the negative power supply. The investigation begins with the incremental mode of the realized inverse memristor (when switch $S_1$ is connected to $Z_+$). Subsequently, the key distinguishing characteristics of the inverse memristor are plotted in Fig. 5. These three curves are generated at different operating frequencies. It is evident that the area under the pinched hysteresis loop (PHL) lobes expands as the operating sinusoidal signal frequency is increased, aligning with the anticipated ideal property of the inverse memristor emulator.

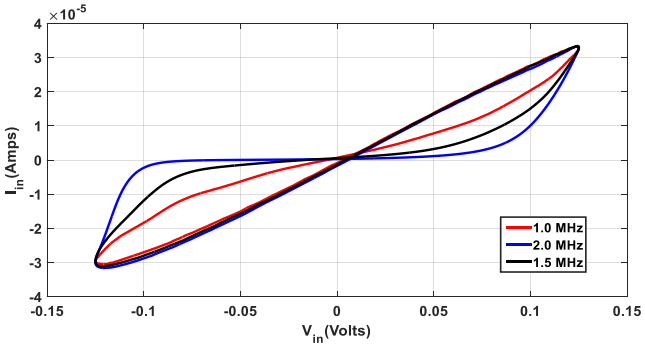



**Fig. 5.** Transient *v-i* loops of presented inverse memristor emulator at different operating frequencies

## 6 Application example

The proposed inverse memristor was used to extend the bandwidth of a memristor emulator. As outlined in Section 1, the interconnection of an inverse memristor with a memristor enables the manipulation of the frequency response of the memristor. It is imperative to note that linking a memristor with an inverse memristor yields a distinct function, the nature of which is contingent upon the elements in the shunt. However, we configure the coefficients of the inverse memristor in a manner that ensures the resultant circuit consistently functions as a memristor emulator. This novel memristor emulator can exhibit an expanded operating frequency range, allowing for a pinched hysteresis loop (PHL) response at significantly higher operating frequencies. This frequency range can be determined by judiciously adjusting the values of passive elements associated with the inverse memristor emulator circuit. To validate this application of the presented inverse memristor, we have selected the floating memristor emulator previously documented in [14]. This emulator, based on the modified voltage differencing current conveyor (MVDCC), is depicted in Fig. 6, and its corresponding PHL response with frequency variation is shown in Fig. 7. Notably, this memristor emulator demonstrates a satisfactory PHL response up to 1500 kHz for specific simulation parameters detailed in [14].

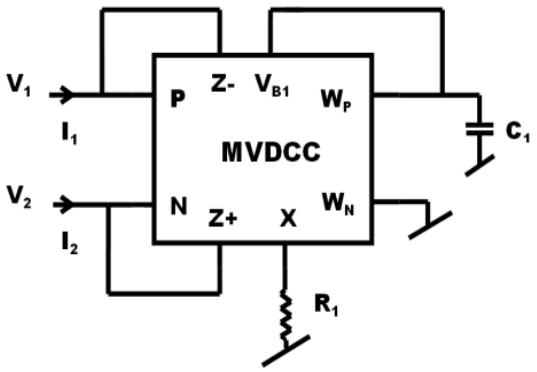



**Fig. 6.** Proposed MVDCC based configuration of a floating memristor emulator reported in [14]

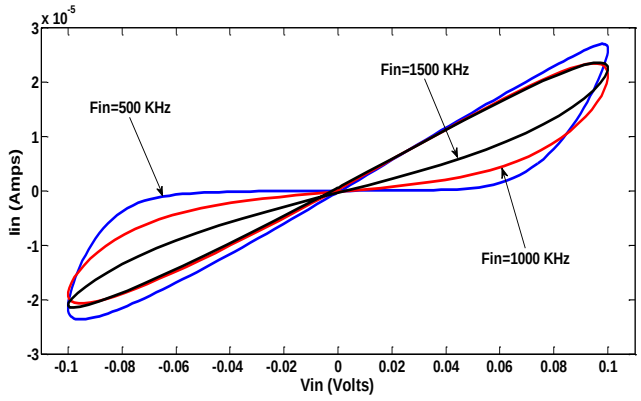



**Fig. 7.** Transient *v-i* characteristics of the memristor emulator proposed in [14]

Subsequently, we interconnect the presented inverse memristor emulator and the memristor emulator depicted in Fig. 6, placing them in parallel. Subsequent to plotting the transient characteristics between $V_{\text{in}}$ and $I_{\text{parallel}}$, illustrated in Fig. 3, the PHL response is obtained, as demonstrated in Figs. 8 and 9. Both plots correspond to the incremental and decremental modes of the utilized inverse memristor emulator, achieved by connecting switch $S_1$ to $Z_+$ and $Z_-$ respectively. Simulation results presented in Figs. 8 and 9 underscore that the incorporation of the inverse memristor leads to an expanded maximum operating frequency range. Specifically, a maximum operating frequency of up to 3 MHz and 5 MHz is achievable in the incremental and decremental modes, respectively.

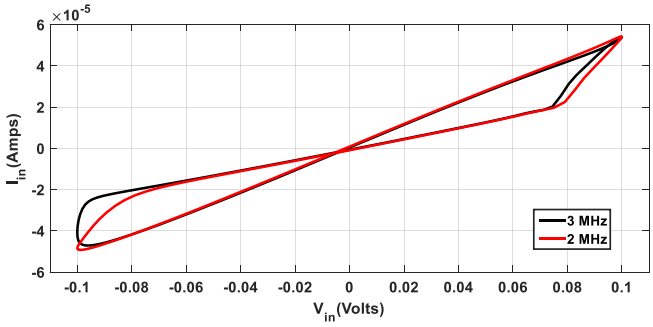



**Fig. 8.** Hysteresis behaviour of the described parallel connection given in Fig. 3 for inverse memristor parameters chosen as $R_1$=1 kΩ and $C_1$=0.01 nF

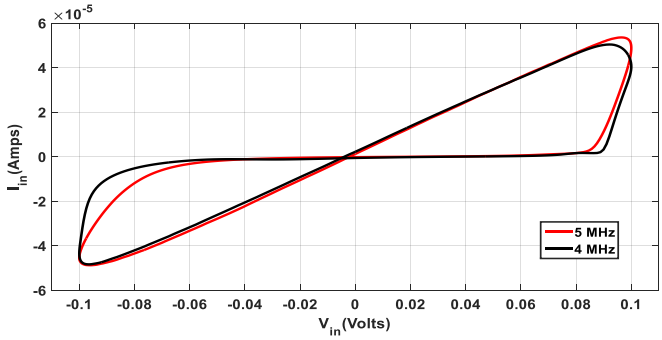



**Fig. 9.** PHLs for the decremental mode of the used inverse memristor with parameters values $R_1$=10 kΩ and $C_1$=0.04 nF

## 7 Implementation of the inverse memristor using off-the-shelf ICs

The LM13700 features two transconductance amplifiers that operate independently of each other. Utilizing the LM13700 IC, architecture of designed inverse memristor emulator is shown in Fig. 10.

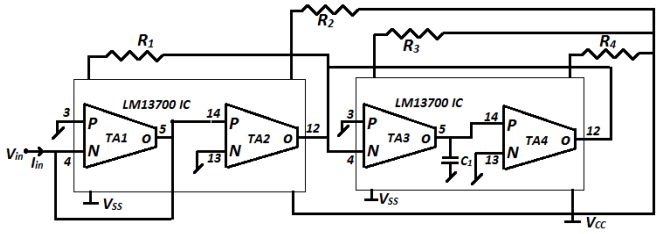
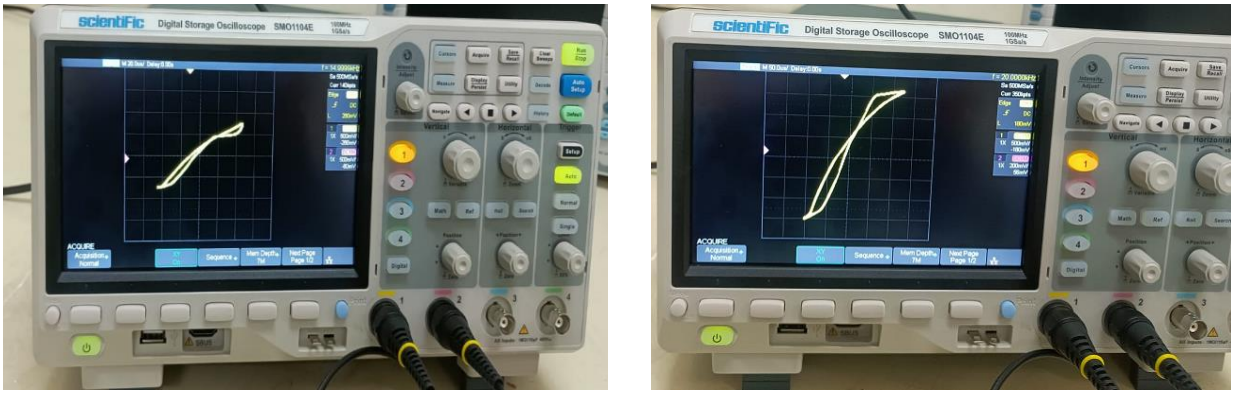



**Fig. 10.** Designed inverse memristor emulator using four transconductance amplifiers

The employed breadboard setup for Fig. 10 incorporates two LM13700 ICs and a differential amplifier utilizing the Op-Amp IC μA741. The differential amplifier serves the purpose of measuring the input current of the circuit, which is then transmitted to the digital storage oscilloscope (DSO) for the generation of the Lissajous pattern.

The transient *v-i* contours of the above circuit have been traced using the DSO and the results are depicted in Fig. 11 for two different operating frequencies. The plots are generated at a sinusoidal signal with a peak value of $V_{\text{m}} = 5$ V. The LM13700-based emulator has been tested for the passive element values selected as $R_1 = R_2 = R_3 = R_4 = 33$ kΩ, $C_1 = 100$ nF with power supply voltage $V_{\text{EE,CC}} = \pm 15$V.




(a) (b)

**Fig. 11.** Transient *v-i* curves of the LM13700-based inverse memristor emulator (given in Fig. 10) on the DSO screen: (a) for 15 kHz, (b) for 20 kHz

## 8 Conclusion

The inverse memristor has historically garnered little attention from circuit designers, primarily due to its perceived lack of utility in storage and switching applications, in contrast to traditional memristor elements. While its non-linear inductive nature finds application in chaotic oscillators, the abundance of compact memristor emulators in non-linear scenarios has rendered the realization of the inverse memristor seemingly redundant. However, the innovative application proposed in this work aims to inspire circuit researchers to actively explore and implement this overlooked element. The approach presented is both simple and effective, leveraging the inverse frequency dependency of the inverse memristor in comparison to a standard memristor. This exploitation results in a memri-stive hysteresis response at higher operating frequencies, a crucial aspect for memristive switching applications functioning at elevated frequencies. The compact design of the inverse memristor emulator in this work enhances its applicability in various non-linear memristive applications, especially when compared to bulkier circuit architectures employed by some popular memristor emulators. Simulation results obtained validate the functionality of the proposed circuit, aligning with other theoretical discussions. Additionally, the article showcases experimental results for an LM13700 implementation, further affirming the viability of the proposed approach.

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