Journal of Electrical Engineering, Vol. 75, No. 1, 2024, pp. 47-55

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PAPERS

Design and implementation of a current-fed dual active bridge converter for an AC battery

Tuan Anh Do[1,2], Quang Dich Nguyen[2], Phuong Vu[1*]

Home battery has become more and more popular in which the AC battery is a trending product along with the AC-coupled system. The energy conversion of an AC battery commonly consists of a two-stage power converter to flexibly connect to the wide-range input battery voltage and different grid or load types. This study specifically concentrates on the DC/DC stage which plays an important role in transferring power with the battery. In addressing the need for isolation, bidirectional power flow, and limited battery current ripple, the Current-fed Dual Active Bridge (CFDAB) structure is chosen for this stage. This paper presents a comprehensive design for the CFDAB converter for an AC battery application, especially a technical solution focusing on zero voltage switching is applied to increase the efficiency of the converter. Finally, an experimental prototype is carried out to validate the performance of the CFDAB converter in both two modes of the power flow.

Keywords: AC battery, current-fed dual active aridge, zero voltage switching

1 Introduction

In recent years, home batteries have become increasingly popular due to their cost-effectiveness in sharing energy capacity and the growing trend of enhancing self-reliance in energy consumption [1-3]. These domestic applications involve integrating various distributed power sources and consumption elements, such as photovoltaic (PV) systems, battery energy storage systems, the grid, and household loads. Two common topologies for home batteries are the AC-coupled and DC-coupled systems. This research specifically focuses on the AC-coupled system based on its adaptability to retrofit existing residential PV installations, flexibility in accommodating additional modules, and isolation for the battery system. Within the AC-coupled topology, the AC Battery, which combines both the battery and the power converter, has been introduced by numerous well-known manufacturers. Some products even incorporate second-life batteries [4-6] for economic and environmental purposes. The power converter of the AC battery includes a two-stage energy conversion as shown in Fig. 1: the DC/DC stage connecting to the battery and the DC/AC stage connecting to the grid and load. This paper specifically focuses on the DC/DC stage, in which a bidirectional isolated converter is applied to exchange power between the battery and the DC-link voltage.

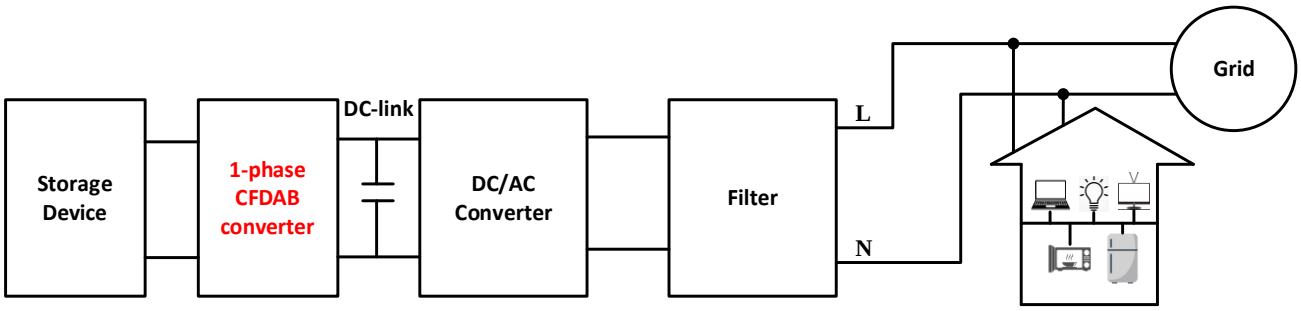

Fig. 1. Structure of an AC battery for domestic application using current-fed dual active converter

[1] School of Electrical and Electronic Engineering, Hanoi University of Science and Technology, Hanoi, Vietnam
[2] Institute for Control Engineering and Automation, Hanoi University of Science and Technology, Hanoi, Vietnam
*phuong.vuhoang@hust.edu.vn

https://doi.org/10.2478/jee-2024-0007, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

In recent years, the dual active bridge (DAB) has gained attention as an isolated DC/DC converter, attributed to its notable advantages including high-frequency isolation capability, soft switching characteristics, and bidirectional power flow [7-9]. Nevertheless, a drawback lies in the direct supply of voltage to the power circuit, leading to a high battery current ripple. This, in turn, results in extra bulky filters, increased costs, and a reduced system lifespan [10]. Additionally, due to DC bias issues, series capacitors with the primary transformer or complex modified modulation are required to avoid core flux saturation [11].

To address the aforementioned issues, this paper proposes a particular technological solution to optimize the performance of DC/DC converters used in an AC Battery. Firstly, a current-fed DC/DC converter with a Current Fed Dual Active Bridge (CFDAB) structure [12,13] is employed, where the interleaved boost circuit on the primary side helps reduce current stress, providing soft switching capabilities like Zero Voltage Switching (ZVS) to contribute to minimizing switching losses, especially at high frequencies. This topology could also be flexibly modified for the specific application [14,15].

Secondly, silicon carbide (SiC) MOSFET technology and Litz wire winding are chosen to reduce losses in semiconductor switches and transformers across all frequency ranges. Litz wire has recently become a promising material in the power electronics field, allowing inductors and transformers to operate at high currents with low resistance [16], achieving minimal losses at operating frequencies from tens to hundreds of kilohertz [17]. The Litz wire also helps minimize the skin effect and reduce losses caused by eddy currents [18], lowering the operating temperature of the system and simplifying the heat dissipation design. SiC MOSFET technology has significant advantages over conventional Si MOSFETs: it operates at higher voltage levels with greater thermal endurance, lower conduction resistance, and smaller gate charge leading to shorter switching times, thus reducing losses due to valve switching, and it can operate at higher frequencies [19-20]. Therefore, the overall losses of SiC mosfet are significantly reduced compared to conventional Si technology.

To validate the effectiveness of the proposed solution, a 3.3 kW experimental system is carried out. The obtained results make a good agreement with the theoretical design: all switches achieve ZVS capability, and the efficiency of the converter reaches up to 96.5%.

2 Operation principle

Figure 2 presents the structure of the CFDAB converter, comprising two primary parts: the interleaved boost circuit and the Dual Active Full-Bridge circuit. Within the interleaved boost circuit, two DC inductors function as distinct current sources. Inductor L_{dc1} collaborates with the left leg with switches Q_1 and Q_{1a}, which makes the first boost converter. Simultaneously, the right leg, equipped with switches Q_2 and Q_{2a}, collaborates with inductor L_{dc2} to form the second boost converter. These boost converters operate with a 180° phase shift, creating an interleaved boost circuit where the boost voltage is maintained constant by the clamp capacitor C_c. Besides, the Dual Active Full-Bridge circuit comprises two H-bridge modules positioned on two sides of an isolated high-frequency transformer with a turn ratio of N:1. The input capacitor and output capacitor voltages are defined as the Low-Voltage Side (LVS) and High-Voltage Side (HVS), respectively. The direction of the power flow between the LVS and the HVS side is determined by the sign of the phase-shifted angle. The AC inductor L_r, comprising the primary-referred transformer leakage inductor and the auxiliary leakage inductor, functions as a power link connecting the two sides of the transformer.

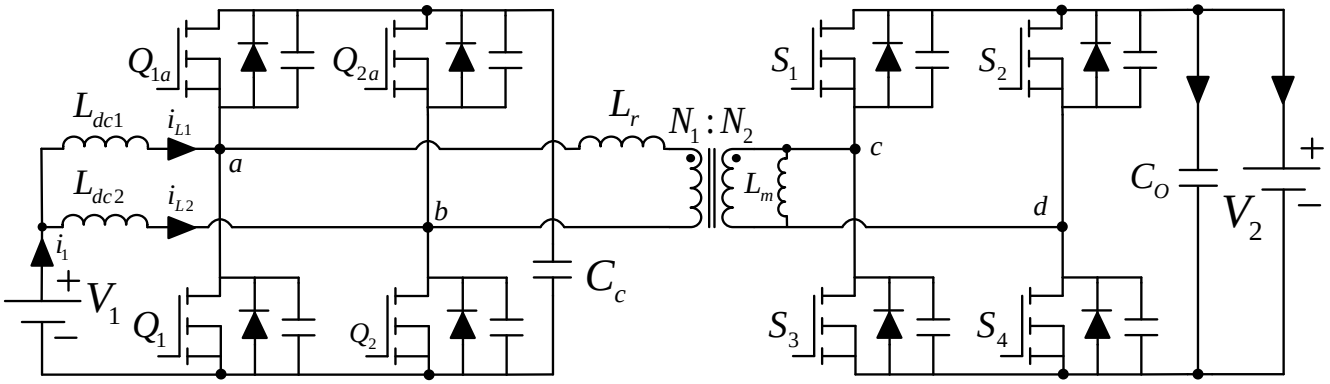

Fig. 2. The structure of the CFDAB converter

The significant reduction in current ripple by the interleaved boost part, the isolation with bidirectional power flow, and the flexible gain factor make the CFDAB converter suitable for home battery applications in general and the AC Battery in particular.

2.1 Pulse width modulation method

To address issues related to voltage ratio variations and minimize conduction losses in power transfer stages, the PWM plus phase-shifted (PPS) approach is employed. In this method, the duty cycle for HVS switches is fixed at 50%, while the duty ratio for the primary LVS switches Q_1 and Q_2 is a variable D. However, during non-power transfer stages of PPS, there is a notable circulation loss with a high spike in leakage current.

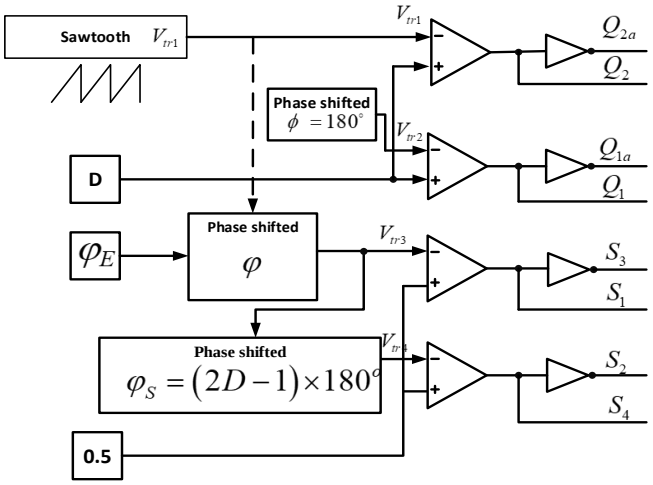

Fig. 3. Modulation technique DPDPS [10]

In this study, an extra phase shift is introduced through the PWM plus Double Phase-Shifted (DPDPS) method [10] denoted as $(2D-1)\times T_S/2$, aimed at eliminating the spike in leakage current. Figure 3 outlines the modulation strategy for the CFDAB converter, specifying that the phase shifts between $Q_1 - Q_2$, $Q_2 - S_1$, and $S_1 - S_4$ are 180˚, φ, and φ_S, respectively. Parameter φ_E plays a crucial role in determining power flow and direction, with $\varphi_E > 0$ representing operation in boost mode where power flows from the LVS to the HVS and vice versa. Through the utilization of DPDPS modulation, Fig. 4 [10] illustrates eight operational modes within a single switching period, showcasing the main current and voltage waveform.

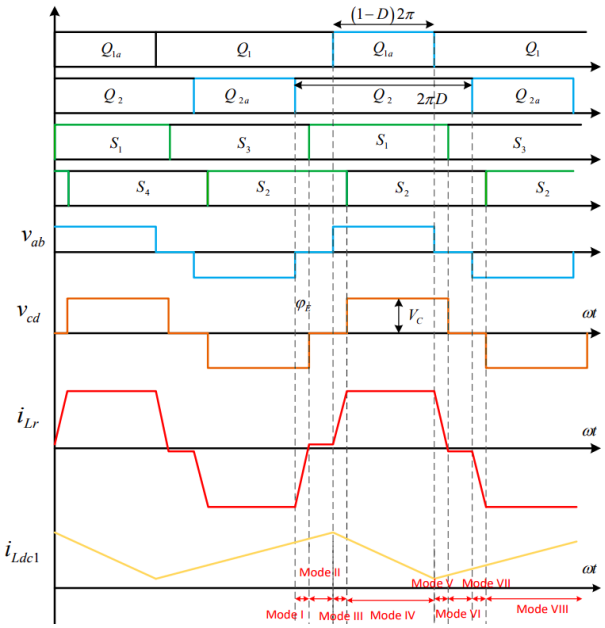

Fig. 4. Key waveform of CFDAB converter under the DPDPS modulation method

2.2 ZVS analysis

Specifically, at the turn-on interval of each switch, there should be a sufficient current i_{ZVS} to discharge the parasitic capacitance of the switches within the particular dead time. The direction of the leakage current i_{Lr} is chosen to be the same as that of the inductor current i_{Ldc1}. Table 1 illustrates the ZVS condition for each switch of the converter. These conditions will be analyzed in the primary-side and the secondary-side switches of the converter.

Table 1. ZVS conditions for 8 switches

Switches	ZVS condition at turn-on interval
Q_{1a}	$i_{Ldc1} - i_{Lr} > i_{ZVS}$
Q_1	$i_{Lr} - i_{Ldc1} > i_{ZVS}$
Q_{2a}	$i_{Ldc2} + i_{Lr} > i_{ZVS}$
Q_2	$i_{Ldc2} + i_{Lr} < -i_{ZVS}$
S_1	$i_{Lr} > i_{ZVS}$
S_2	$i_{Lr} < -i_{ZVS}$
S_3	$i_{Lr} < -i_{ZVS}$
S_4	$i_{Lr} > i_{ZVS}$

2.2.1 Deadtime calibration

Deadtime is commonly applied to avoid the short-circuit phenomenon. Moreover, in this situation, an appropriate deadtime needs to be utilized so that the voltage on the parasitic capacitor can be discharged to zero before the drain current starts to rise. However, a large deadtime could make the current flow in the reverse direction through the body diode, hence the drain voltage V_{ds} then rises again.

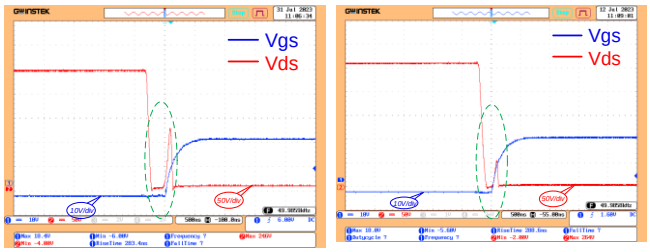

Fig. 5. Turn-on interval of switch Q_{1a} with different deadtime: a) T_d=0.4 µs, b) T_d=0.35 µs

Figure 5 illustrates the drain-to-source voltage V_{ds} and the gate voltage V_{gs} in the turn-on interval of an upper switch Q_{1a} in the open-loop mode with the input voltage of 50 V and the resistor of 128 Ω. As per the above analysis, the ZVS current for this switch is larger than that of the lower switch, and the same deadtime is applied for each leg. As a result, the deadtime could to larger than the sufficient time to discharge the parasitic capacitor. In Fig. 5a, the V_{ds} voltage rises again from zero to a peak of about 100 V, which generates more switching loss in the turn-on period. In Fig. 5b, this peak voltage has decreased significantly by reducing the deadtime from 0.4 µs to 0.35 µs. Hence, a suitable deadtime will be chosen for a particular operating load.

2.2.2 DC inductor selection

The DC inductors L_1 and L_2 directly determine the ripple of the DC-current and the ZVS condition of the primary-sided switches as shown in Table 1. Moreover, it is more difficult to achieve ZVS on the lower switches compared to the upper ones. Therefore, the comparison of the turn-on interval of the lower switch Q_1 between 2 DC inductor values is given in Fig. 6 with the same test condition in section *2.2.1*.

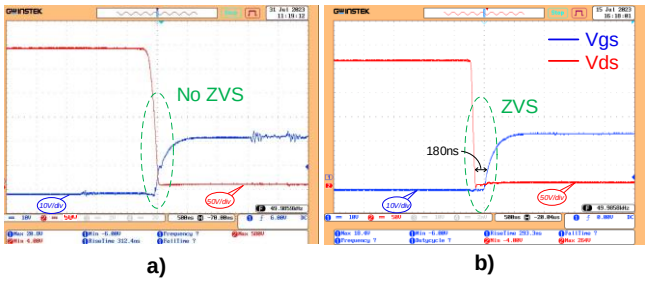

Fig. 6. Voltage response of switch Q_1 with different DC inductors: a) L_{dc}=*330* µH, b) L_{dc}=*130* µH

With the large DC inductor of 330 µH, the discharging current is not enough and the ZVS cannot be achieved on switch Q_1 as shown in Fig. 6a. By reducing the inductor value to 130 µH, the current ripple significantly increases which leads to the higher i_{ZVS} and the ZVS is achieved as shown in Fig. 6b.

2.2.3 Determining the additional phase shift Δφ

To obtain a bias current i_{bias} for discharging the parasitic capacitance of switches S_1 and S_3 in this interval, a phase-shift angle $\Delta\varphi$ needs to be set [10]. The bias current needs to be chosen large enough so that the parasitic capacitor can be discharged completely within the deadtime. However, if the i_{bias} current is too high, it will increase losses as this is a circulating period. The response of switch S_1 in boost mode is taken as an example, with the same scenario outlined in section *2.2.1*, illustrated in Fig 7. Figure 7a shows that the hard-switching occurs when S_1 turns on with a small $\Delta\varphi$ (5°). At this condition, by increasing $\Delta\varphi$ to 8°, S_1 could just achieve ZVS and this value be selected for the phase-shifted angle $\Delta\varphi$ instead of continuously increasing to avoid the power losses.

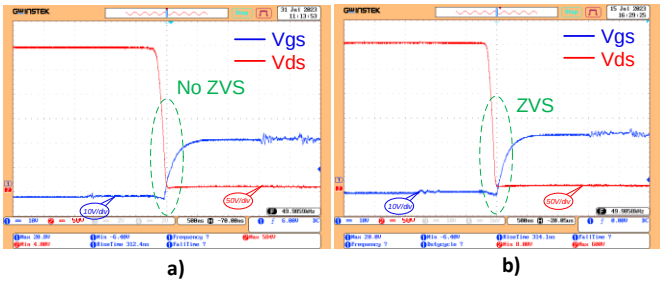

Fig. 7. Turn-on interval of switch S_1 with different values of $\Delta\varphi$: a) $\Delta\varphi = 5°$, b) $\Delta\varphi = 8°$

2.2.4 Leakage inductor selection

Besides the influence of power transfer, the value of the leakage inductance also affects the ZVS condition of the switches on both sides, particularly on the secondary side. Reducing the leakage inductance will increase the primary-side current ripple and help the primary-sided switches achieve ZVS more easily. However, this reduction in leakage inductance decreases the stored energy in the leakage inductance, making it more difficult for the secondary-side switches to achieve soft switching. The response of switch S_1 in boost mode is taken for example with the same scenario outlined in section *2.2.1*. With a similar phase-shift angle, a small leakage inductance (13 μH) is insufficient for switch S_1 to achieve soft switching. However, by increasing the value of the leakage inductance to 16 μH, switch S_1 begins to achieve ZVS.

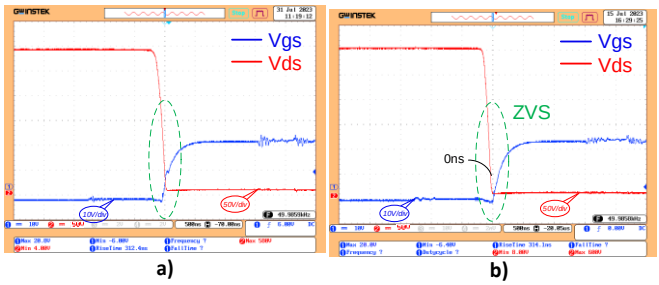

Fig. 8. Turn-on interval of switch S_1 with different L_r: a) L_r=13 μH, b) L_r=16 μH

Therefore, a suitable combination is required among choosing the values of the DC inductor, leakage inductor, phase-shift angle, and deadtime to simultaneously achieve soft switching of the switches and avoid circulating losses, ultimately aiming to enhance the efficiency of the converter.

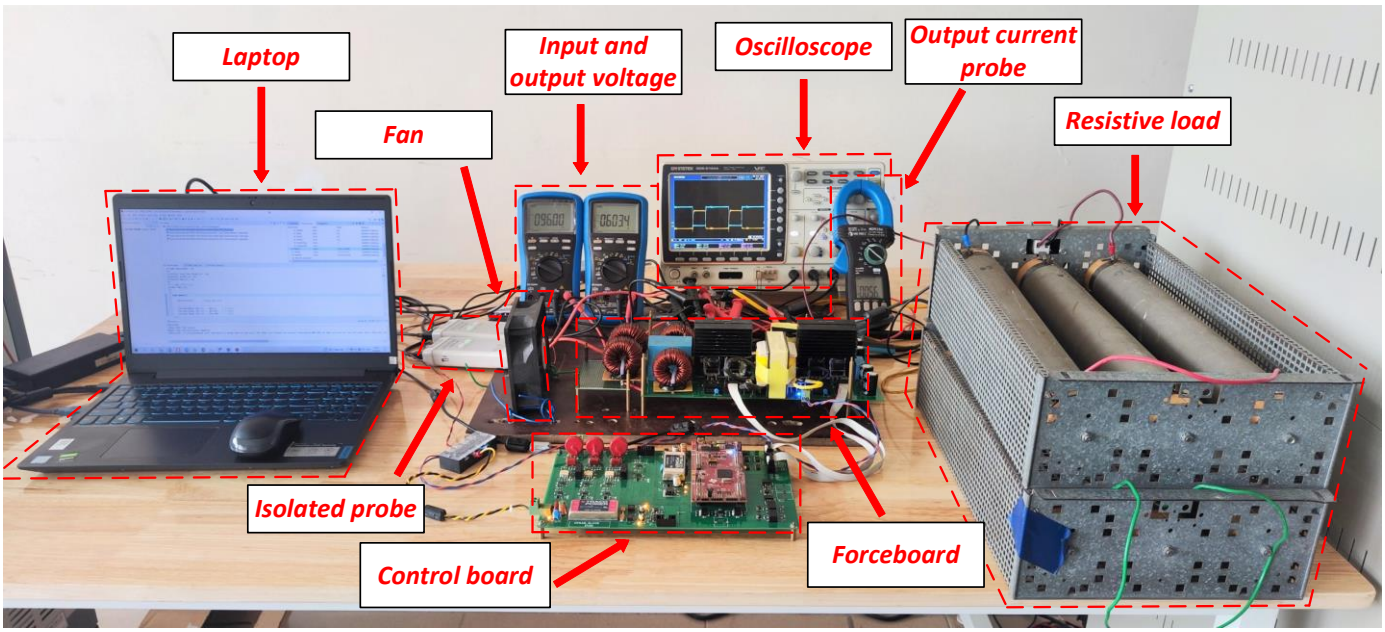

Fig. 9. Experimental prototype of CFDAB converter

3 Experimental results

To verify the theoretical basis of soft switching and the operational principles of the CFDAB converter, a 3.3 kW experimental prototype has been carried out with the parameters being presented in Table 2. The experimental system shown in Fig. 9 includes the CFDAB converter, the control circuit, the resistor load, and a DC power supply model ITECH IT6018C-1500-40.

The control algorithm is programmed in the control kit Launchpad TMS320F28379D. To display and collect the data, a GW INSTEK GDS-2104A Digital Oscilloscope is used with the isolated voltage probe Micsig DP10013 and the current probe Micsig CP2100A.

Table 2. Key specification of the CFDAB prototype

Components	Parameter
Primary-sided switches	C2M0040120D, 1200 V, 60 A
Secondary-sided switches	C2M0080120D, 1200 V, 36 A
Transformer T	Ferrite core EE65, turn ratio 4:9 Number of primary turns N_1=12 Magnetic inductor L_m=411 µH leakage inductor L_k=1.5 µH
Auxiliary leakage inductor L_s	Ferrite core EC42, 16 turns L_s=11.5 µH
Total leakage inductor L_r	$L_r = L_k + L_s$ = 13 µH
DC inductor	130 µH
Clamp capacitor	50 µF, 920 V
Input capacitor	220 µF, 400 V

The SiC Mosfets C2M0040120D and C2M0080120D are respectively utilized for the primary-sided and secondary-sided switches of the CFDAB converter to minimize switching losses and enhance the efficiency of the converter. For this converter, the total leakage inductor is designed to include the leakage inductor on the primary side of the transformer and an auxiliary leakage inductor L_s. Furthermore, Litz wire is employed for winding the main transformer and the auxiliary leakage inductance to reduce losses induced by eddy currents. With the selected frequency for the converter is 50 kHz, based on the skin depth relationship, the corresponding diameter for the Litz wire is 0.1 mm.

3.1 Experimental results in boost mode

The 3-level primary voltage is lagging in phase compared to the secondary voltage of the transformer, as shown in Fig. 11, ensuring energy transfer from the LVS to the HVS in boost mode. The current through the leakage inductor has the same waveform in the theoretical analysis, with an aiding bias current to help switches S_1 and S_3 achieve ZVS.

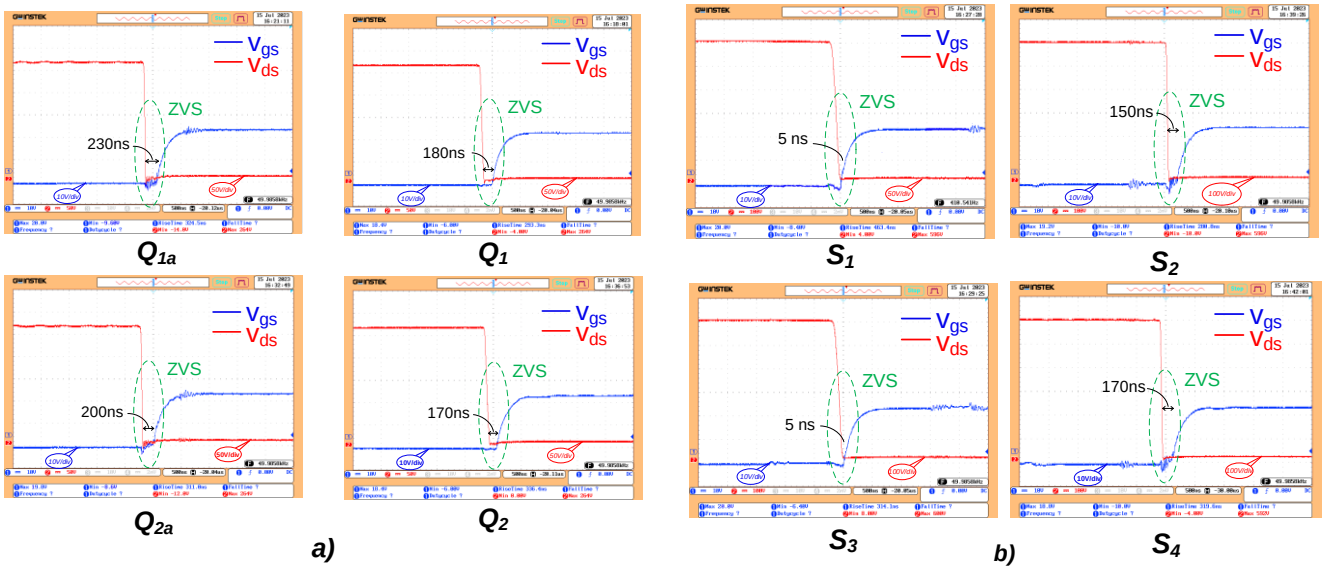

Fig. 10. Experimental results in boost mode
a) ZVS on primary switches, b) ZVS on secondary switches

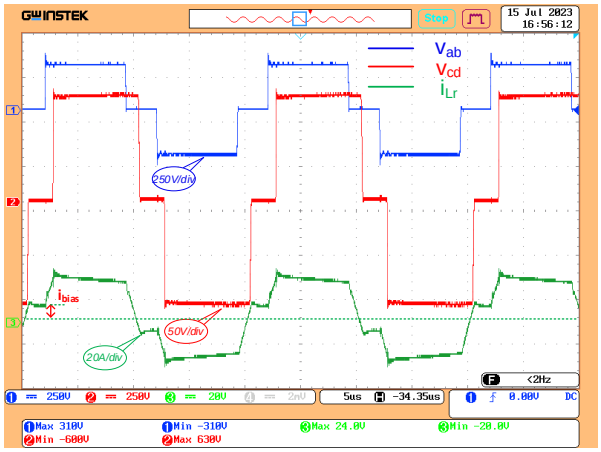

Fig. 11. Transformer voltage V_{ab}, $V_{cd,}$ and leakage current i_{Lr} in boost mode

By adjusting the values of the inductors, the phase-shift angle $\Delta\varphi$, and the deadtime, all 8 switches achieve ZVS at a power rate of 3300W, as depicted in Fig. 10. In this mode, the primary-side switches Q_{1a}, Q_{2a}, and the secondary-side switches S_2, S_4 achieve ZVS more easily compared to other switches with a larger discharge current i_{ZVS}. This is illustrated by a longer time for the voltage to reach zero before the turn-on signal. The converter obtains an efficiency exceeding 94% across the entire power range and a maximum efficiency of 96.4% at the power rate, as shown in Fig. 12.

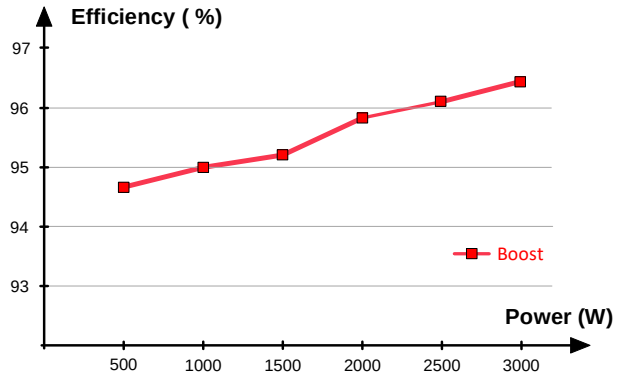

Fig. 12. Efficiency evaluation in boost mode

3.2 Experimental results in buck mode

Similarly, in buck mode, all 8 switches achieve ZVS at a power rate, as depicted in Fig. 13. The primary-side switches Q_1, Q_2, and the secondary-side switches S_1, and S_3 achieve ZVS more easily compared to other switches with a larger discharge current i_{ZVS}. This is shown by a longer time for the voltage to reach zero before the turn-on signal.

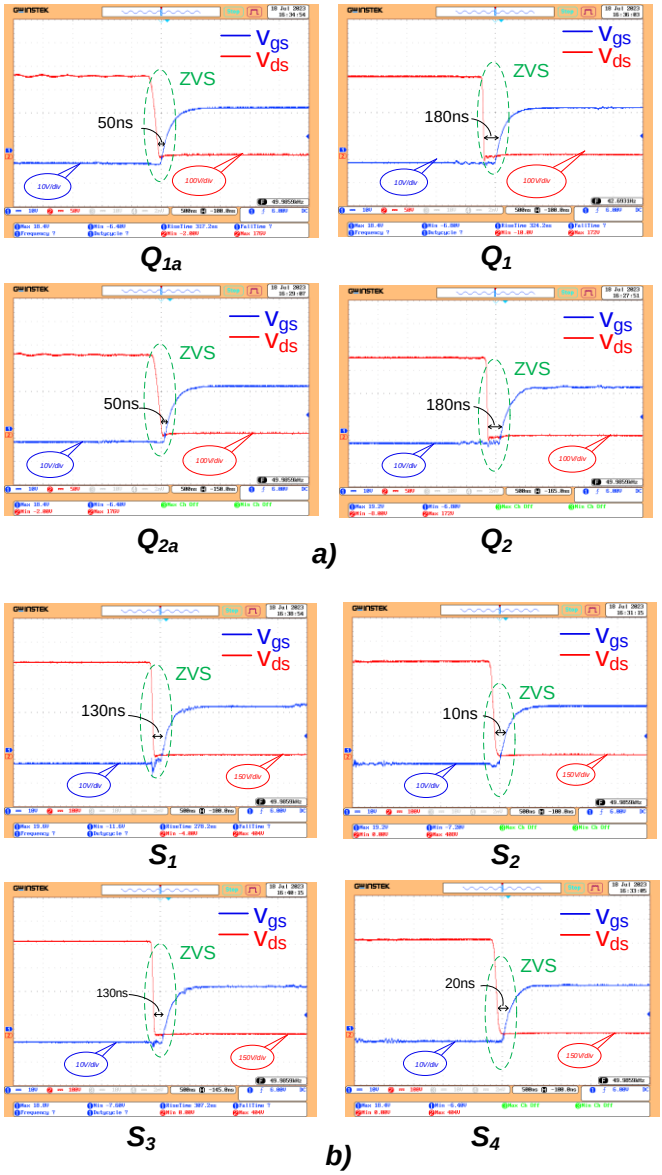

Fig. 13. Experimental results in boost mode: a) ZVS on primary switches, b) ZVS on secondary switches

The 3-level primary voltage is leading in phase compared to the secondary voltage of the transformer, as shown in Fig. 14, ensuring energy transfer from the HVS to the LVS in buck mode. The current through the leakage inductor has the same waveform in the theoretical analysis, with an aiding bias current to help switches S_2 and S_4 achieve ZVS.

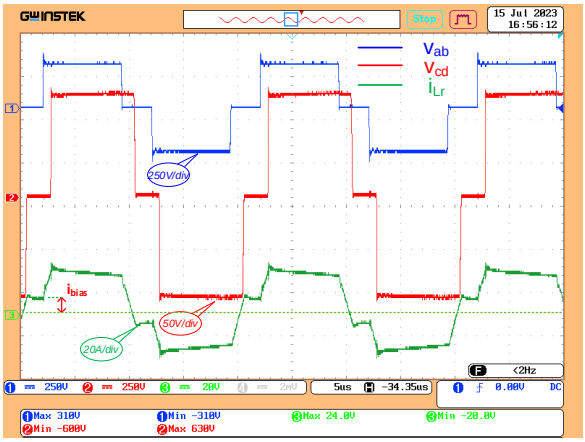

Fig. 14. Voltage and current response in buck mode

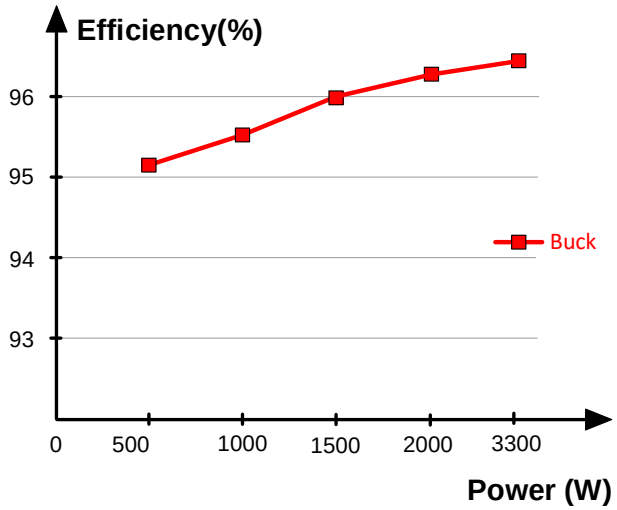

Fig. 15. Efficiency evaluation in buck mode

In buck mode, the converter obtains an efficiency exceeding 95% throughout the power range and the maximum efficiency of 96.5% at the power rate, as shown in Fig. 15.

4 Conclusions

The paper proposes technical solutions to enhance the performance of an isolated DC/DC converter used in an AC battery. By selecting the CFDAB structure, the reduced current ripple, bidirectional power flow and the isolation is obtained for the AC Battery. A detailed designed by adjusting deadtime, DC inductor and leakage inductor are presented to achieve ZVS for all the switches of the converter. Furthuremore, to increase the efficiency of the converter, the SiC Mosfet technology and Litz wire are applied in an experimental prototype. Experimental results demonstrate that the system achieves all desired technical features, including bidirectional ZVS switching (corresponding to both boost and buck modes), and the actual efficiency of the converter reaches 96.5%.

Acknowledgment

This research is funded by the Hanoi University of Science and Technology (HUST) under project number T2022-TĐ-001.

References

[1] J. Zich and J. Jandik, "Active Battery Management System for Home Battery Energy Storage," 2020 *21st International Scientific Conference on Electric Power Engineering (EPE)*, Prague, Czech Republic, 2020, pp. 1-4, doi: 10.1109/EPE51172.2020.9269172.

[2] T. Tungjittrong and N. Teerakawanich, "Design and Sizing of Home PV/Battery System with Energy Cost Constraint using Web Application," *2021 9th International Electrical Engineering Congress (iEECON)*, Pattaya, Thailand, 2021, pp. 129-132, doi: 10.1109/iEECON51072.2021.9440066.

[3] Isdawimah, N. Nadhiroh and A. D. Aji, "Optimization of Stand Alone Solar Home System with Battery, "*2021 4th International Conference of Computer and Informatics Engineering (IC2IE)*, Depok, Indonesia, 2021, pp. 500-504, doi: 10.1109/IC2IE53219.2021.9649406.

[4] E. Hossain, D. Murtaugh, J. Mody, H. M. R. Faruque, M. S. Haque Sunny and N. Mohammad, "A Comprehensive Review on Second-Life Batteries: Current State, Manufacturing Considerations, Applications, Impacts, Barriers & Potential Solutions, Business Strategies, and Policies," in *IEEE Access*, vol. 7, pp. 73215-73252, 2019, doi: 10.1109/ACCESS.2019.2917859.

[5] J.-M. Timmermans *et al.*, "Batteries 2020 — Lithium-ion battery first and second life ageing, validated battery models, lifetime modelling and ageing assessment of thermal parameters," *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, Germany, 2016, pp. 1-23, doi: 10.1109/EPE.2016.7695698.

[6] H. Li, M. Alsolami, S. Yang, Y. M. Alsmadi and J. Wang, "Lifetime Test Design for Second-Use Electric Vehicle Batteries in Residential Applications," in *IEEE Transactions on Sustainable Energy*, vol. 8, no. 4, pp. 1736-1746, Oct. 2017, doi: 10.1109/TSTE.2017.2707565.

[7] J. -Y. Lee, H. -S. Kim and J. -H. Jung, "Enhanced Dual-Active-Bridge DC–DC Converter for Balancing Bipolar Voltage Level of DC Distribution System," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 12, pp. 10399-10409, Dec. 2020, doi: 10.1109/TIE.2019.2959503.

[8] D. Das and K. Basu, "Optimal Design of a Dual-Active-Bridge DC–DC Converter," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 12, pp. 12034-12045, Dec. 2021, doi: 10.1109/TIE.2020.3044781.

[9] S. Shao *et al.*, "Modeling and Advanced Control of Dual-Active-Bridge DC–DC Converters: A Review," in *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1524-1547, Feb. 2022, doi: 10.1109/TPEL.2021.3108157.

[10] D. Sha and G. Xu, "High-Frequency Isolated Bidirectional Dual Active Bridge DC–DC Converters with Wide Voltage Gain," *CPSS Power Electronics Series*.

[11] D. Atkar, P. Chaturvedi, F. Pellitteri, P. Nachankar and S. Chaitanya, "DC Bias Abatement in Dual Active Bridge Converter using Covalent Active and Passive Components," *2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, Birmingham, United Kingdom, 2022, pp. 1-6, doi: 10.1109/CPE-POWERENG54966.2022.9880875.

[12] P. Vu, D. Anh, H. D. Chinh, “A Novel Modeling and Control Design of the Current-Fed Dual Active Bridge Converter under DPDPS Modulation,” *Engineering, Technology and Applied Science Research*, *v*ol 11, No. 2, pp. 7054-7059, 2021. doi:10.48084/etasr.4067.

[13] K. Bathala, D. Kishan, N. Harischandrappa, Soft Switched Current Fed Dual Active Bridge Isolated Bidirectional Series Resonant DC-DC Converter for Energy Storage Applications. *Energies* 2023, *16*, 258. https://doi.org/10.3390/en16010258

[14] E. Hossain, D. Murtaugh, J. Mody, H. M. R. Faruque, M. S. Haque Sunny and N. Mohammad, "A Comprehensive Review on Second-Life Batteries: Current State, Manufacturing Considerations, Applications, Impacts, Barriers & Potential Solutions, Business Strategies, and Policies," in *IEEE Access*, vol. 7, pp. 73215-73252, 2019, doi: 10.1109/ACCESS.2019.2917859.

[15] D. Sha, Y. Xu, J. Zhang and Y. Yan, "Current-Fed Hybrid Dual Active Bridge DC–DC Converter for a Fuel Cell Power Conditioning System With Reduced Input Current Ripple," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 8, pp. 6628-6638, Aug. 2017, doi: 10.1109/TIE.2017.2698376.

[16] A. Rosskopf and C. Brunner, "Enhancing Litz Wire Power Loss Calculations by Combining a Sparse Strand Element Equivalent Circuit Method With a Voronoi-Based Geometry Model," in *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 11450-11456, Sept. 2022, doi: 10.1109/TPEL.2022.3169992.

[17] I. Reese and C. R. Sullivan, "Litz wire in the MHz range: Modeling and improved designs," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-8

[18] T. Guillod, J. Huber, F. Krismer and J. W. Kolar, "Litz wire losses: Effects of twisting imperfections," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-8

[19] L. F. S. Alves, P. Lefranc, P.-O. Jeannin and B. Sarrazin, "Review on SiC-MOSFET devices and associated gate drivers,"*2018 IEEE International Conference on Industrial Technology (ICIT)*, Lyon, France, 2018, pp. 824-829, doi: 10.1109/ICIT.2018.8352284.

[20] Y. Duan, Y. -L. Zhang, J. Q. Zhang and P. Liu, "Development of SiC Superjunction MOSFET: A Review," 2022 *19th China International Forum on Solid State Lighting & 2022 8th International Forum on Wide Bandgap Semiconductors (SSLCHINA: IFWS)*, Suzhou, China, 2023, pp. 13-17, doi:10.1109/SSLChinaIFWS57942.2023.10071020.

Tuan Anh Do received his B.S. and M.S. degrees in control engineering and automation from Hanoi University of Science and Technology, Ha Noi, Vietnam in 2019 and 2021, respectively. Since 2022, he has started to study for his PhD degree in control engineering and automation at Hanoi University of Science and Technology, Vietnam. His research interests include power electronics and control systems.

Quang Dich Nguyen received a B.S. degree in electrical engineering from the Hanoi University of Technology, Hanoi, Vietnam, in 1997. He received an M.S. degree in electrical engineering from the Dresden University of Technology, Dresden, Germany, and a Ph.D. from Ritsumeikan University, Kusatsu, Japan, in 2003 and 2010, respectively. Since 2000, he has been with the Hanoi University of Science and Technology, Vietnam, where he is currently an Associate Professor and Executive Dean of the Institute for Control Engineering and Automation. His research interests include magnetic bearings, self-bearing motors, and sensorless motor control.

Phuong Vu received his B.S., M.S., and Ph.D. degrees from Hanoi University of Science and Technology, Vietnam, in 2006, 2008, and 2014, respectively, all in Control Engineering and Automation. Since 2006 he has been employed at Hanoi University of Science and Technology, where he is a lecturer and researcher at School of Electrical Engineering, and currently is an Associate Professor. His research interests include modeling and controlling power electronics converters for applications.

Received 14 November 2023