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Design and verification of down asynchronous counter using toggle flip-flop in QCA

Rohit Kumar Shaw, Angshuman Khan*

This study presents an innovative single-layered toggle flip-flop with highly polarized output designed specifically for Quantum-dot Cellular Automata (QCA), a cutting-edge nanocomputing approach. Building on the capabilities of this advanced flip-flop, a two-bit asynchronous down (ripple) counter was developed using QCADesigner 2.0.3, all within the QCA framework. The counter exhibits exceptional scalability and reliability, addressing key challenges in QCA circuit design. Energy efficiency and cost-effectiveness are standout features of the design, with a 53% improvement in energy efficiency and a 38% reduction in QCA-specific cost, as verified by QCADesigner-E 2.2 simulations. Furthermore, the physical stability of the proposed circuit was thoroughly examined through kink energy calculations, highlighting its robustness. These optimizations were achieved by avoiding complex crossovers and leveraging the benefits of the enhanced flip-flop architecture. The results underscore the significant potential of QCA in improving digital circuit performance, paving the way for more efficient, scalable, and cost-effective nanoelectronic designs and pushing the boundaries of next-generation nanocomputing solutions.

Keywords: asynchronous counter, QCA, T flip flop, ripple counter, kink energy

1 Introduction

Numerous fundamental and technical challenges in traditional CMOS technology have been encountered as physical limits such as drain-induced barrier lowering, velocity upgradation, sub-threshold leakage current, etc., and short channel effects are approached while scaling and shrinking the transistors to satisfy Moore's law. These lead to excessive heat generation, higher power consumption, and quantum mechanical phenomena such as electron tunneling, all of which undermine the scalability of traditional semiconductor technology [1]. To overcome these, researchers incepted the Quantum-dot Cellular Automata (QCA), a novel transistorless nanocomputing paradigm, which would face insurmountable hurdles. Unlike traditional transistors, which use voltage to control current flow, QCA employs quantum dots that can confine electrons, and their arrangement in quantum-dot cells allows for information processing without the need for current flow through a circuit, thus enabling ultra-low power consumption at a high operating speed due to its small size and absence of parasitic capacitances that limit conventional technologies [2]. This arrangement is affected by the electron arrangement in adjacent cells because of Coulombic electrostatic forces. Signals are spread throughout the system via this contact. Quantum dot cells can process information efficiently without the need for power-hungry transistors since the binary state of "0" or "1" is determined by the location of electrons in the cell [3–5].

1.1 Motivation

The use of sequential logic in QCA provides design flexibility and modularity. Designers can build complex circuits by combining basic QCA cells in sequential configurations to achieve desired functionalities. This modular approach facilitates the construction of larger and more complex digital systems with tailored performance characteristics. It can help implement error detection and correction schemes within QCA systems. As quantum dot-based computation is susceptible to various types of noise and disturbances [3], having robust sequential logic circuits can enhance the reliability and accuracy of QCA-based nanocomputations. For example, flip flops and counters are used in QCA circuitry for timing and synchronization purposes. Flip-flops, used in counters, ensure that the counting process is accurate and synchronized with clock signals, which is essential for reliable operation in digital systems.

1.2 Key contributions

The key contributions of this study are listed below:

- A novel single-layered toggle flip-flop (TFF) with highly polarized output is introduced in QCA circuitry.
- A single-layered two-bit down ripple counter is developed using the proposed TFF design.

Department of Electronics & Communication Engineering, University of Engineering & Management, Jaipur, Rajasthan, India
* angshumankhan2910@gmail.com

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- The counter improves performance and energy efficiency while maintaining scalability and stability.
- Physical verification of the design was performed through kink energy analysis.
- The proposed designs eliminate crossovers and ensure comprehensive input-output accessibility.

1.3 Organization

This article is arranged, including the following sections. Section 2 explains the basic terminologies associated with this nanotechnology. Section 3 reviews some relevant prior studies and infers the overall gaps that are overcome through the suggested designs. Section 4 explains the methodology used to implement the circuits. Section 5 introduces the proposed circuits, describing their design parameters. Section 6 analyzes the suggested designs in-depth, while Section 7 compares this study with relevant prior studies, and Section 8 wraps up the article.

2 Fundamentals of QCA

A square-shaped quantum-dot cell consists of four quantum dots, where two electrons can tunnel between the dots. The length of each side of a cell, *l* is 18 nm, i.e., 0.018 μm. The tunneling occurs via quantum mechanical processes, restricted to moving between adjacent dots, as shown in Fig. 1(a). This inherent quantum tunneling plays a significant role in determining both propagation and contamination delays. Due to Coulombic repulsion, these electrons settle in opposite corners of the cell, defining two stable polarization states, typically labeled as "+1" and "–1," which represent binary values of 1 and 0, respectively [4, 5]. Figure 1(b) explains the typical dimensions of both polarized and unpolarized QCA cells in the order of a few nanometers, allowing for high-density integration [6]. A QCA wire is designed to propagate the position of electrons, which represent binary data. The data is carried by the linear arrangement of quantum dots in a specific pattern shown in Fig. 1(c), which aligns the electrons in a way that mimics the behavior of electrical signals in logic circuits [2]. Next, a programmable logic gate, such as a QCA inverter, termed *QI*, is a device to invert a binary input value using the positional configuration of electrons in quantum dots. This represents a significant shift from traditional electronic logic gates and offers potential benefits in terms of power efficiency and density [3]. The typical arrangement is illustrated in Fig. 1(d). Another logic gate consisting of three inputs with a decision-making device cell, which is a fundamental logic block in QCA circuitry, is the majority voting logic gate, termed QM. The typical five-cell-based layout, including an output cell with its schematic, is shown in Fig. 1(e-f) [3, 6].

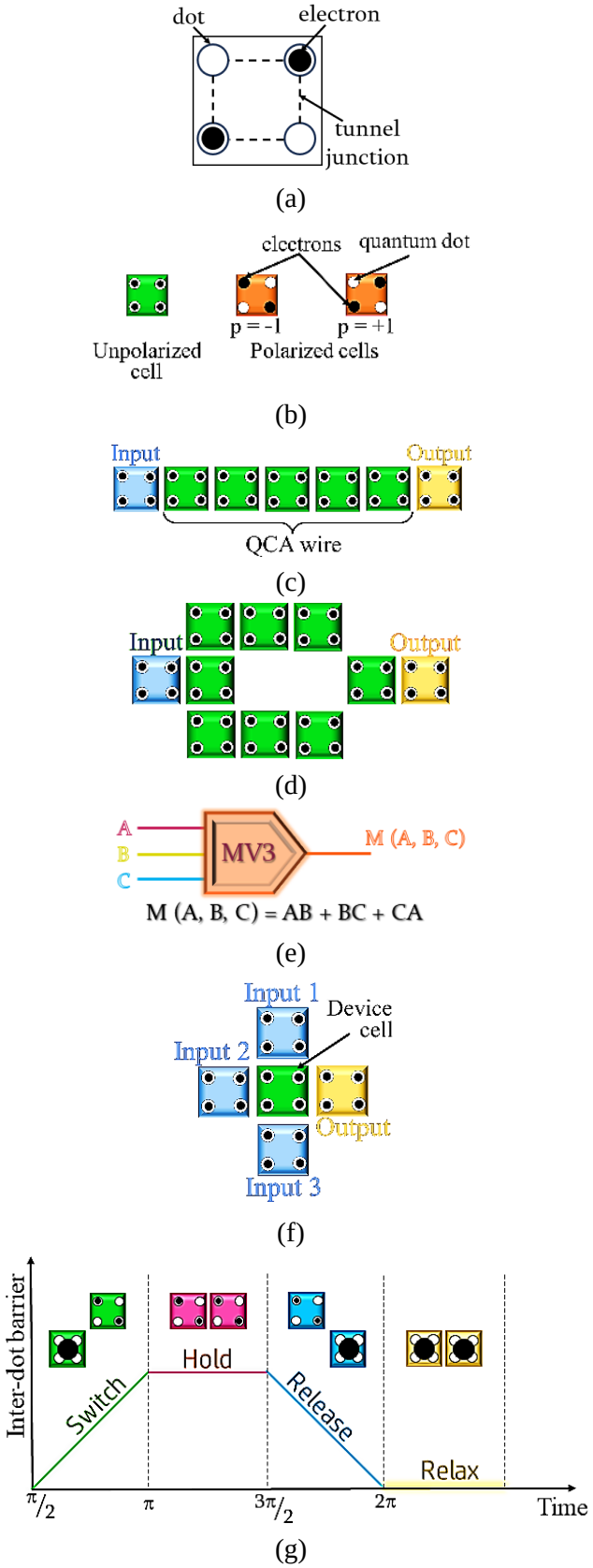


Fig. 1. QCA fundamentals, (a) QCA cell, (b) cell states, (c) wire, (d) QI, (e) QM schematic, (f) QM layout, and (g) transition of clock phases at clock zone 0

In QCA, the clocking concept is crucial for managing the timing and control of data flow within the circuit, which involves a series of clock phases that control the state of the QCA cells and their interactions. This clocking scheme divides the circuit into four distinct phases: switch, hold, release, and relax. The switching phase activates the QCA cells, allowing them to change states based on input signals, which is crucial for data propagation. Following this, the hold phase stabilizes the circuit by maintaining cell states temporarily, reducing the risk of errors during transitions. The release phase prepares cells to reset their states for the next cycle, while the relax phase allows them to return to a low-energy state, enhancing energy efficiency [4]. Each phase, being apart by ninety degrees from the next one, controls the electron movement by modulating potential barriers between the dots, as depicted in Fig. 1(g), ensuring synchronization of cell state transitions. Clocking in QCA also provides power gain, reduces energy dissipation, and enables pipelining, which is crucial for maintaining signal integrity across large-scale circuits. Properly coordinated, these clocking phases create a controlled environment for smooth data transmission and robust circuit operation, making them vital for high-speed applications. By optimizing these mechanisms, designers can significantly improve the performance and reliability of QCA circuits, mitigating issues such as noise and fabrication imperfections [6]. In QCA circuits, propagation delays can be influenced by the distance between cells and the rate of tunneling. If the tunneling rate is slow, it can lead to longer propagation delays as the state change in one cell needs time to affect adjacent cells. The variability in tunneling rates across different cells can cause inconsistencies in how quickly signals propagate through the circuit, especially in counters where sequential bits are closely interconnected. In sequential circuits, contamination delays can occur due to unintended interactions between cells. For instance, if a QCA cell transitions but the state change propagates through the circuit in an uncoordinated manner, it may lead to glitches or unstable outputs. Quantum tunneling can contribute to contamination delays by allowing for intermediate states that do not correspond to the final output.

Several strategies can be employed to mitigate these delays in QCA circuits. First, optimizing cell layout is essential, which includes minimizing the distance between cells to reduce propagation delays through careful design and placement of QCA cells in the circuit. Additionally, organizing cells within larger clock zones can help synchronize state changes and further reduce contamination delays. Another approach is tuning tunneling rates by selecting materials with favorable tunneling properties in silicon-based semiconductor QCA cells, which can enhance the overall speed of signal propagation. Furthermore, designing robust cells that favor stable configurations can help mitigate issues related to quantum tunneling, ensuring that transitions occur more predictably [2, 4].

3 Literature study

The design of TFF and counters remains a dynamic research domain with significant potential for advanced nanoscale sequential memory circuits, as it reveals a variety of approaches addressing layout design, optimization, and robustness addressed in this section. This study highlights key research contributions, challenges, and advancements in the field.

3.1 Review of relevant works

A 21-cell-based T-latch, as well as TFF, was introduced by M. Gholami *et al.* in [7], which features a 0.75 clock delay utilizing two *QM*s with two *QI*s within an area, *UA* of 0.02 μm^2. Based on this TFF, authors extended their work to fulfill their aim of designing a three-bit synchronous counter, which utilizes 137 cells with a latency of 2 clock cycles for each output. This work attempted energy calculations to show the energy efficiency of the circuits. A. Khan *et al.* in [8] proposed a single-layered toggle FF in QCA comprising 39 cells. The design utilized a *UA* of 0.05 μm^2, along with 4 *QM*s and 3 *QI*s, resulting in a latency (*QL*) as 1.25 clock cycles. While the study conducted a detailed energy analysis and provided cost estimations, the proposed circuit demonstrated relatively high latency and only moderate output polarization values. In [9], A. Khan introduced a modern TFF, termed QTFF, based on a novel approach that leverages 19 cells employing two *QM*s with a *QI* by cell translation within a single layer structure, allocating *UA* of 0.01 μm^2 area. While the design focuses on creating an energy-efficient circuit with less cell complexity, the author did not prioritize enhancing the average output polarization, which is essential for developing reliable sequential nanocircuits. S. Husain *et al.* introduced a TFF proposal in [10] featuring 77 cells, four QMs, and two QIs, with an area, *UA*, of 0.11 μm^2 and a delay of 2 clock cycles. Despite its innovative design, this approach is criticized for its large size, internal nodes, and lack of any energy calculations. Next, a TFF presented in [11] employs 22 cells and two *QM*s, with a delay of 1 clock cycle and occupying *UA* of 0.017 μm^2. A secondary design with 20 cells, two *QM*s, and one *QI* also has the same delay occupying *UA* of 0.018 μm^2. Both designs are notable for their simplicity with fewer cell complexities but lack energy dissipation or cost analyses. In [12], a multiplexer-based TFF was introduced using 19 cells occupying *UA* as 0.013 μm^2. This design has a delay of 0.75 clock cycles and utilizes a single *QI*. However, it lacks reliable *QM*s, a clock signal, and low output

polarization, which is essential for effective TFF functionality. Additionally, no energy calculations are provided for this design. In [13], a negative edge-triggered TFF was designed leveraging 21 cells without employing any primitive logic gates. This design exhibits clock delay but lacks energy estimation. Next, A. H. Majeed *et al.* proposed a novel but simpler TFF logic in [14]. Their design uses 21 cells employing a *QM* and an MMV gate in a single-layer structure with a coplanar crossover, utilizing an area of 0.018 μm^2, with a 1.25 clock delay. This study was further extended to develop a 2-bit counter with a novel clock signal design using 80 cells employing three *QM*s with two MMVs attributing a 2-clock delay. Energy dissipation was analyzed, but only for the TFF design. The primary drawback of this design is the significant input-to-output delay relative to its simplicity. In [15], another uncommon TFF design was proposed, featuring two inputs with one select line, utilizing 43 cells with a total area, *UA* of 0.05 $\mu m^{2,}$ and incorporating three *QM*s plus one *QI*. The design achieves an input-output delay of 1.25 clock cycles and includes energy calculations. Notably, this design includes multiple inputs and the absence of a T-input. In [16], another asynchronous down counter was introduced, utilizing 93 cells with four *QM*s and two *QI*s, covering a total utilized area, *UA* of 0.08 μm^2. The design incurs a significant delay of 2 clock cycles for each bit output. Its primary drawback is the high cell complexity, with numerous translated cells, which increases the overall design complexity despite its functionality.

3.2 Gaps in relevant works

The existing designs in the literature provide notable innovations but are often accompanied by significant limitations that hinder their practical application in nanocircuitry. One common issue in TFF designs is the trade-off between cell complexity and output polarization. While some circuits achieve reduced cell complexity, they suffer from lower output polarization, which compromises the reliability and scalability of the sequential circuits. In contrast, counter designs tend to exhibit higher cell complexity, which increases the design's overall complexity and area yet still produce low-polarized outputs, affecting the stability and performance of the circuits.

A crucial gap across many designs is the lack of thorough power analysis and cost estimations, which are essential for assessing the efficiency and feasibility of circuits in nanoelectronics. Many works either overlook or intentionally omit these factors, leaving unanswered important questions about the circuit's energy efficiency and overall performance. These gaps – cell complexity, output polarization, and the absence of energy and cost analysis – must be addressed to advance the field and create more reliable, scalable, and energy-efficient QCA-based circuits.

3.3 Problem statement

To address the trade-off between cell complexity and output polarization in QCA-based circuits while integrating comprehensive power, cost, and stability analysis to enhance their scalability, reliability, performance, and energy efficiency in nanocomputing.

3.4 Research objectives

The primary objectives of this study are as follows:

(i) To develop a TFF and ripple counter design that minimizes cell complexity while enhancing output polarization, thereby improving reliability and scalability in QCA circuits.

(ii) To provide a comprehensive analysis of power consumption and cost efficiency, addressing the gaps in existing designs to create more efficient and practical solutions.

(iii) To thoroughly assess the stability of the proposed counter design through physical verification using kink energy calculations.

3.5 Novelty of this work

This work covers significant novel features as:

- This study introduces an energy-efficient Toggle flip-flop (TFF) with highly polarized output.
- The novel design eliminates internal nodes and includes both normal and complementary outputs while utilizing minimal logic gates and lower latencies, addressing gaps overlooked by previous designs.
- The proposed TFF is utilized to develop a two-bit down ripple counter.
- The counter design aims to reduce latency and enhance sequential design in nanocircuits.
- The work provides a thorough power analysis using commonly employed tools like QCAPro and QCADesigner-E.
- It include cost estimations for the developed circuits, contributing to the creation of scalable and reliable designs.
- This work also includes average output polarizations for the developed circuits, contributing to the creation of stable and reliable designs under different temperature conditions.

- The study conducts kink energy analysis to physically verify the stability, including the counterion effects during design and simulation stage, of the proposed non-neutral QCA system.
- These efforts are directed towards applications in nanocomputing, reinforcing the reliability of the circuits developed.

4 Methodology

The process of designing, verifying, optimizing, and evaluating digital logic circuits in QCA starts by determining the specific function of the circuit, whether it is a basic logic gate, flip-flop, or a more complex system such as a counter or multiplexer. The layout is then created, followed by a careful arrangement of QCA cells to ensure proper signal flow, minimal interference, and correct logic operations. Clocking zones are applied to control signal propagation timing across the circuit. Initial simulations are run to validate the circuit's functionality. This iterative process continues until the circuit produces an accurate output, ensuring both the reliability and precision of the design, as shown in Fig. 2.

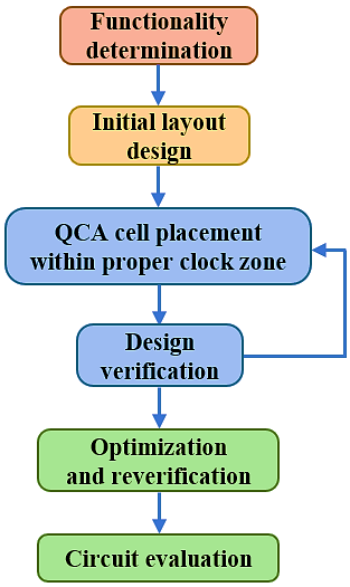


Fig. 2. Circuit design flow during QCA design phase

Additionally, the design undergoes optimization to minimize the number of QCA cells, reduce delay, and lower energy dissipation. Detailed performance analysis helps assess the circuits' efficiency and reliability. A comparison with existing works highlights improvements. Finally, overall performance is eva-luated, considering practical implementation, scalabi-lity, and integration into larger systems for nano-electronic computing.

5 Proposed works and simulation results

In sequential logic circuits, a flip-flop is a fundamental building block used for storing binary data. Unlike combinational logic circuits, which depend only on current inputs, sequential logic circuits rely on both current inputs and previous states. Flip-flops are essential for implementing memory, state machines, and timing circuits.

A toggle flip flop (TFF) is a type of digital storage element used in sequential circuits. This TFF has a straightforward operation and implementation, making it easy to use in various digital circuits. In practical digital systems, TFFs can be used to create toggle switches in user interfaces or control systems, which are essential in counting and frequency division applications. During high clock pulse, *C*, if the T-input of this flip flop is logic low, it holds the previous data and toggles its next data, *Q*, if the T-input becomes logic high. A novel approach, adapted from a study by A. H. Mazeed *et al.* [14], is employed to implement a T flip-flop (TFF) using the *QM* and Modified Majority Voter (MMV) gates, offering enhanced flexibility in QCA circuit design. As highlighted in [17], the MMV gate performs a three-input XOR operation. The Modified Majority Voter (MMV) gate in QCA is a multifunctional element capable of executing AND, OR, XOR, and XNOR operations. It is designed to minimize hardware requirements, conserve area, and lower clock latency. It operates efficiently at low temperatures (2 K) and can be configured for two binary inputs and a control input, functioning as a three-input exclusive-OR gate. Its stable output, ensured by electrostatic interactions, enhances its suitability for QCA-based digital logic design [17]. Building on these foundations, we develop a schematic, which is noted in Fig. 3(c), and the proposed TFF, referred to as P_T, is introduced in this study. Its functionality is verified against the logic table shown in Table 1.

Table 1. Logic table of P_T

Inputs		Outputs		Remarks
C	T	Q	$\bar{Q}$	
0	0	1	0	Hold (H)
0	1	1	0	No change (N)
1	0	1	0	Hold (H)
1	1	0	1	Toggle (T)

5.1 Toggle flip-flop design

The P_T consists of a 26-cell single-layer structure designed using QCADesigner [18] *ver.* 2.0.3 tool, with a clock delay of 0.50 to produce the next-state output *Q*, applying appropriate clocking mechanisms for each cell, as shown in Fig. 3 (d). Each cell covers an area of 324 nm^2, i.e., 0.000324 μm^2, spaced 2 nm, i.e., 0.002 μm apart, resulting in 28% area utilization within a total area, *UA* of 0.03 μm^2. A fixed polarized cell ($p = -1$, representing logic 0) is a common input to both *QM* and MMV gates. The memory loop incorporates two *QI*s with distinct clock phases. Notably, the design avoids the use of crossovers, also ensuring full accessibility of input and output nodes, making it scalable for higher-order circuit design.

P_T effectively balances cell complexity and latency by utilizing a single layer with a minimal logic gate without any crossovers. This streamlined approach minimizes the number of components required, thus reducing cell complexity, while the high polarization of the output ensures stable and rapid signal propagation, achieving a remarkable clock cycle latency of just 0.5. By avoiding crossovers, the design simplifies the circuit and enhances scalability, allowing for the easy integration of multiple T flip-flops into larger circuits without introducing significant delays or complexity. Overall, the P_T design illustrates how strategic architectural choices can optimize performance in QCA systems while ensuring efficient scalability for practical applications.

5.2 Two-bit down ripple counter design

P_T toggles its output on every clock pulse when the T-input is high. This behavior is ideal for counting because it alternates the output between logic 0 and 1, effectively counting binary states, where the primary requirement is to increment the count with each clock pulse. A ripple counter can be implemented using TFFs due to the specific toggling behavior of the P_T. Furthermore, the natural incrementing behavior of TFFs facilitates straightforward binary counting when connected in a ripple configuration, whereas D Flip-flops and J K Flip-flops may require additional logic for similar functionality. Its lower switching activity contributes to power efficiency, which is particularly important in QCA designs. In this counter, the output of one flip-flop is used as the clock input for the next TFF. This means each TFF toggles when the previous TFF changes from 1 to 0, causing a ripple effect. Here, each TFF represents one bit of the binary count.

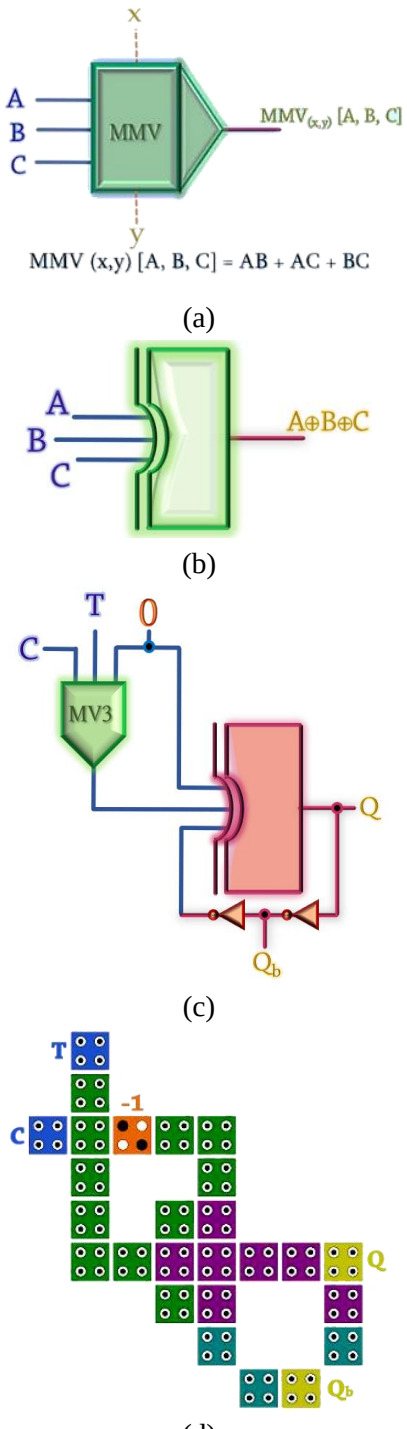


Fig. 3. Proposed P_T design, (a) typical MMV gate, (b) MMV based XOR3, (c) TFF schematic, and (d) TFF layout in QCA

For example, the first T flip-flop (the least significant bit, or LSB) toggles on every clock pulse. The second T flip-flop toggles when the first one completes a full cycle (i.e., toggles from 1 to 0), and so on. This results in a binary counting sequence. In the ripple counter, only

the first TFF feeds the clock pulse, and the next onward TFFs feed the output of the respective previous TFF, and a logic high input is applied on all TFFs to proceed with counting binary sequences. Based on these mechanisms, this study prepares a schematic design for a two-bit down ripple counter, called P_C, implemented in QCA circuitry. Its functionality is verified against the logic table shown in Table 2.

Table 2. Logic table of P_C

Input	Outputs		Q_1Q_0 output	
C	Q_0	Q_1	Binary	Decimal
0	1	1	11	3
0	0	1	10	2
1	1	0	01	1
1	0	0	00	0

In a single-layer structure, the P_C design is introduced using QCADesigner [18] *ver.* 2.0.3 tool, by instantiating two TFFs sequentially, utilizing 56 cells within a total area of 0.07 μm^2, achieving an area usage efficiency of 26%. The design incorporates four fixed polarized cells, with two cells polarized at $p = -1$, representing logic 0, which serve as the third input to the logic gates of each TFF. The other two cells, polarized at $p = +1$, provide a logic high input for the TFFs, completing the P_C architecture. This design also utilizes four QM gates and four QIs, as Fig. 4(b) depicts. Similar to the P_T design, the P_C architecture eliminates the need for crossovers, ensuring full scalability by keeping all input and output nodes external, allowing for higher-order design implementations. While implementing P_C, several trade-offs were made to achieve reduced latency. The design employs a single layer of cells to minimize propagation delays, but this increases complexity in cell placement to avoid signal interference. Using only two majority gates and two MMV gates helps speed up the circuit but limits its ability to perform more complex operations. The choice of achieving the counter in 1.5 clock cycles emphasizes speed, though it may increase susceptibility to errors during state transitions. Additionally, the design avoids crossovers to prevent signal interference, further reducing latency, but this complicates the layout. Overall, these trade-offs reflect a balance between reduced latency, reliability, functionality, and fabrication feasibility.

Reducing cell complexity often risks signal degradation, leading to lower output polarization due to weakened or less reliable interactions between cells. Furthermore, optimizing the circuit with fewer cells can make it harder to avoid signal interference and maintain stable majority and MMV gate operations. While fewer cells might reduce propagation delays by shortening the distance between elements, improper optimization can still disrupt polarization and timing. Moreover, the absence of crossovers in the single-layer design increases the risk of crosstalk or signal interference, which can degrade polarization if adjacent cells interact unintentionally, increasing the difficulty in sustaining the strong polarization needed for accurate outputs. In order to maintain high output polarisation and ensure reliable circuit performance, this design choice promotes smoother signal propagation by reducing the possibility of signals unintentionally influencing one another.

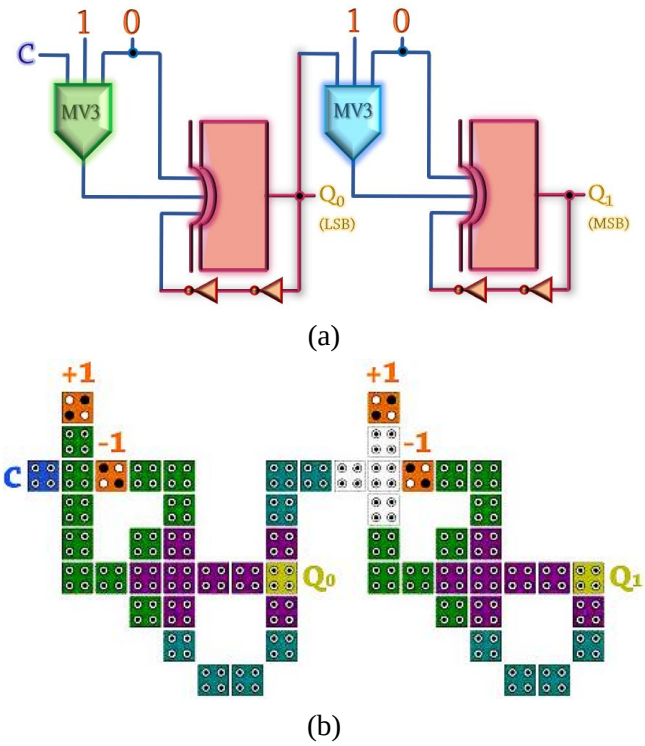


Fig. 4. Proposed P_C design, (a) schematic, and (b) QCA layout

Despite these challenges, the circuit overcomes them by leveraging an optimized arrangement of 56 cells and the strategic use of two *QM*s and two MMV gates, ensuring efficient signal transmission without cross-overs. The careful placement of these elements enhances stability, allowing the circuit to maintain high output polarization even with reduced cell complexity. Additionally, the use of well-defined clocking zones and proper synchronization across cells helps to preserve strong polarization, ensuring correct outputs even at lower latency. This balance between design efficiency and performance ensures reliable operation with minimal complexity.

5.3 Outline of n-bit counter

While asynchronous counters are simpler to design than synchronous ones, they may experience ripple delays, which can be minimized through optimized clocking and cell placement. To build an *n*-bit down

counter, multiple TFFs are cascaded, meaning the output of each TFF drives the clock input of the next one. As each TFF toggles upon receiving a clock pulse from the previous stage, the count decreases progressively. For instance, in a two-bit down ripple counter, the output of the first TFF, such as Q_0, is used as the clock input for the next TFF (Q_1). This same mechanism is applied in the *n*-bit system, where the output of each flip-flop serves as the input for the subsequent one. The schematic of the *n*-bit one is outlined in Fig. 5 below.

Increasing the number of bits necessitates more cells and logic gates, which could complicate the layout and make it difficult to maintain the same level of separation between signal paths, potentially reintroducing issues of interference. Moreover, managing the complexity of routing without crossovers can become more challenging as the number of connections grows, leading to a higher likelihood of longer interconnects that may introduce delays. Additionally, achieving the necessary synchronization across a larger number of gates while avoiding crossovers requires careful design consideration to ensure that all components operate in harmony, which may further complicate the circuit architecture. While eliminating crossovers improves signal integrity, scaling to higher-bit designs demands innovative strategies to address the increased complexity and potential propagation delays.

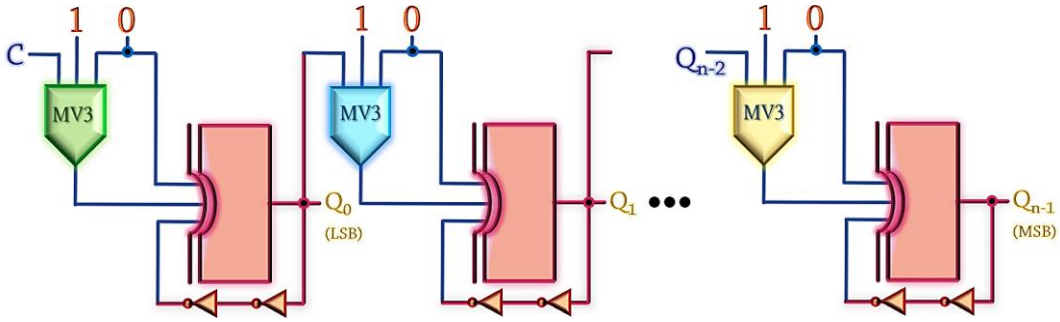
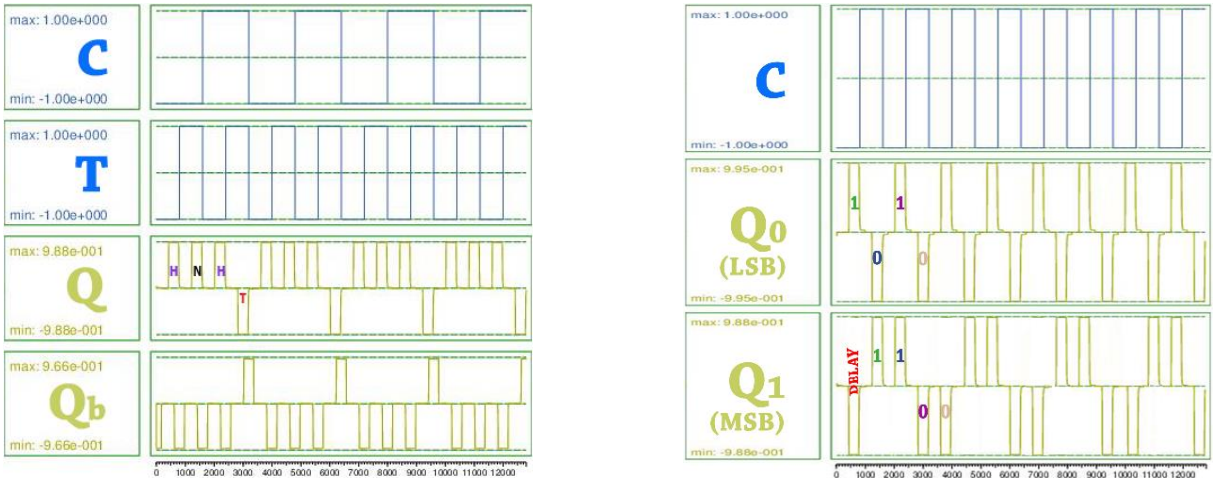


Fig. 5. Schematic for *n*-bit down ripple counter design in QCA

5.4 Design results

Simulations for both proposed designs were conducted using QCADesigner [18], *ver*. 2.0.3, with the coherence vector simulation engine set to the Euler method. The simulations were conducted under specific conditions, including a radius of effect of 65 nm and a temperature *T* of 1 K. Under these parameters, highly polarized outputs were obtained for each design, as illustrated in Fig. 6, by applying proper clocking to each cell.

A cell-level methodology was followed to achieve the simulation results. The outputs were subsequently verified against the truth tables, confirming the accuracy of the proposed designs based on the QCA layouts. These results clearly validate the correctness and functionality of the proposed architectures.



(a) (b)

Fig. 6. Simulation outputs, (a) that of P_T, and (b) that of P_C

6 Analyses

This study is further extended to analyze the proposed circuits by their design parameters and by conducting rigorous mathematical analyses to be more significant in nanocomputing applications.

6.1 Energy dissipation analysis

This analysis of QCA circuits is crucial for assessing energy efficiency and thermal behavior, particularly for low-power applications in nanoelectronics. To analyze the energy dissipation of the suggested single-layered designs, we employed the QCAPro [19] tool. This tool considers various physical parameters, including cell polarization and tunneling energy, to estimate power consumption. Temperature and tunneling energy are also the key input parameters that users can adjust in this tool to calculate different energy dissipation scenarios. Table 3 delves into a detailed power analysis at a temperature T of 2 K for both proposed designs.

Table 3. Energy values obtained using QCAPro

Ckt	E_{leak}			E_{switch}		
	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k
P_T	9.25	24.72	42.16	20.19	17.08	14.24
P_C	22.61	60.57	102.74	59.00	43.00	33.00

Ckt: Proposed circuits, E_{leak}: Average leakage energy dissipations in meV, E_{switch}: Average switching energy dissipations in meV

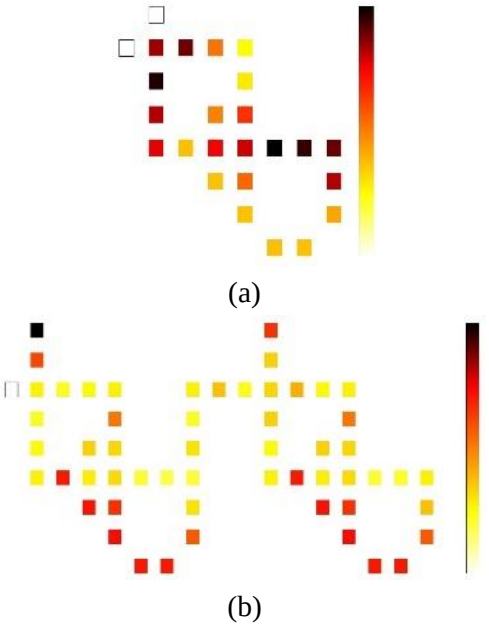


Fig. 7. Thermal hotspots at 0.5 E_k, (a) that for P_T, and (b) that for P_C

To calculate the energy in QCAPro, the circuit is first designed using QCADesigner *ver.* 1.4.0, exported, and then loaded into QCAPro. After evaluating a lot of internal iterations, the total energy dissipation (TE_1) at 0.5 E_k was found to be 29.44 meV and 81.61 meV for the P_T and P_C designs, respectively. The thermal hotspots found in the same physical conditions are showcased in Fig. 7.

Another well-known energy estimation tool is QCADesigner-E (QD-E), *aka* QCADesigner-Enhanced [20] *ver.* 2.2. It provides detailed energy consumption per individual QCA cell, allowing designers to pinpoint the most power-hungry components of a circuit. This can help in optimizing the layout and design to reduce energy consumption and enhance circuit performance. Simulating the proposed circuits in this tool using the Euler method of coherence vector simulation engine at a temperature, T of 1 K, the total power dissipation (TE_2) was recorded as 7.23 meV at an average value of 0.657 meV per cycle for P_T design. Similarly, the TE_2 for the P_C design was evaluated as 14.1 meV, at an average value of 1.28 meV per cycle, making the same conditions unaltered at any instance.

Table 4. Comparison of energy values obtained using QCADesigner-E

Works	TE_2	aTE_2
[7]	NA	NA
[8]	16.4	1.49
[9]	5.74	0.522
[10]	NA	NA
[11]	7.88	0.716
[11]	6.83	0.621
[12]	NA	NA
[13]	NA	NA
[14]	NA	NA
[15]	33.6	3.06
P_T	7.23	0.657

TE_2: total energy dissipation values in meV evaluated using QCADesigner-E, aTE_2: average energy dissipation per cycle in meV, NA: not applicable

Under different tunneling energy levels, QCAPro shows significant variation, especially for the P_C design, where the dissipation escalates drastically at higher energy levels. The P_T design has lower dissipation and exhibits more stability across the tunneling energy range. In QD-E, the dissipation values are much lower than those predicted by QCAPro. The average dissipation per cycle suggests that P_T consumes less energy than P_C, aligning with QCAPro's findings, but QD-E presents a more energy-efficient scenario overall.

In conclusion, both tools agree that P_T is more energy-efficient than P_C under all conditions, but the exact dissipation values vary significantly depending on the tool and method used for simulation.

6.2 Cost estimations

To thoroughly assess and optimize QCA circuit designs, a cost analysis [21] is crucial. This analysis generally focuses on three main components: area-delay cost (ADC), QCA-specific cost (QSC), and energy-delay cost (EDC). These aspects are quantitatively expressed through Eqns. (1-3).

$$ADC = UA \times (QL)^2 \tag{1}$$

$$EDC = (TE_1)^2 \times (QL)^2 \tag{2}$$

$$QSC = n[(QM)^2 + QI + (QC)^2] \times (QL)^2 \tag{3}$$

Considering *UA* as the total utilized in mm^2, QL as latency in clock cycles, TE_1 as total energy in eV evaluated in the QCAPro tool, *n* as the number of layers incorporated, and *QC* as the number of crossovers used in the design, the *ADC*, *EDC* and *QSC* values for P_T are 0.0075 unit, 0.0002 unit and 1.50 units respectively. Similarly, for P_C, these are 0.157 unit, 0.0149 unit, and 45 units, respectively.

6.3 AOP analysis

In a QCA circuit, the average output polarization, *AOP*, refers to the mean polarization of the output cells at the time of simulation [22]. This reflects how consistently the output cells maintain a certain binary state (either 0 or 1). It is calculated based on Eqn (4) below.

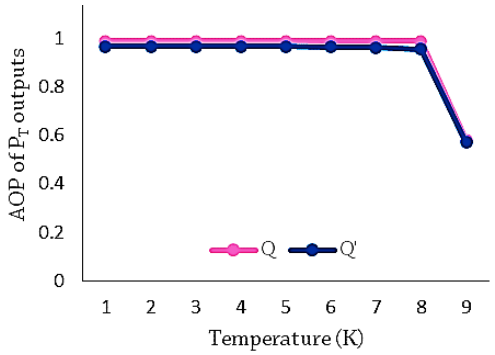
$$AOP = \left(\frac{P_{max} - P_{min}}{2}\right) \tag{4}$$

For example, the maximum output polarization (P_{max}) and the minimum output polarization (P_{min}) of the P_T design were recorded as 0.988 and –0.988, respectively, during the simulation for the output *Q*. So the AOP in this case should be 0.988. Table 4 shows all the outputs' *AOP* values at different temperature levels.

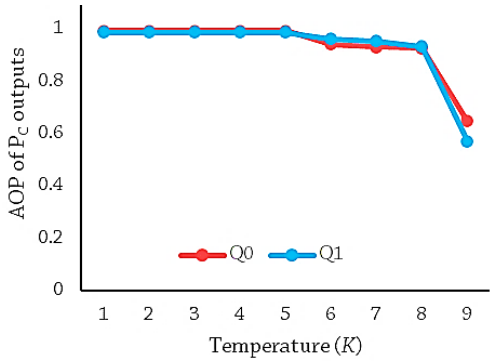
The simulation of the proposed circuits involves recording the corresponding AOPs by adjusting the temperature (in Kelvin) within the configuration of the specified simulation engine. This variant is obtained in Fig. 8.

Table 5. AOP values at different temperatures

Temp. (K)	AOP of P_T outputs		AOP of P_C outputs	
	Q	$\overline{Q}$	Q_0	Q_1
1	0.988	0.966	0.995	0.988
2	0.988	0.966	0.995	0.988
3	0.988	0.966	0.995	0.988
4	0.988	0.966	0.995	0.988
5	0.988	0.965	0.995	0.988
6	0.988	0.964	0.942	0.964
7	0.988	0.961	0.933	0.955
8	0.988	0.955	0.928	0.934
9	0.581	0.570	0.649	0.571



(a)



(b)

Fig. 8. AOP variation with temperatures, (a) that for P_T, and (b) that for P_C

The temperature-dependent change of the average output polarization significantly influences the efficacy and reliability of the introduced circuits. Through analysis, designers are able to forecast the QCA circuits' thermal limitations and put plans in place to ensure steady functioning at different temperatures.

6.4 Physical verification

During the design phase of a QCA nanocircuit, physical verification ensures that the circuit performs as expected under real-world physical conditions, considering factors like quantum coherence and thermal noise. It refers to a method used to assess the stability and correctness of the circuit by analyzing its kink energy [4]. Kink energy indicates the extra energy required when neighboring QCA cells are not aligned as expected in their lowest energy configuration. Each cell typically holds two mobile electrons. Due to Coulombic repulsion, these two electrons will always tend to occupy opposite corners of the square to stabilize as well as minimize their energy. Kink energy in QCA designs affects stability and reliability by representing the electrostatic repulsion between polarized neighboring cells.

Coulombic interaction is vital in positioning electrons within QCA cells, allowing for stable configurations that minimize potential energy. This interaction enhances energy efficiency by enabling precise electron arrangements, thus reducing power consumption during logic state switching, which is crucial for larger digital circuits. Additionally, it impacts signal propagation by maintaining strong polarization, ensuring reliable and fast signal transmission between cells. However, as circuit sizes increase, managing these interactions becomes more complex, potentially leading to crosstalk and signal degradation. Therefore, while beneficial, optimal design considerations are necessary to maintain the advantages of Coulombic interaction in larger QCA circuits. Coulomb's law regulates the basic interaction between charges. Given two charges q_1 and q_2, spaced apart by a distance r, the electrostatic potential energy U should be calculated as follows:

$$U = \frac{kq_1q_2}{r} \tag{5}$$

The kink energy depends on whether the cells have the same or opposite polarizations [4, 23], as expressed in Eqn (6).

$$E_k = E_k^{opp} - E_k^{same} \tag{6}$$

When cells exhibit opposite polarizations, such as one representing '1' and the other '0,' the resulting interaction energy, denoted as E_k^{opp}, tends to be higher due to increased charge repulsion. In contrast, adjacent cells with the same polarization generally experience lower interaction energy, represented as E_k^{same}. The same formula is employed to compute the kink energy in both cases, but the specific configurations considered correspond to either opposite or identical polarization states [23].

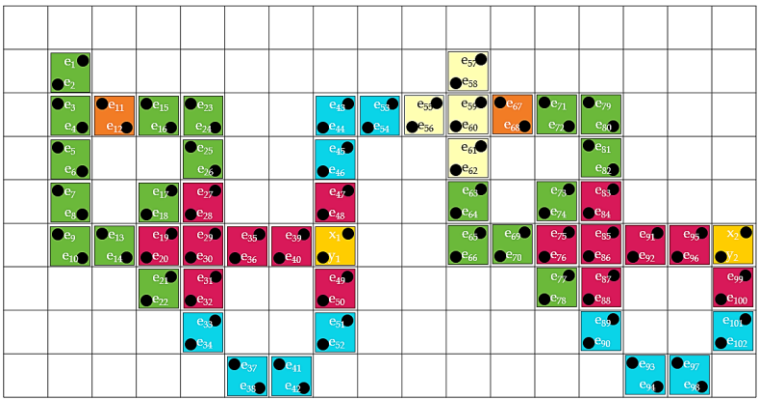


Fig. 9. Layout of P_C at same polarization states of output cells with respect to that of neighbouring cells considering input bit as 0

In this configuration, the interaction energy (E_k^{opp}) tends to be higher due to the increased repulsive forces between charges when neighboring cells have opposite polarizations (e.g., one cell represents '1' and the other '0'). Conversely, when adjacent cells share the same polarization, the interaction energy (E_k^{same}) is typically lower. The same approach is applied to calculate the kink energy in this scenario, although configurations with opposite polarization dominate [23]. During physical verification, minimizing kink energy is essential to reduce errors, improve circuit stability, and enhance performance. High kink energy can increase error rates and slow data propagation, so designers optimize cell placement and layout to ensure low-energy configurations. This ensures stable operation during both simulation and actual fabrication of QCA circuits.

Figure 9 illustrates the electron placement within each quantum dot cell, all aligned in the same polarization based on the layout of the P_C design for an input bit of C as 0. The black dots in each cell indicate

the exact positions of the electrons for this specific input bit. Each quantum dot is positioned within a square-shaped cell, where the side length of the square is 0.018 μm, and the quantum dots are separated by a distance of 0.002 μm from one another. This configuration is assumed to be the same for the given design scenario. With respect to the same polarization of the output cell Q_0 as that of the adjacent cell with the 39th and 40th electrons, Table V reviews all of the U values for the influence of all electrons on the output cell electron x_1. According to Coulomb's law, the distance between the electrons in adjacent cells increases, and the electrostatic repulsion between them decreases, resulting in lower energy. Therefore, electrons that are farther apart exert less influence on each other. For the purpose of kink energy evaluation in QCA circuits, only the interactions between the electrons in the first 90 cells neighboring the x_1 electron, which experience the stronger repulsion and thus have a greater impact on the system's overall energy, are considered.

Table 6. Electrostatic energy values based on distances between x_1 and neighboring cell electrons at the same polarization state

Electron	Dist*	$U^{\#}$	Electron	Dist*	$U^{\#}$
e_1	144.2	0.16	e_{46}	28.4	0.81
e_2	151.3	0.15	e_{47}	20.0	1.16
e_3	150.5	0.15	e_{48}	18.1	1.28
e_4	127.1	0.18	e_{49}	20.0	1.16
e_5	143.7	0.16	e_{50}	42.0	0.55
e_6	122.0	0.19	e_{51}	40.0	0.58
e_7	139.4	0.17	e_{52}	60.7	0.38
e_8	120.0	0.19	e_{53}	63.2	0.37
e_9	138.0	0.17	e_{54}	42.0	0.55
e_{10}	121.3	0.16	e_{55}	72.1	0.32
e_{11}	166.9	0.15	e_{56}	47.4	0.49
e_{12}	108.5	0.15	e_{57}	100.0	0.23
e_{13}	118.0	0.18	e_{58}	74.9	0.31
e_{14}	101.6	0.16	e_{59}	84.9	0.27
e_{15}	114.9	0.19	e_{60}	59.4	0.39
e_{16}	90.3	0.17	e_{61}	72.1	0.32
e_{17}	82.5	0.19	e_{62}	47.4	0.49
e_{18}	98.0	0.17	e_{63}	63.2	0.37
e_{19}	80.0	0.16	e_{64}	42.0	0.55
e_{20}	99.6	0.15	e_{65}	60.0	0.39
e_{21}	82.5	0.15	e_{66}	45.7	0.51
e_{22}	105.1	0.18	e_{67}	86.3	0.27
e_{23}	98.4	0.16	e_{68}	90.3	0.26
e_{24}	73.2	0.19	e_{69}	80.0	0.29
e_{25}	87.6	0.17	e_{70}	64.6	0.36
e_{26}	63.9	0.19	e_{71}	101.6	0.23
e_{27}	63.2	0.17	e_{72}	108.5	0.21
e_{28}	78.0	0.16	e_{73}	101.9	0.23
e_{29}	60.0	0.15	e_{74}	82.0	0.28
e_{30}	80.1	0.15	e_{75}	100.0	0.23
e_{31}	63.2	0.18	e_{76}	83.9	0.28
e_{32}	86.8	0.16	e_{77}	101.9	0.23
e_{33}	72.1	0.19	e_{78}	90.4	0.26
e_{34}	97.2	0.17	e_{79}	118.3	0.20
e_{35}	40.0	0.19	e_{80}	127.1	0.18
e_{36}	60.7	0.17	e_{81}	109.6	0.21
e_{37}	83.4	0.16	e_{82}	122.0	0.19
e_{38}	87.6	0.15	e_{83}	121.6	0.19
e_{39}	20.0	0.15	e_{84}	102.0	0.23
e_{40}	42.0	0.18	e_{85}	120.0	0.19
e_{41}	71.0	0.16	e_{86}	103.6	0.22
e_{42}	80.5	0.19	e_{87}	121.6	0.19
e_{43}	60.0	0.17	e_{88}	108.8	0.21
e_{44}	45.7	0.19	e_{89}	126.5	0.18
e_{45}	40.0	0.17	e_{90}	117.3	0.20

*Distances are determined in nm
#Coulombic energies (U) are expressed in joules$\times 10^{-20}$

Equation (5) may be simplified as follows: The parameter k actually is $k = 1/4\pi\varepsilon_0\varepsilon_r$, where free space permittivity ε_0 values 8.85×10^{-12} F/m, and in vacuum, the relative permittivity, ε_r, is 1, evaluates $k = 9\times10^9$ and q_1=q_2 being electronic charges each of value as 1.602×10^{-19} C. As a result, $U = 23.1 \times 10^{-29}/r$. For instance, when calculating the Coulombic energy U between the electron x_1 in the output cell and the electron e_{40} in the 20th cell, we first determine the distance r_{40} between them. Using the Pythagorean theorem, the distance, $r_{40} = \sqrt{38^2+18^2} = 42$ nm. This distance corresponds to $U_{40} = 0.18\times10^{-20}$ J. Similarly, for kink energy evaluations, the electrons that have a stronger repulsion and more impact on the output cell electrons x_2 and y_2 are considered. Specifically, the 57th to 102nd electrons, which are closer together and therefore exert more influence on each other, are the primary contributors to kink energy, as analyzed in Table VI for x_2 electron.

Table 7. Coulombic interaction energy values based on distances between x_2 and neighboring cell electrons at the same polarization state

Electron	Dist*	$U^{\#}$	Electron	Dist*	$U^{\#}$
e_{57}	144.2	0.16	e_{80}	73.2	0.32
e_{58}	151.3	0.15	e_{81}	87.6	0.26
e_{59}	134.2	0.17	e_{82}	63.9	0.36
e_{60}	144.2	0.16	e_{83}	63.2	0.37
e_{61}	126.5	0.18	e_{84}	78.0	0.30
e_{62}	139.7	0.17	e_{85}	60.0	0.39
e_{63}	121.6	0.19	e_{86}	80.0	0.29
e_{64}	138.0	0.17	e_{87}	63.2	0.37
e_{65}	120.0	0.19	e_{88}	86.8	0.27

e_{66}	139.2	0.17	e_{89}	72.1	0.32
e_{67}	132.4	0.17	e_{90}	97.2	0.24
e_{68}	108.5	0.21	e_{91}	40.0	0.58
e_{69}	100.0	0.23	e_{92}	60.7	0.38
e_{70}	119.4	0.19	e_{93}	83.4	0.28
e_{71}	114.9	0.20	e_{94}	87.6	0.26
e_{72}	90.3	0.26	e_{95}	20.0	1.16
e_{73}	82.5	0.28	e_{96}	42.0	0.55
e_{74}	98.0	0.24	e_{97}	71.0	0.33
e_{75}	80.0	0.29	e_{98}	80.5	0.29
e_{76}	99.6	0.23	e_{99}	20.0	1.16
e_{77}	82.5	0.28	e_{100}	42.0	0.55
e_{78}	105.1	0.22	e_{101}	40.0	0.58
e_{79}	98.4	0.23	e_{102}	60.7	0.38

Based on this analysis, the E_k^{same} for electron x_1, y_1, x_2 and y_2 are evaluated as 30.41×0^{-20} J, 30.97×10^{-20} J, 14.69×10^{-20} J and 19.31×10^{-20} J, which demonstrates total E_k^{same} at the same polarization as 95.39×10^{-20} J.

Similarly, for opposite polarizations of output cells with respect to their neighboring cell configurations, the E_k^{opp} values for the four electrons are also evaluated as 51.84×10^{-20} J, 39.25×10^{-20} J, 29.3×10^{-20} J, and 25.96×10^{-20} J for electrons, respectively. These demonstrate the total E_k^{opp} is calculated as 146.35×10^{-20}J. Finally, the kink energy, E_k, as per Eqn (6), is 51×10^{-20} J.

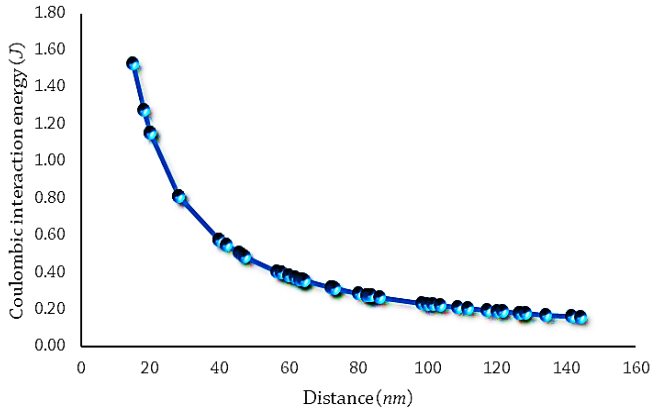


Fig. 10. Coulombic interaction energy variation with measured distances

It is worth noting that the kink energy is lower when cells have the same polarization compared to when they have opposite polarization, as the electrostatic repulsion is minimized in the aligned state. This lower kink energy contributes to the circuit's stability, as fewer disruptions or errors are likely to occur. Conversely, higher kink energy in the opposite polarization state leads to increased instability and a higher risk of errors.

Electrostatic interactions get more complex in the case of non-neutral systems, which have defects or charge imbalances. The existence of counterions [24] in a non-neutral QCA system changes the electric field and overall charge distribution, therefore the definition of kink energy must be changed to account for the impact of this non-neutrality on cell interactions. In order to preserve charge neutrality inside a molecule or system, counterions are ions that accompany oppositely charged ions. In molecular Field-Coupled Nanocomputing (FCN) designs, they are essential, especially for oxidised and zwitterionic molecules. Counterions reduce electrostatic disturbances that might have a major effect on charge distribution and device performance by balancing charges [24].

As a result, the kink energy, E_k defines straightforward models as the energy landscape is complicated by other elements including charge redistribution and long-range interactions. As a result, using the formula (7) below, we can write the kink energy for non-neutral systems as $E_k^{non\text{-}neutral}$, and include the contribution of counterions and net charge distribution in the total kink energy.

$$E_k^{non\text{-}neutral} = E_k + \Delta E \tag{7}$$

Depending on how the counterions affect cell connections, this contribution is denoted by the term ΔE and can be either positive or negative. As a result, when the majority of cells retain the same polarisation, the circuit's stability is increased. This stability can be confirmed by examining the kink energy, which shows that the circuit functions as planned.

6.5 Scalability and reliability

Both the P_T and P_C designs demonstrate excellent scalability and reliability, making them well-suited for advanced QDCA applications. Their single-layer structures, without the need for crossovers, ensure straightforward access to input and output nodes, which simplifies the design and enhances scalability for larger, more complex circuits. With optimized area usage, these designs efficiently utilize space, supporting their application in higher-order systems. This streamlined layout reduces the physical space required and minimizes the complexity of interconnections, enabling the design to maintain performance as the bit width increases.

Additionally, the highly polarized outputs achieved during simulation, even at low temperatures (1 K), reflect the designs' reliability and stable performance. By eliminating crossovers, they avoid signal interference and crosstalk, reducing errors and improving overall circuit robustness. Finally, the designs were

validated through simulations, confirming their accurate operation and reliable functionality.

The implementation of QCA binary ripple counters relies on an effective clocking scheme to ensure synchronous operation of flip-flops and prevent glitches, with a multi-phase clocking strategy aiding in transition management. Attention to propagation delays caused by quantum tunneling, is crucial and can be addressed through strategic cell placement and buffering. These ripple counters have practical applications in digital clocks for timekeeping, frequency division in communication systems, data processing units, and memory circuits for efficient counting and addressing. The advantages of QCA technology, including increased speed and lower propagation delays compared to traditional CMOS, contribute significantly to modern processing and computing.

Table 8. Design and analyzed parameters of prior and proposed TFFs

Works	Year	CC	UA	QL	#QM	#QI	AOP	TE_1	TE_2	Cost functions		
										ADC	EDC[1]	QSC
[7]	2023	21	0.02	0.75	2	2	0.986	16.2	NA	0.0095	0.0001	3.37
[8]	2023	39	0.05	1.25	4	2	0.952	35.1	16.4	0.0781	0.0019	28.1
[9]	2023	19	0.01	1.25	2	1	0.953	25.1	5.74	0.0031	0.0009	7.81
[10]	2023	77	0.11	2.00	4	2	0.902	NA	NA	0.44	NA	72.0
[11]	2022	22	0.02	1.00	2	0	0.953	31.1	7.88	0.017	0.001	4.00
[11]	2022	20	0.02	1.00	2	1	0.953	25.2	6.83	0.018	0.0006	5.00
[12]	2021	19	0.01	0.75	1	1	0.863	NA	NA	0.0073	NA	1.12
[13]	2020	22	0.03	1.00	2	2	0.930	NA	NA	0.03	NA	6.00
[14]	2019	21	0.02	1.25	2	0	0.933	29.2	NA	0.0281	0.0013	6.25
[15]	2018	43	0.05	1.25	3	1	0.933	49.3	33.6	0.0781	0.0037	15.6
P_T	NA	26	0.03	0.50	2	2	0.988	29.4	7.23	0.0075	0.0002	1.50

CC: cell count, UA: total utilized area in mm^2, QL: latency in clock cycles, #: count, TE_1: total energy in meV calculated in QCAPro at 0.5 E_k, TE_2: total energy in meV evaluated using QD-E tool, NA: not applicable

[1] EDC were calculated based on TE_1 measured in eV

Table 9. Design and analyzed parameters of prior and proposed counters

Works	Year	CC	UA	QL	#QM	#QI	#QC	AOP_1	AOP_2	TE_1	TE_2	Cost functions		
												ADC	EDC[1]	QSC
[16]	2024	93	0.08	2.00	4	2	NA	0.950	0.950	NA	30.1	0.32	NA	72.0
[7]	2023	137	0.16	2.00	8	3	NA	0.994	0.994	196	NA	0.64	0.1536	268
[14]	2019	80	0.09	2.00	5	0	1	0.988	0.953	NA	NA	0.18	NA	100
P_C	NA	56	0.07	1.50	4	4	NA	0.995	0.988	81.6	14.1	0.157	0.0149	45.0

#QC: number of wire crossovers, AOP_1: AOP were calculated for output Q_0, AOP_2: AOP were calculated for output Q_1

[1] EDC were calculated based on TE_1 measured in eV

As devices continue to shrink in size, maintaining scalability while enhancing energy efficiency becomes critical for the continued advancement of computing technologies. The successful implementation of such designs can lead to more compact and powerful circuits that consume less energy, paving the way for high-performance applications in areas like nanocomputing, advanced microprocessors, and low-power electronic devices. Moreover, the miniaturization potential of QCA supports the development of compact electronic components, which are essential for advancements in wearable devices and the Internet of Things (IoT). Ultimately, the unique properties of QCA facilitate the exploration of new computational architectures, paving the way for breakthroughs in processing capabilities and problem-solving efficiency.

7 Comparisons

This section highlights the significant improvements observed in the proposed designs compared to relevant prior works, particularly when analyzing all key parameters. Table 8 has been organized to display both the design parameters and the associated mathematical metrics, including costs, for a comprehensive comparison of P_T. These allow for a clear and detailed evaluation of performance, showing how the proposed design outperforms earlier approaches across multiple factors.

Though the P_T design requires five more cells compared to the most relevant design [7], it offers a notable performance improvement. The suggested design reduces latency by 0.25 clock cycles, making it 21% more efficient in terms of area-delay cost. Additionally, it shows a significant enhancement of 55.5% in terms of QSC.

Similarly, Table 9 offers a comprehensive comparison of the P_C design. These tables collectively allow for a clear and systematic evaluation, showcasing how the proposed designs outperform previous approaches in terms of efficiency, performance, and other critical metrics. The results underscore the enhanced capabilities of the new designs, further emphasizing their superiority over prior implement-tations across multiple dimensions.

Compared to the latest 2-bit down counter referenced in [16], P_C demonstrates significant improvements in *AOP* and associated costs, leveraging 37 lesser cells and reducing clock delay by 0.5 cycles. The proposed circuit is 51% more efficient in terms of area-delay cost and 38% more efficient in *QSC*, with a 5% improvement in *AOP*. Furthermore, it is 53% more energy-efficient, as evaluated using QD-E [20]. These improvements highlight the design's ability to balance increased complexity with better overall efficiency and performance, reinforcing its advancements, including high energy efficiency compared to previous implementations.

8 Conclusion

This article presents P_T and P_C designs with significant advancements in the realm of QCA nanocomputing, offering substantial improvements in scalability, efficiency, and performance. Both designs leverage single-layer structures and avoid crossovers, simplifying circuit implementation and enhancing scalability for more complex systems. The P_T design reduces latency by 0.25 clock cycles, resulting in a 55.5% enhancement over QCA-specific cost. On the other hand, the P_C design demonstrates a notable 53% improvement in energy efficiency compared to the latest 2-bit down counter. These enhancements, validated through simulations using QCADesigner, QCAPro, and QCADesigner-E tools, showcase the designs' ability to optimize performance while managing complexity. Besides these, By ensuring that the majority of the cells remain in low-energy, same-polarization states, the circuit's overall stability is confirmed. This method of evaluating kink energy, including counterion effects under different polarization conditions, provides a key mechanism for physical verification of this non-neutral QCA system, ensuring the P_C circuit behaves as intended under real-world conditions and external influences. These advancements collectively highlight the proposed designs' effectiveness in pushing the boundaries of QCA-based circuit designs. These scaled designs can be further evaluated for fabrication feasibility to implement higher-bit counters, registers, memory cells and more complex sequential logic circuits, enabling real-world integration in nanoscale devices.

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