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COMPARISON OF A STANDARD AND A SCHOTTKY DUAL GATE MOSFET

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The article presents modelling and simulation of the electrical properties of Schottky dual gate (DG) MOSFET structures. The contribution focuses on the influence of the design parameters upon the properties of the DG MOSFET. The design parameters strongly affect the slope of the transfer characteristics and the magnitude of leakage currents because in nanometer structures they have a substantial influence on band-to-band tunnelling in the vicinity of the drain. The active region of the transistor structure must be viewed upon as a quantum well whose parameters affect the effective bandgap width, which in turn has a key influence in the model of band-to-band tunnelling.

K e y w o r d s: Schottky dual gate, MOSFET

1 INTRODUCTION AND THEORY

The most serious issue in shrinking the dimension of MOS transistors is the Short Channel Effect (SCE). It brings about complications in the production of CMOS structures. Small changes in the length of the channel result in considerable variations in the threshold voltage. In the current CMOS technology, this phenomenon is suppressed by high doping of the regions around the source and drain junctions. The high carrier concentration in these regions causes a decrease in the mobility of free charge carriers. It is this very effect of SCE that motivates further investigations of novel MOS structures that might lead to possible integration of transistors with channel lengths in the nanometer range [1]. One of the promising devices of the new CMOS technology is the dual gate thin film transistor, in the literature referred to as DG-MOS (Dual-Gate MOS). It has a lot of variations.

We have designed, in ISE MDRAW, a 2-dimensional standard DG MOSFET structure (Fig. 1a) and a Schottky DG MOSFET (Fig. 1b) with a 1 nm thick SiO_2 gate and metal gate length $L_{MG} = 30$ nm. The concentration profile of the semiconductor with a heavily doped region n^+-Si (5×10^{19}cm^{-3}) is shown in Fig. 2. The transitions between the n^+ region and the undoped region were simulated by an exponential profile with a decrease of donor concentration from the maximum value by three orders of magnitude at a length of 8.4 nm.

The ISE DESSIS calculator was used to simulate the electric properties of the designed standard and Schottky DG MOSFETs. Within the calculator, the fundamental equations were based on the drift-diffusion model of charge transport with Fermi-Dirac statistics, the Lombardi and Masetti models for low field mobility, and the Caughey-Thomas/Canali model for velocity saturation with default DESSIS parameters for silicon. Since the

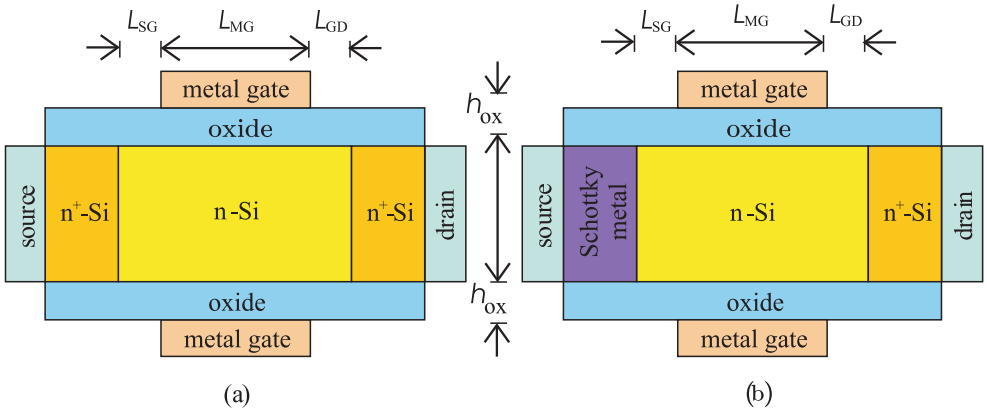

Fig. 1. Two-dimensional standard DG MOSFET structure (a), and Schottky DG MOSFET structure (b) with a 1 nm thick SiO_2 gate and metal gate length $L_{MG} = 30$ nm.

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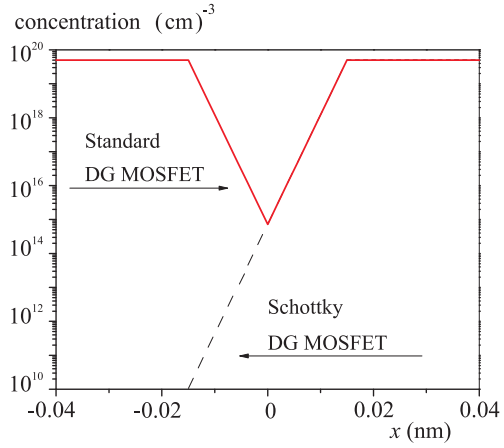

Fig. 2. Concentration profile of the standard and Schottky DG MOSFETs with $L_{\rm MG} = 30$ nm and $L_{\rm SG} = L_{\rm GD} = 0$ with a heavily doped region n^+–Si $(5 \times 10^{19}{\rm cm}^{-3})$.

leakage drain current $I_{\rm D}$ (in the switched-off state with negative $V_{\rm GS}$) in the designed submicrometer structures stems from band-to-band tunnelling in the drain region (see the band diagrams in Figs. 3a,b), utmost attention was paid to physical modelling of this phenomenon.

To simulate the effect of band-to-band tunnelling, simple and commonly used models from DESSIS are available. A general expression for the band-to-band models can be written for the generation term occurring in the continuity equations as [2, 3]

$$R^{b2b} = AE^{\alpha} \exp\Big(-\frac{B}{E}\Big), \qquad (1)$$

where E is the local electric field. The value of exponent α is 1. Coefficient A for band-to-band tunnelling was set to $1.1 \times 10^{27}{\rm cm}^{-2}{\rm V}^{-1}{\rm s}^{-1}$. Coefficient B was calculated, assuming a parabolic potential barrier with transverse energy component $E_{\perp}$, from expression

$$B = \frac{\pi\sqrt{m^* E_g}\big(E_g + 4E_{\perp}\big)}{2\sqrt{2}q\hbar}\,, \qquad (2)$$

where $E_g \approx 1.124$ eV for silicon at room temperature and the value of the fitting parameter $E_{\perp}$ was set to 0.0085 eV. In such a case the value of parameter B is 2.13×10^9 V/m, which is the default value in DESSIS. However, the active semiconductor region of the transistor structure presents, along with the side insulating layers, a quantum well in the band diagram [4], see Fig. 4.

By solving the Schrödinger equation for this structure we found the closest allowed energy level for electrons at a distance of δE_C above the lower edge of the conduction band E_C of the semiconductor and the closest allowed energy level for holes at a distance of δE_V below the upper edge of the valence band E_V. Due to this, the effective bandwidth of the semiconductor is broadened to

$$E_g^* = E_g + \delta E_C + \delta E_V\,. \qquad (3)$$

Parameters of the quantum structure, such as the width of the semiconductor, Y and the band offsets ΔE_C and ΔE_V between the insulator and semiconductor affect the effective bandgap E_g^*, which in turn has an impact upon the value of coefficient B.

In case the well width is large, $Y > 15$ nm, the values of $\delta E_C \approx 0$ and $\delta E_V \approx 0$ can be neglected. In our simulation we considered smaller well widths, $Y = 6$, 8 and 10 nm. The values of δE_C and δE_V were calculated using the applet Numerov Quantum Well Calculator designed at the University of Buffalo [5].

In addition to the aforementioned input parameters we considered a band offset $\delta E_C = 3.2$ eV of the SiO_2/Si junction. The bandgap of the oxide was $E_g^{\rm SiO_2} = 8.9$ eV and the effective electron and hole masses $m_e^* = 0.26\,m_0$ and $m_h^* = 0.16\,m_0$. The values of δE_C and δE_V are given in Tab. 1 along with the values of E_g^* and B calculated subsequently from Eqns. (3) and (2).

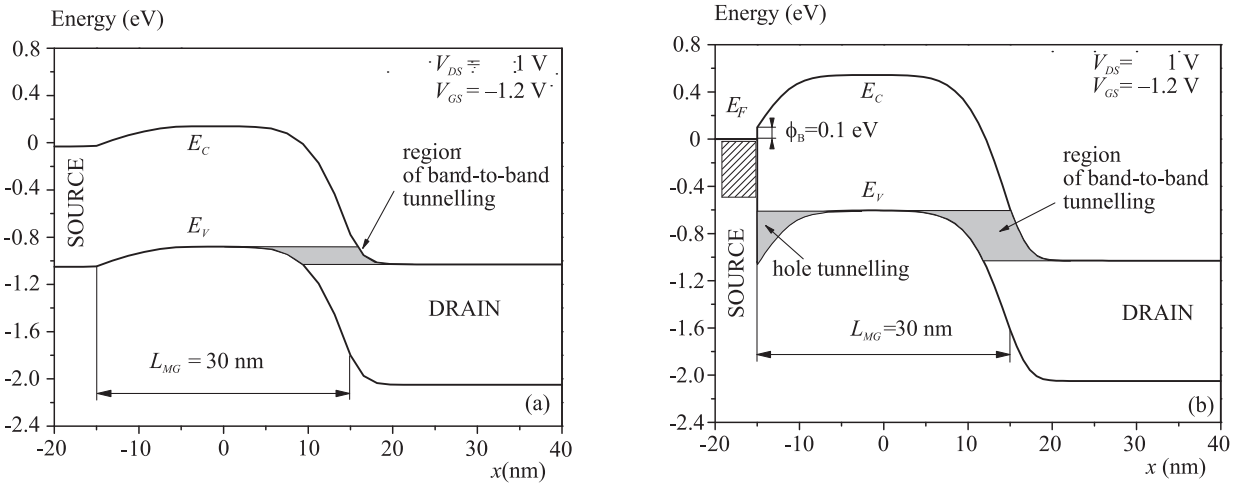

Fig. 3. Band diagrams: (a) standard DG MOSFET, (b) a Schottky DG MOSFET with Schottky barrier height $\Phi_{\rm B} = 0.1$ eV, metal work function $\Phi_{\rm M} = 4.17$ eV, dimensions $h_{0x} = 1$ nm, $Y = 10$ nm, $L_{\rm MG} = 30$ nm, $L_{\rm SG} = L_{\rm GD} = 0$, and voltages $V_{\rm DS} = 1$ V, $V_{\rm GS} = -1.8$ V.

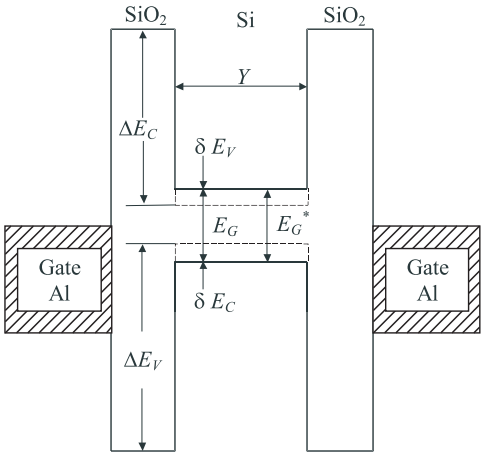

Fig. 4. Cross section of the DG MOSFET structure — the quantum well.

Table 1. Positions of energy levels above E_C and below E_V, effective bandgap E_g^*, and parameter B occurring in Eqns. (1) and (2) in dependence on the well width Y.

well width Y (nm)	δE_C (eV)	δE_V (eV)	E_g^* (eV)	B (V/m)
6	0.0465	0.0562	1.67	2.448×10^9
8	0.0272	0.0327	1.1839	2.324×10^9
10	0.0178	0.0214	1.1632	2.264×10^9

2 SIMULATION RESULTS

The Schottky DG MOSFET was simulated with a barrier height Φ_B varying from -0.2 eV to 0.2 eV while considering tunnelling through the Schottky contact with $L_{MG} = 30$ nm, $\Phi_{MG} = 4.17$ eV (aluminium), $L_{SG} = L_{GD} = 0$ and with a heavily doped region n^+-Si(2.5×10^{19}cm^{-3}). The resulting transfer characteristics are shown in Figs. 5a and 5b for $V_{DS} = 1$ V (reverse biased Schottky junction) and for $V_{DS} = -1$ V (forward biased Schottky junction), respectively. In these simulations we did not consider the effect of gate tunnelling of free charge carriers through the oxide layer. The highest slope and lowest leakage current are obtained for structures with Schottky barrier heights $\Phi_B = 0$ and 0.1 eV with a reverse biased Schottky junction ($V_{DS} = 1$ V). To the contrary, with a forward biased Schottky junction ($V_{DS} = -1$ V) neither the slope nor the threshold voltage change with the Schottky barrier height but the leakage currents are higher by approximately one order of magnitude than in the reverse biased Schottky junction ($V_{DS} = 1$ V), whereas in the on-state the currents are roughly intact. Low Schottky barrier metal-semiconductor contacts that were considered in our simulations might be prepared on silicon with those metals whose work function is nearly equal to the electron affinity of the semiconductor, and $\Phi_B \approx \Phi_M - \chi_{Si}$, where $\chi_{Si} = 4.05$ eV. Examples of metals with such work functions: $\Phi_{Hf} = 3.53$ eV, $\Phi_{Nb} = 4.01$ eV, $\Phi_V = 4.11$ eV and $\Phi_{Ta} = 4.12$ eV. This expression holds only if the interface traps density is low. Other possibilities how to reach low Schottky barriers on Si are examined in [6].

Further we examined how the leakage current I_D can be decreased by suppressing the effect of band-to-band tunnelling without substantial lowering of the drain current in the on-state by increasing the distance L_{GD}. Simulated results for the Schottky DGMOSFET and standard DGMOSFET are shown in Fig. 6. With a growing distance L_{GD} between the gate and the drain, the leakage current I_D becomes lower but this goes hand in hand with a decrease of the transistor current in the on-state ($V_{GS} = 2$ V). A distance of L_{GD} above 5 nm lowers the drain current in the on-state by about 15 % compared to the case with $L_{GD} = 0$.

Simulations of the effect of the well width Y upon the transfer characteristics are shown in Fig. 7. The insets represent details of the I-V curves in the on-state, the

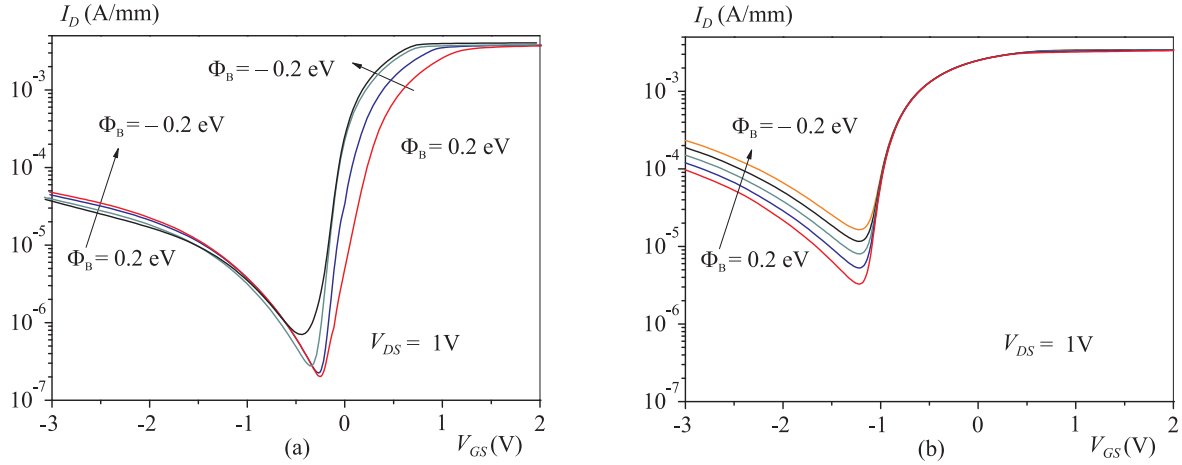

Fig. 5. Transfer characteristics of the Schottky DG MOSFET with a variable Schottky barrier height $\Phi_B = -0.2$, -0.1, 0, 0.1 and 0.2 eV, $L_{MG} = 30$ nm, heavily doped region n^+-Si(2.5×10^{19}cm^{-3}), $\Phi_{MG} = 4.17$ eV, $h_{0x} = 1$ nm, $Y = 10$ nm and $L_{SG} = L_{GD} = 0$: (a) $V_{DS} = 1$ V, (b) $V_{DS} = -1$ V.

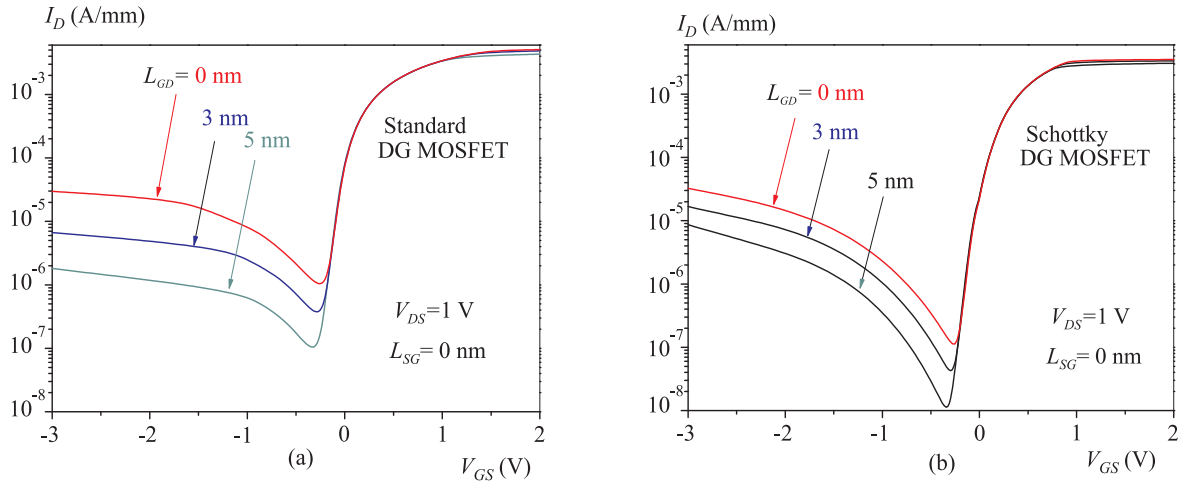

Fig. 6. Transfer characteristics at $V_{\mathrm{DS}} = 1$ V: (a) standard DGMOSFET with a heavily doped region (n^+-Si, $5{\times}10^{19}\,\mathrm{cm}^{-3}$), (b) Schottky DGMOSFET with $\Phi_{\mathrm{B}} = 0.1$ eV, with a heavily doped region n^+-Si, ($2.5 \times 10^{19}\mathrm{cm}^{-3}$). Without considering the effect of band-to-band tunnelling the cut-off currents drop below 10^{-17} A/mm (outside the scale of the figure). This confirms that band-to-band tunnelling and tunnelling through the gate oxide limit the cut-off current.

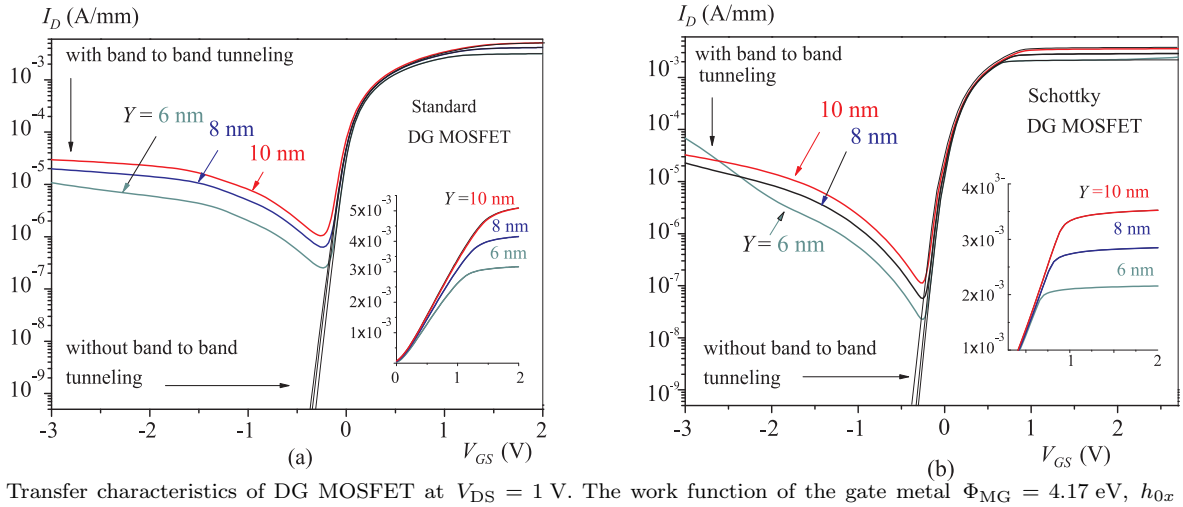

Fig. 7. Transfer characteristics of DG MOSFET at $V_{\mathrm{DS}} = 1$ V. The work function of the gate metal $\Phi_{\mathrm{MG}} = 4.17$ eV, $h_{0x} = 1$ nm, $L_{\mathrm{MG}} = 30$ nm, $L_{\mathrm{SG}} = L_{\mathrm{GD}} = 0$ and variable parameter Y: (a) standard DGMOSFET with a heavily doped region n^+-Si ($5{\times}10^{19}\mathrm{cm}^{-3}$), (b) the Schottky DGMOSFET with barrier height $\Phi_{\mathrm{B}} = 0.1$ eV and a heavily doped region n^+-Si ($2.5 \times 10^{19}\mathrm{cm}^{-3}$.

scale of current being linear. Narrowing of the well suppresses the effect of band-to-band tunnelling upon the leakage current due to a higher parameter B (the effective silicon band gap is wider) but this again goes along with a decrease of the drain current in the on-state because the thickness of the conductive channel becomes smaller. In other words, what one achieves in decreasing the leakage current, is lost due to the decrease of the drain current in the on-state.

Finally we compare the transfer characteristics of Schottky and standard DG MOSFET structures. Comparisons were made for the following parameters common to both types of structure: $L_{\mathrm{MG}} = 30$ nm, $\Phi_{\mathrm{MG}} = 4.17$ eV, $L_{\mathrm{SG}} = L_{\mathrm{GD}} = 0$ nm, $Y = 10$ nm and with a heavily doped region n^+-Si, $5 \times 10^{19}\mathrm{cm}^{-3}$. In the Schottky DGMOSFET we considered barrier heights $\Phi_{\mathrm{B}} = 0.1$ and 0 eV. Results are shown in Fig. 8. The transfer characteristics of the Schottky DG MOSFET with barrier height $\Phi_{\mathrm{B}} = 0$ has the same slope as that of the standard DG MOSFET (approx. 100 mV/decade in the steepest part of the curve). For the Schottky DG MOSFET, the lower minimum on the transfer characteristics lies by half an order of magnitude lower than in the standard DG MOSFET. However, the effect of band-to-band tunnelling at higher reverse gate voltages V_{GS} is more pronounced than in the standard DG MOSFET (at $V_{\mathrm{GS}} = -3$ V the difference in leakage currents is higher than one half of the order). The rise of the leakage current with increasing negative gate voltage V_{GS} is steeper in the Schottky DG MOSFET structures than in the standard ones, see Fig. 8. This is due to tunnelling of holes through the Schottky potential barrier for holes as shown in Fig. 3b. Thus, band-to-band tunnelling is enhanced also by hole tunnelling in the source region. This hole component of charge transport is not present in standard DG MOSFET structures shown in Fig. 3a. The currents at $V_{\mathrm{GS}} = 2$ V in the Schottky DG MOSFET are higher than in the standard DG MOSFET by a factor of 1.5, which, we believe, is caused by the higher electron mobility in Schottky

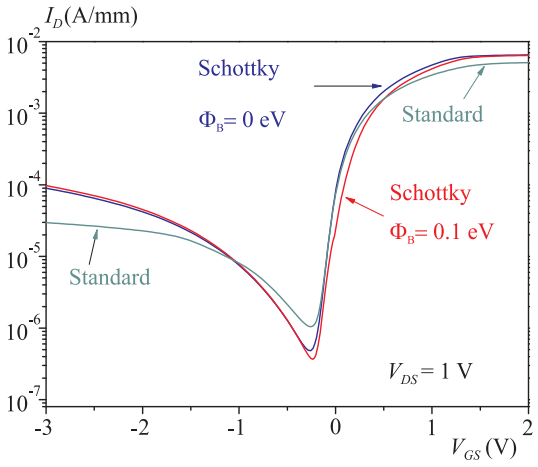

Fig. 8. Comparison of transfer characteristics of Schottky DG MOSFETs with barrier heights $\Phi_B = 0.1$ and 0 eV with a standard DG MOSFET at $V_{DS} = 1$ V. Gate metal work function $\Phi_{MG} = 4.17$ eV, $h_{0x} = 1$ nm, $L_{MG} = 30$ nm, $L_{SG} = L_{GD} = 0$, $Y = 30$ nm with a heavily doped region n^+-Si (5×10^{19}cm^{-3}). The Schottky barrier height $\Phi_B = 0.1$ and 0 eV.

DG MOSFET structures are due to a lower level of doping in the source region (see Fig. 2) and the higher source series resistance R_S in the standard DG MOSFET (in the Schottky MOSFET $R_S = 0$). This lowers the effective (or intrinsic) V_{GS} above the threshold voltage thereby reducing the drain current.

3 CONCLUSION

As far as lowering of the leakage currents and increasing the currents in the on-state are concerned, simulations confirmed that the structures of DG MOSFETs had both technological and design limits. The technological limit is determined by setting such parameters as the doping level of the n^+-Si region and the Schottky barrier height on the source, the design limits are given by dimensions L_{MG}, L_{GD} and Y. In addition to these parameters one can vary also the work function of the metallic gate Φ_{MG}, which, however, has no effect upon the slope or on the currents, it only shifts the threshold voltage. Similarly, parameter L_{SG}, if it is different from zero, lowers the drain current in the on-state but it has almost no impact on the leakage current. All of the aforementioned parameters affect the field intensity in the vicinity of the drain and hereby also band-to-band tunnelling. This is why a correct physical model of band-to-band tunnelling plays a key role in simulating the properties of DG MOSFET structures. It will be necessary to verify if the model we have chosen describes reality precisely enough. In our future work we will concentrate on a more accurate evaluation of the band-to-band currents J_{TUN}^{b2b} and of the generation terms R^{b2b} derived thereof that are customarily not provided by DESSIS.

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