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MAXIMUM TEMPERATURE DETECTION SYSTEM FOR INTEGRATED CIRCUITS

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The paper describes structure and measurement results of the system detecting present maximum temperature on the surface of an integrated circuit. The system consists of the set of proportional to absolute temperature sensors, temperature processing path and a digital part designed in VHDL. Analogue parts of the circuit where designed with full-custom technique. The system is a part of temperature-controlled oscillator circuit — a power management system based on dynamic frequency scaling method. The oscillator cooperates with microprocessor dedicated for thermal experiments. The whole system is implemented in UMC CMOS 0.18 μm (1.8 V) technology.

K e y w o r d s: TCO, DFS, VLSI, CMOS

1 INTRODUCTION

Because of scaling down the technology node of modern digital integrated circuits (IC) the power density inside the package is increasing significantly in late years [1]. As an effect the operating temperature of the chip is rising and endangers the circuit to overheating [2]. For that reason engineers must take into account thermal effects inside integrated circuit.

There are many works trying to solve problem of huge power dissipation in ICs. Most of them focus on temporal limitation of system throughput while closing to overheating or quite the contrary: boosting the performance in safe temperature range. Such solutions are described as DPM (Dynamic Power Management) systems [3, 4]. The goal is to find the optimal balance state between keeping the throughput of the system on the possible maximum level and decreasing power consumption of the device to keep thermal constraints. Assuming that circuit cannot exceed acceptable maximum temperature for proper work it should be controlled in that way to keep its temperature as close to the permissible limit as possible with minimal fluctuations. To achieve that some dynamic control systems have been developed including: dynamic voltage scaling (DVS) [5], dynamic clock throttling (DCT) [6] and dynamic frequency scaling (DFS) [7]. Despite former achievements on the field some further investigations must be done to improve thermal behaviour of the circuit.

Crucial operation in power management is measuring chip temperature and finding the hottest part of integrated circuit. The paper describes design and structure of the set of temperature sensors spread over the IC layout and a circuit for detection of maximum value produced by these sensors. Presented system is a part of temperature-controlled oscillator (TCO) which is circuit based on DFS method for continuous and instantaneous control of chip performance referring to present maximum temperature of the chip. Designed TCO cooperates with OctaLynx microprocessor which is a prototype circuit designed by a team together with authors of this paper for thermal test purposes. The whole system of TCO with the processor is designed in UMC CMOS 0.18 μm (1.8 V) technology. The analogue part of the system (sensors, analogue multiplexer and temperature comparator) was designed with full-custom technique. The digital part responsible for maximum temperature recognition was designed with top-down technique and synthesized from VHDL code.

2 IDEA OF TEMPERATURE–CONTROLLED OSCILLATOR

Set of temperature sensors with circuit for maximum temperature detection, which are main subject of this paper, are part of Temperature-Controlled Oscillator (TCO) — a thermally-aware power management system for high performance processors [8, 9]. This section will concisely describe proposed TCO structure.

The concept of temperature-controlled oscillator origins from the fact that CMOS digital circuit working with higher frequency consumes more power according to (1) where P_{diss} is power dissipated in integrated circuit, K is proportionality factor, f_0 is operating frequency, V_{DD} is supply voltage and C_L is load capacitance.

$$P_{diss} = K f_0 V_{DD}^2 C_L \,. \tag{1}$$

The equation above means that if the silicon die reaches high temperature range it is necessary to decrease the clock rate and as a consequence cool the chip down. The problem is how to manage the frequency of the clock to minimize temperature fluctuations and let the circuit work possibly fast. The other problem is how to measure temperature distribution over chip area and how to find maximum temperature inside it.

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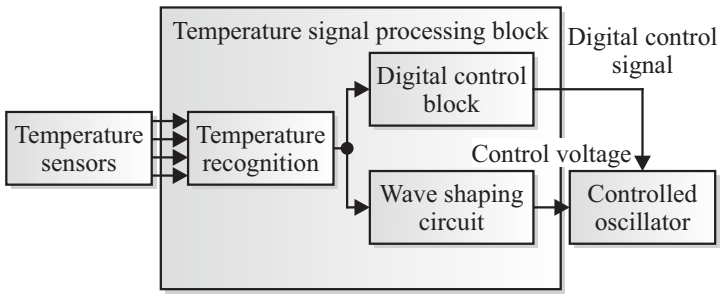

Fig. 1. Block diagram of the temperature-controlled oscillator

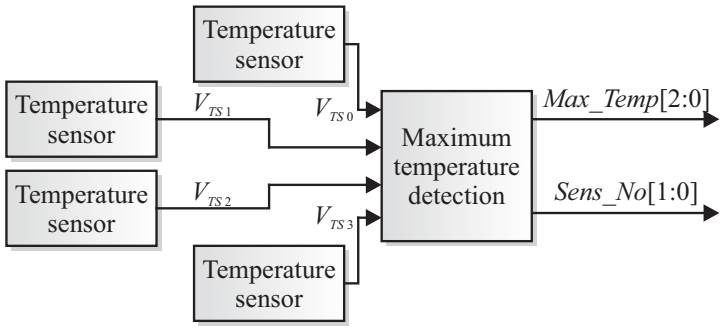

Fig. 2. Block diagram of set of temperature sensors with temperature comparator

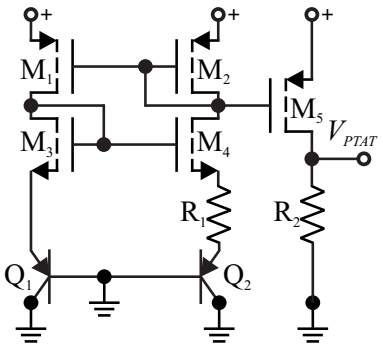

Fig. 3. Schematic diagram of the PTAT sensor

Structure of designed TCO is depicted in Fig. 1. Source of information about current temperature of the integrated circuit is a set of temperature sensors spread over the area of the chip. The temperature-proportional signal has to be processed for further usage. Firstly, the present temperature range indicated by each sensor must be recognized by flash ADC [10] alike circuit and maximum temperature in the circuit must be found. The signal referring to maximum temperature is passed to next part of the control block. The aim of division of further processing path into to sub-blocks (digital control block and analogue wave shaping circuit) is precise and efficient control of generator designed as ring oscillator.

As can be seen, set of temperature sensors and method of maximum temperature detection inside integrated circuit are key elements for the TCO work and optimum control of system behaviour. Since they are very important part of the TCO they have to be designed thoroughly and special attention has to be put on these circuits. Their structure and measurement results will be presented in next section.

3 PROBLEM OF MAXIMUM TEMPERATURE DETECTION AND ITS SOLUTION

Overheating and hot spots are usual problems in modern microelectronics. As a consequence researchers work on many methods to solve them. Some of this works focus on transferring the heat outside the chip package [11] while others consider hardware and software methods of managing the power dissipated inside the package. In second case monitoring of the chip temperature is necessary [12] and usually is performed by means of temperature sensors array located uniformly on the chip die surface. For example AMD Opteron had 38 built-in temperature sensor [13]. Some works lead to optimization of sensors allocation on the IC surface [14] while others to reduction of number of sensor which are necessary for efficient operation [15]. This work is author's solution for the problem of maximum temperature detection. Main requirements for designed circuit were as small as possible energy consumption and layout area coverage because designed power management system has limited area near the microprocessor in the silicon die and should not add too much to total power dissipated in the package. As a result authors were looking for unsophisticated but efficient methods which resulted with many simplifications in circuit structure.

Block diagram of the part of TCO which is main subject of this paper is depicted in Fig. 2. The system consist

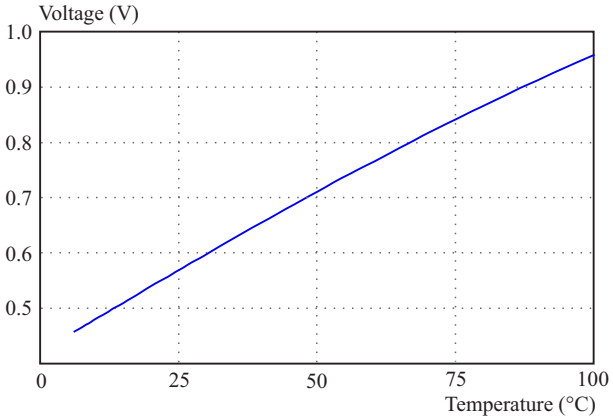

Fig. 4. Voltage vs. temperature characteristic of PTAT sensor

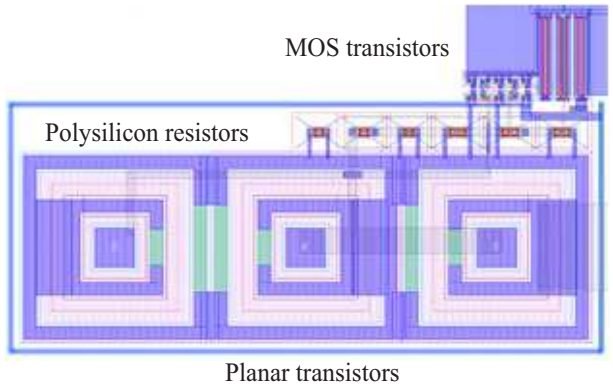

Fig. 5. Topography of the PTAT sensor

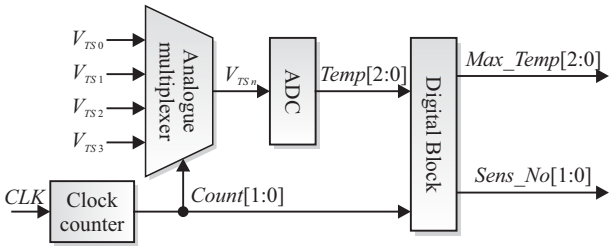

Fig. 6. Block diagram of the temperature comparator

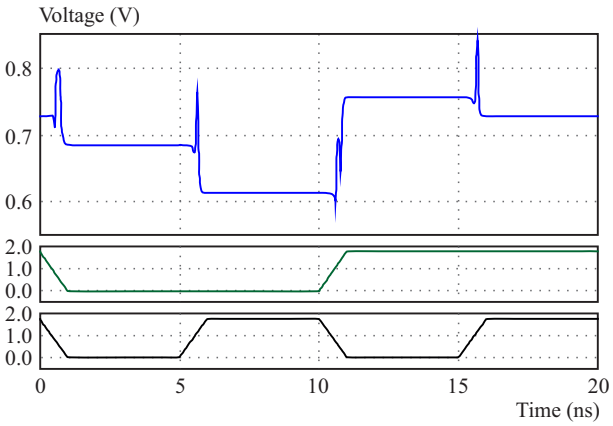

Fig. 7. Result of analogue multiplexer operation

of four temperature sensors spread over the area of integrated circuit. Each sensor produces voltage V_{TSi} (where i is sensor number) which is proportional to present temperature of silicon die at the place where the sensor is located. These voltages are the input to temperature comparator block which produces digital information about present maximum temperature value and number of sensor which has detected maximum temperature. Firstly, sensor structure and its analysis will be given, then the comparator will be considered in next part of the paper.

The temperature sensors are realized as PTAT (Proportional To Absolute Temperature) sensors [16, 17]. The PTAT sensor task is to give the voltage proportional to the temperature of the chip. Its work is based on the phenomenon that difference between voltages of two diodes or bipolar transistors, which have different areas and conduct the same current, is proportional to the absolute temperature. Implemented structure, presented in Fig. 3, has been chosen from many other possible sensor applications because the accuracy is sufficient for described case and presented circuit is easy to implement in CMOS process with usage of planar transistors. Presented PTAT sensor consists of 5 MOS transistors, 2 bipolar transistors and 2 resistors.

The sensor produces voltage given by

$$V_{TS} = \frac{W_5}{W_2}\frac{kT}{q}\ln(n)\frac{R_2}{R_1} \tag{2}$$

where W_2 and W_5 are widths of the gates of the M2 and M5 transistors, k is the Boltzmann's constant, T is temperature, q is the charge and n is the ratio between emitter areas of Q1 and Q2 planar transistors. Great advantage of such structure is that it produces linear voltage response to the temperature which is very convenient for further processing of signal proportional to temperature. Current conducted by the circuit is limited to prevent self-heating of the sensor. In presented case the temperature sensor was designed using two PNP planar transistors with the emitters area multiplication factor $n = 2$. The material of the resistors has significant influence to the parameters of this sensor. In this work resistors were built of highly resistive polysilicon layer. Thermal characteristic of designed temperature sensor is presented in Fig. 4. The V_{PTAT} signal is increasing with slope of about 5.54 mV/°C and ranges from 458.2 to 956.6 mV at expected temperature range of 10 to 100 °C. Very good linearity of the temperature sensor response is clearly visible. Layout of designed PTAT sensor is depicted in Fig. 5 (main elements are marked on the picture).

The process performed by the temperature comparator block is divided into three separate steps. At first, signal from four sensors are multiplexed and only one signal is sampled. Such operation limits processing of measured temperature to single path and, as a consequence, leads to area coverage and power consumption reduction. In second step the temperature range of sampled signal is recognized and in third its value is compared with previous samples and maximum temperature is found. Such structure of temperature comparator is presented in Fig. 6.

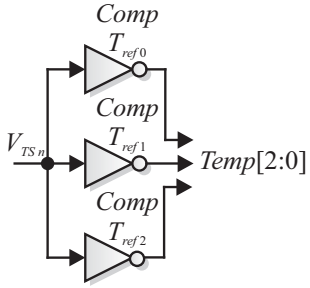

Fig. 8. Block diagram of the temperature comparator

Table 1. Transfer function of the temperature comparator

Temperature (°C)		V_{TS} (mV)		Output vector		
min	max	min	max	$Temp_2$	$Temp_1$	$Temp_0$
–	70	(0)	808	0	0	0
70	80	808	860	0	0	1
80	90	860	910	0	1	1
90	–	910	(1800)	1	1	1

Table 2. Main parameters of TCO

TCO element	Area (μm^2)	Mean current consumption (mA) (at ambient temperature)
PTAT sensor	45×77	0.2–0.5 (at 10–100 °C)
Analogue part	73×100	1.7
Digital part	117×120	~ 1 (highly dependent on temperature dynamics)

Analogue multiplexer is a circuit consisting of structure of transmission gates controlled by the modulo 4 clock counter. In such a way at the moment only one voltage signal from four sensors is transferred to the block responsible for temperature range recognition. Effect of this block operation when four different signals (623, 685, 730 and 755 mV) are provided to multiplexer input is depicted in Fig. 7 (two bottom graphs are control signals from clock counter; the top graph is multiplexer output). The signal is sampled and processed by next blocks when steady, the operation will be described more precisely in next part of paper.

When the signal proportional to temperature is multiplexed then it can be recognized. It is done by the flash ADC-alike circuit. In fact, it has been decided that in described application exact temperature value does not have to be known. For the TCO work it is sufficient to know only in which of four temperature ranges the circuit currently is. In human language it can be compared to low, medium and high temperature of the chip. As an effect the converter can be minimized to three comparators producing 3-bit output vector in linear n-of-3 code [18]. Standard structure of flash ADC consists also of the decoder translating the vector to natural binary code. In presented circuit it is not necessary because next digital block can be designed to work with n-of-3 code as well and such solution has been implemented because of power consumption and area saving reasons. What is more, standard flash structures contains resistive voltage divider to produce a reference voltage for each comparator, but if the reference voltages referring to temperature values are specified and constant the comparators and resistors can be replaced by much simpler CMOS inverter gates designed for proper threshold voltages indicated by temperature sensor characteristic. The solution covers much smaller area with much lower power consumption. The problem of sample synchronization and input signal noise (lack of hysteresis) are solved in next digital block. Block diagram of described temperature comparator is presented in Fig. 8. Table 1 describes behaviour of the temperature comparator in different temperature ranges. The reference temperatures are result of previous thermal experiments with integrated circuits. Temperature below 70 °C is quite low and safe for the chip while some circuits (especially generators) indicated behavioural problems at temperature above 90 °C. Third reference is in middle of two previous ones.

Final stage of digital processing of the temperature signal is the FIFO (First-In, Fast-Out) buffer consisting of four words, each storing information about other sensor.

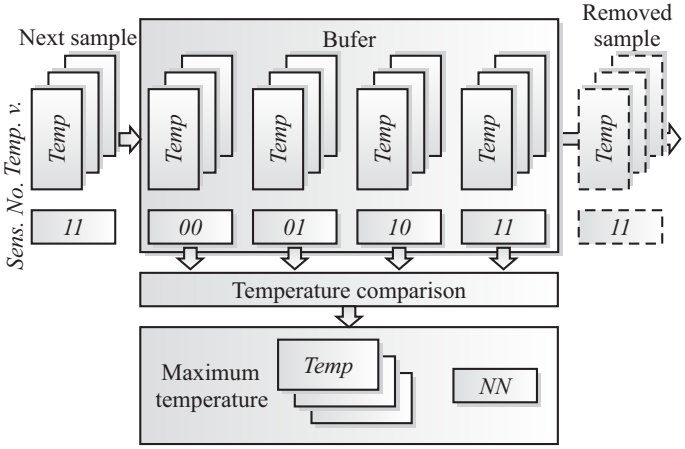

Fig. 9. Block diagram of the final block of maximum temperature detection

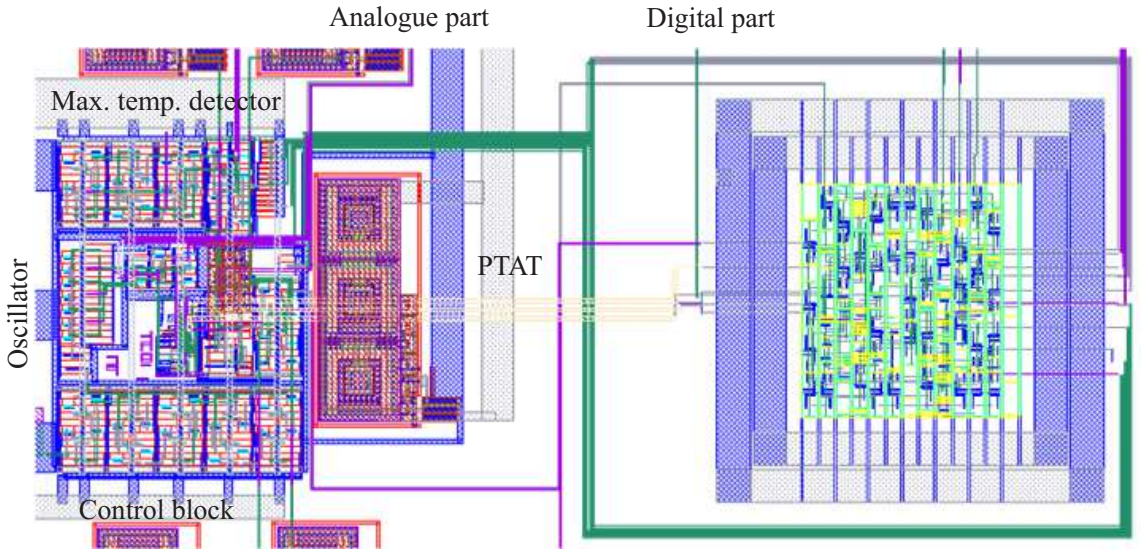

Fig. 10. Layout of the TCO with one of the PTAT sensors

The word is built of 3-bit temperature value from temperature comparator and 2-bit number of sensor from which the value comes. When a new value is prepared, it replaces the last value from the buffer. The moment of writing new sample to the buffer synchronizes temperature measurement and solves problems from previous asynchronous circuits. That way after each clock cycle the four temperature samples produced in four last clock cycles are stored in the buffer. Since thermal time constant of an integrated circuit is much larger then the clock period it can be assumed that in specified moment present temperature values from all four sensors are stored in the buffer. As the temperature is coded in n-of-3 code the temperature comparison of four samples is done by simple combinatory circuit. Result containing 3-bit value of maximum temperature found on the chip surface and 2-bit number of sensor which produced signal of maximum value are stored in special registers. These registers are available for read-only operation to both TCO and microprocessor which enables hardware and software methods of power management in the circuit. Structure of described buffer operation is depicted in Fig. 9.

Figure 10 presents layout of fabricated TCO. Its structure is divided into two separate parts: analogue (designed with full custom technique) and digital synthesized from code written in VHDL hardware description language. The digital part is recoiled from the analogue one because of noise reduction reasons. Important element of the analogue part is one of the PTAT sensors visible in presented part of circuit topography. Depicted structure of temperature sensor was chosen because bipolar transistors are easy to implement in CMOS technology as planar structures, but their important disadvantage is quite big area, what can be observed in the picture below. Designed circuit covers area of: $73 \times 100\,\mu\text{m}^2$ (analogue part without sensor) and $117 \times 120\,\mu\text{m}^2$ (digital part with supply ring lines).

Obviously every part of TCO consumes some amount of power. This power consumption is an additional cost which has to be paid if frequency control is needed. This extra cost can be considered as an disadvantage of described solution but ensures stabilization of the chip temperature and safe work of the circuit. Presented approach can significantly improve thermal behaviour of the chip. Main parameters of presented circuit are gathered in Tab. 2. Presented current consumption is a mean value and it has to be emphasized that it strongly depends on present value of chip temperature and its changes in time.

4 CONCLUSIONS

The paper described concisely structure and presented results of a system for detection of present maximum temperature on the surface of integrated circuit. The system consists of set of four temperature sensors and a decisive block. Information about value of maximum temperature found in the circuit and number of sensor which indicated this value is transferred for further processing. The system is a part of dynamic power management system designed for optimum control of microprocessor throughput under thermal constraints. The circuit has been fabricated in UMC CMOS 0.18 mm technology with 1.8 V supply. Future tests will include cooperation of dedicated microprocessor and optimization of circuit parameters.

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