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Simulation of cooling efficiency via miniaturised channels in multilayer LTCC for power electronics

Alena Pietrikova, * **Tomas Girasek,** * **Peter Lukacs,** *
Tilo Welker, ** **Jens Müller** **

The aim of this paper is detailed investigation of thermal resistance, flow analysis and distribution of coolant as well as thermal distribution inside multilayer LTCC substrates with embedded channels for power electronic devices by simulation software. For this reason four various structures of internal channels in the multilayer LTCC substrates were designed and simulated. The impact of the volume flow, structures of channels, and power loss of chip was simulated, calculated and analyzed by using the simulation software Mentor Graphics FloEFD^{TM}. The structure, size and location of channels have the significant impact on thermal resistance, pressure of coolant as well as the effectivity of cooling power components (chips) that can be placed on the top of LTCC substrate. The main contribution of this paper is thermal analyze, optimization and impact of 4 various cooling channels embedded in LTCC multilayer structure. Paper investigate, the effect of volume flow in cooling channels for achieving the least thermal resistance of LTCC substrate that is loaded by power thermal chips. Paper shows on the impact of the first chips thermal load on the second chip as well as. This possible new technology could ensure in the case of practical realization effective cooling and increasing reliability of high power modules.

K e y w o r d s: thermal simulation, thermal resistance, LTCC, cooling channels

1 Introduction

The interest in the fluidic structures is growing in LTCC in the recent years [4-5, 12, 15, 18, 19, 20]. LTCC is well suited as package solution for harsh environments due to their inherent features such as excellent thermal and chemical stability, hermiticity, simple 3D structuration, matching of thermal expansion coefficient with silicon and possibility of different fluidic and electrical component integration inside one ceramic substrate [1, 8, 10, 13-14, 16, 19]. Low temperature co-fired ceramics (LTCC) technology is mainly used for automotive technology, avionics, biology, military and telecommunication applications where the heat dissipation and high frequency property are mainly required [1-2, 11-12, 15]. These interesting features are used in different applications of industry, where is the necessity to cooling the devices by the coolant inside the microfluidic system, these applications include medical devices, sensors, chemical devices and power electronic devices [2-5, 7, 12, 18, 20].

Thermal management of power devices has becomes a serious problem with the electronics development of miniaturization, high performance and high reliability. The amount of the heat flux is growing up by the improvement of chip integration, package density, small size, layer quality, high frequency and high power loss in small area [3-4]. The electronic devices used in power electronic applications have to work properly in a very wide temperature range up to 200 °C. High temperature changes generate large thermal stress that affects solder joint reliability. Therefore, the thermal management analysis has been carried out at the preliminary stage of the manufacturing and design of the new devices and technologies. LTCC technology via small channels with flowing coolant allows a promising solution for improving heat dissipation and for decreasing the limited high temperature from the power chip for the reason of the advantages such as the small coefficient of thermal expansion (CTE), easiness to create 3D micro structure, low firing temperature and high density device integration capability [5-7, 17]. Cooling of power electronic devices is dependent on quality of joint between power chips and ceramic substrates. At this place, it is very important to show on the quality of solder joint between power chip and substrate that can influence thermal resistant as well as. Voids rate have the most important role in thermal conductivity of soldered joints which are created between ceramic substrates and power chips [21].

However, the poor thermal conductivity (which is about 3 to 5 Wm-1K-1) limits their application for power electronic devices [5-6]. For this reason, the poor thermal conductivity of LTCC has to be improved by a coolant, which is pumped through the fluidic channels inside the LTCC devices [1-3, 6-7, 9]. Integrated microchannel cooling system in LTCC substrate can decrease the additional

* Department of Technologies in Electronics, Faculty of Electrical Engineering and Informatics, Technical University of Košice, Letná 9, 040 01 Košice, Slovakia, alena.pietrikova@tuke.sk ** Electronics Technology Group, Technical University of Ilmenau, Gustav-Kirchhoff-Str.1, Ilmenau, 98693, Germany

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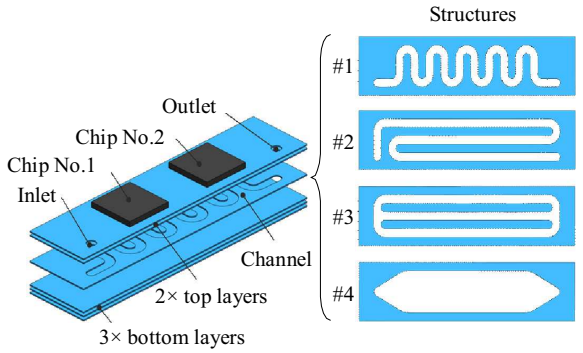

Fig. 1. Multilayered structure of LTCC substrate with embedded microchannels

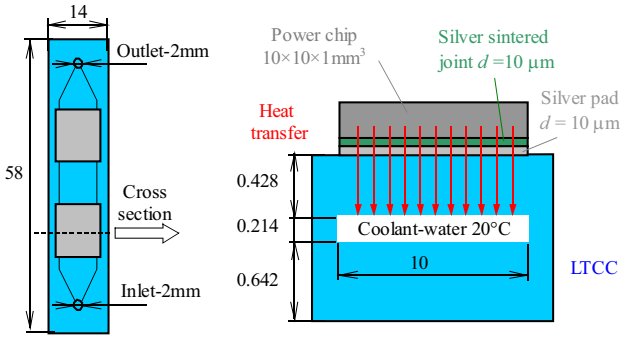

Fig. 2. Cross section of the simulation model with structure #4

temperature more than 80 % [20]. The main advantage of LTCC substrate with integrated liquid cooling system is the heat dissipation from the point of the thermal source. These devices therefore provide an excellent thermal performance for high power application with theoretical heat flux of 1000 W/cm^2 [2-3]. Moreover, the LTCC devices may not be bonded to a metal heat sink, which reduces the process steps, material, weight and volume that means less process steps within production.

This paper presents the comparison of thermal resistance, flow analysis, investigation of the impact of the first chips thermal load on the second chip and distribution of coolant in four various structures of internal channels in multilayer LTCC substrates. The paper shows possibility to utilize hermiticity of LTCC multilayer systems for creating embedded cooling channel. The dimensions and structure of microchannel has been chosen and modified to obtain better cooling performance for different working conditions. The heat transfer behaviours characterized by the decrease of maximum working temperature, thermal resistance of substrate, temperature distribution, fluid pressure and flow velocity fields were simulated by using the commercial simulation software Mentor Graphics FloEFD^{TM}. The results are helpful for the optimization design of microchannel structure and high power applications of liquid cooling microchannel in multilayered electronic LTCC substrates.

2 Four channels structure conceptions

The used material for the experiments is a commercially available green tape DuPont951®. The created 3D model consists of 6 layers of DuPont951® with 0.214 mm thickness and SiC chips with dimension $10 \times 10 \times$ mm^3 such as the thermal load generators. Thickness of the LTCC substrate was 1.2 mm. Simulation of cooling method based on multilayer LTCC was realized at 4 various structures of channels (Fig. 1). The fluidic channel integrated in the third layer from the top of the 3D model has the cross-sectional area of 2×0.214 mm^2 for the shape #1, #2, #3 and 10×0.214 mm^2 for the shape #4. All dimensions of the structures are listed in the Table 1. Multilayer structure of LTCC substrate is shown in Fig. 1.

Table 1. Dimensions of cooling channels structure

Structure	#1	#2	#3	#4
Channel:				
width (mm)	2	2	3 × 2	10
length (mm)	105	150	3 × 48	48
cross section (mm^2)	0.428	0.428	1.284	2.140
thickness of all channels 0.214 mm				
Area under the chip (mm^2)	71	60	60	100
Inlet and outlet hole dimension 2 mm, in all cases				

The silver sintered joints between the chips and silver pads are usually used for surface mounting due to their high thermal stability and high thermal conductivity. Thermal conductivity of silver sintered joints is 140 W/mK and for silver pads are 360 W/mK. The dimension of both layers is 10×10 mm^2 and the thickness is 10 μm. In all structure is used one channel of LTCC layer with thickness 0.214 mm. Inlet and outlet holes are the same for every substrate and diameter of holes are 2 mm. The position of power chip on the substrate is selected due to need to cooling the largest area of the chip by the flow of coolant in the channels. For the investigation of the impact of the first chips thermal load on the second chip, two chips placed on LTCC substrate were used. Figure 2 illustrates the cross section of the structure #4 of the cooling concepts realized by LTCC technology.

3 Simulations of thermal management in various channels

The thermal performance of analysed cooling methods is evaluated by the simulations in Mentor Graphics FloEFD^{TM} commercial simulation software. The junction temperature of the chip is simulated for a constant volume flow of coolant through the fluidic channels. For the simulation of the coolant the demineralized water

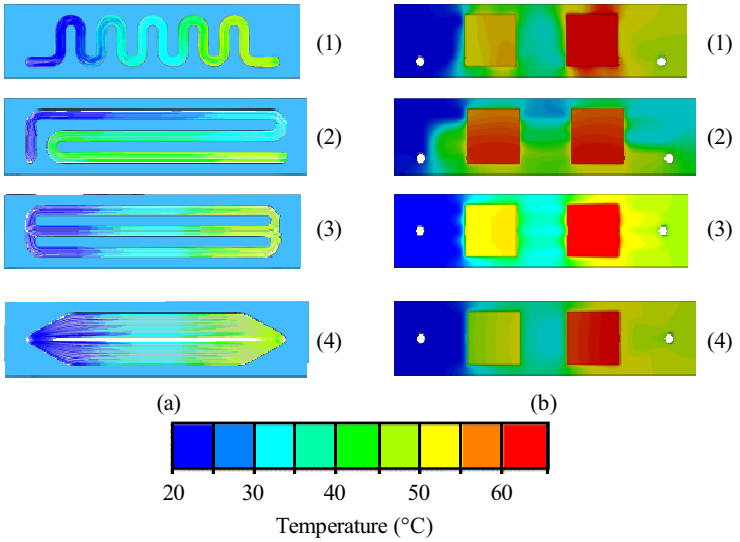

Fig. 3. Simulated temperature distribution of structure #1, #2, #3 and #4 at the thermal load of 10W per chip

Table 2. Key simulation parameters

Parameter	Value
Volume flow rate	10 to 300 ml/min
Thermal load	1 to 20 W
Coolant temperature	20 °C
Thermal conductivity in W/mK	
LTCC	3.3
Chips	120
Silver pads	360
Sintered joints	140
Density in g/cm^3	
LTCC	3.1
Chips	3
Silver pads	4.5
Sintered joints	3.1

with an inlet temperature of 20 °C was used. The thermal load of the chip was selected by the maximum junction temperature which does not exceed the boiling point of the water. The thermal resistance (R_{th}) was calculated from the temperature gradient between chip junction (θ_j), the inlet fluid (θ_{if}) and the thermal load (P) of chip (1) [5].

$$R_{\mathrm{th}} = \frac{\theta_j - \theta_{if}}{p} \tag{1}$$

The thermal resistance was calculated for different volume flow rate with the range of 10 ml/min to 300 ml/min. The key simulation parameters of thermal management are listed in Table 2.

The first type of channel (#1) was designed in the shape of meander with 11 curves. This channel was chosen for simulation and investigation of the curves impact on the fluids pressure inside the channels. The cooling area under one power chip in the structure #1 is 71 mm^2. The difference between the structures #1 and #2 is in the number of used curves and direction of flow fluid. This solution can reduce the pressure in the channel with maintaining the effectiveness of cooling. Cooling area under one of power chip in this structure is 60 mm^2. The structure #3 has three separate channels with a few curves such as can be seen in the Fig. 1. This structure of channel is created for the minimization of the pressure during high flow rate of demineralized water. The cooling area under the power chip in this case is 60 mm^2. The structure #4 has the one big channel with largest cooling area (100 mm^2) under one of power chip. However, the big cross section of channel (2.14 mm^2) provides fluently flow rate with minimum turbulence and decrease the pressure inside channel.

Figure 3 shows the simulated temperature distribution by coolant and substrate from the power chips realized by Mentor Graphics FloEFD$^{\mathrm{TM}}$. The volume flow is set to 10 ml/min and coolant fluid from left side to right. It can be seen that the temperature distribution is from the left side (inlet) to right side (outlet), what is caused by fluidic coolant. The volume flow rate of coolant is set to 10 ml/min. The simulations demonstrate the impact of the thermal load of first chip (left) on temperature of the second chip (right). The minimum impact is in the case of structure #2, which can be seen in Fig. 3 as well as in Fig. 5. In this structure, the coolant flows from the first chip No. 1 to second chip No.2 in the first step. After this the coolant continues again to the chip No. 1, which causes the balanced thermal resistance of both chips.

4 Discussion

In Fig. 4 the thermal resistance as a function of the volume flow rate of all 4 structures is plotted. The sim-

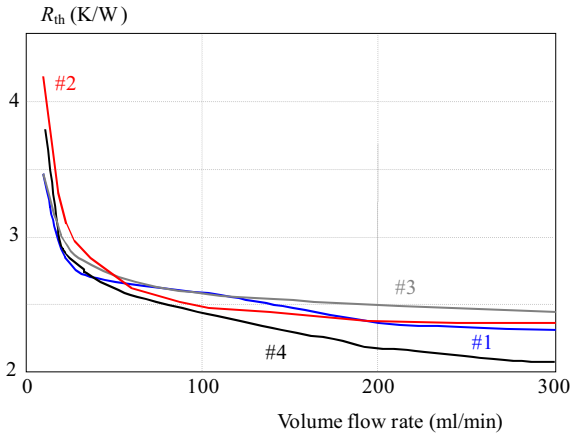

Fig. 4. The influence of volume flow rate on the thermal resitance

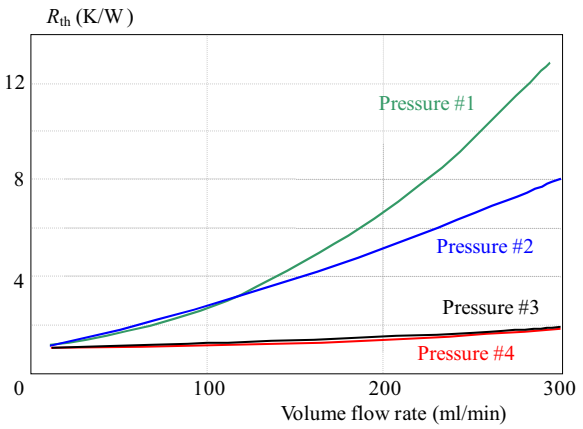

Fig. 5. The influence of volume flow rate on the pressure of coolant

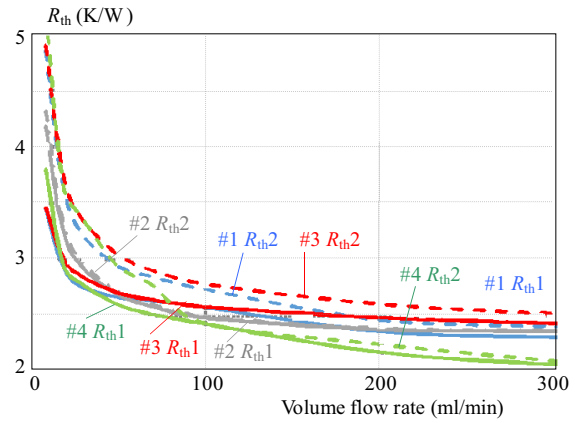

Fig. 6. Difference between thermal resistance of both chips for all structure

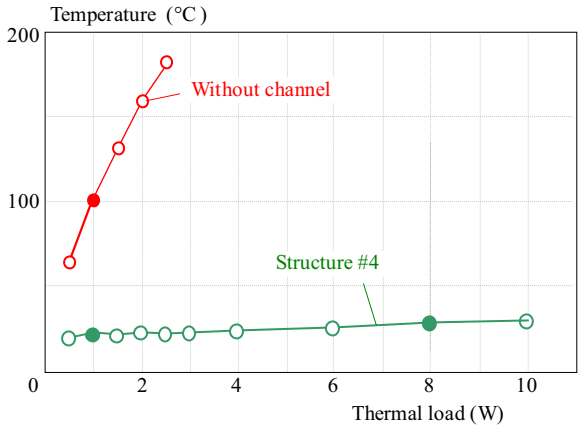

Fig. 7. Comparison of cooling efficiency of thermal loaded chips applied on multilayer LTCC structure

ulations demonstrate the design #4 has the lowest thermal resistance. The one biggest channel inside LTCC substrate reduces the thermal resistance by 2.8 % in average. The structure #2 has the worst thermal resistivity in the case of the flow rate is less than 50 ml/min. It can be seen that the thermal resistance is significantly dependent on the volume flow rate. At volume flow rate lower than 50 ml/min the thermal resistance (R_{th}) increases exponentially. On the other hand, the thermal resistance above 50 ml/min decreases slowly as it can be seen in Fig. 4.

The pressure of coolant inside the channel is also significantly dependent on the volume flow rate, especially in structure with small cross section and a lot of curves (structure #1, #2). The influence of volume flow rate on the pressure of coolant is shown in Fig. 5. The highest pressure (13.4 bar at 300 ml/min) is in the case of structure #1. In the structures #1 and #2 the pressure increases significantly by increasing the flow rate. Especially flow of coolant in the structure #1 is characterized by sharp curve radius. Volume flow rate of coolant at such small channel cross section (2.14 mm^2) is slowing down, thus increasing its pressure, Fig. 5. Simulation of cooling efficiency via cooling water flowed in miniaturized channels embedded in multilayer LTCC structures reports to be a new solution for power modules.

The lowest pressure 1.2 bar in average has the structure #3 and #4. These structures have almost constant pressure during all volume of flow rate (from 1.02 to 1.85 bar). Cross section is 1.28 mm^2 in structure #3 and 2.14 mm^2 in structure #4.

Structure #4 is the most promising candidate to cooling power chips on LTCC substrate for the reason of low thermal resistance at different volume flow rate as well as the simple fabrication requirements. In this structure the optimal flow rate to cooling the power chip is 150 ml/min. If the volume flow rate increases above 150 ml/min the thermal resistance is relatively stable, Fig. 4. Structure #4 gives possibility for optimal flow rate and optimal cooling effect of power chips. Structure #4 reduces the thermal resistance by 2.8

In Fig. 6 the thermal resistance of both chips as a function of the volume flow rate is plotted. The simulations demonstrate the impact of the thermal load of the first chip (No.1) on the temperature of the second chip (No.2). The thermal resistance of substrate is different for the chips No.1 and No.2 in all structures. The high-

est difference of thermal resistance is at structure #1, #3 and #4, 12.9 % in average. This difference is caused by direct flow of fluid from chip No.1 to chip No.2. At chip No.1 there is the transfer of the thermal energy on to chip No.2 by the coolant in the channel. At the structure #4 the difference of the thermal resistance is approximately 0.1 % at optimal flow rate 150 ml/min. The minimum difference of 1.3 % is at the structure #2. It is because the coolant flows from the chip No. 1 to chip No. 2 in the first step. After this the coolant continues again to the chip No. 1, which causes the balanced thermal resistance of both chips, Fig. 3.

Comparison of cooling efficiency of thermal loaded chips applied on multilayer LTCC structure with (type structure #4 with volume flow rate 150 ml/min) and without embedded cooling channels have been realized, see Fig. 7. Simulation via Mentor Graphics FloEFD^{TM} pointed at very different results. Thermal loading from 0.5 W to 2.5 W in the case of structure without channels increases the chip temperature from 64.7 °C to 184 °C. As it can be seen in Fig. 7, increasing of thermal loading in the multilayer structure #4 at much higher range (from the 0.5 W to 10 W) causes only softly increase of the temperature. Important is that such structure has very stable cooling efficiency.

5 Conclusions

This paper reports on possible solution of new method of increasing the power modules performance via cooling water flowed in miniaturized channels embedded in multilayer LTCC structure as substitute of standard DBC substrate.

The cooling efficiency of four types of miniaturized fluidic channels embedded in multilayer LTCC structure were simulated, analysed and compared. The influence of the various channel structures on the thermal resistance and pressure of the coolant was investigated based on simulation by Mentor Graphics FloEFD TM. The simulations show that there is a nonlinear relation between the volume flow rate and the thermal resistance. Increasing the mass flow rate of the coolant causes the reduction of the thermal conductivity as well as causes the pressure rise inside the channels due to turbulent flow of coolant. The structures of channels have the significant impact on the coolant pressure. Substrate with structure #4 is the most promising candidate to cooling power chips on LTCC substrate, for the reason of low thermal resistance at different volume flow rate. Structure #4 reduces the thermal resistance by 2.8 % in average in compare to structure #1, #2, #3. Multilayer LTCC structure with channel #4 can decreased additional temperature of chips about 86% (at 2 W) in comparison with multilayer LTCC structure without embedded cooling system. The simulations demonstrate the impact of the thermal load of first chip (No.1) on the temperature of the second chip (No.2). The minimum difference 1.3 % of the thermal resistance is at structure #2. At the other structures the difference of the thermal resistance is approximately 12.9 % in average at the volume rate flow lower than 150 ml/min.

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Alena Pietrikova received PhD degree in material science in 1986. She is full professor (2007) of electrotechnology and materials at the Faculty of Electrical Engineering and Informatics Technical University of Košice, Slovakia. Her research work is concentrated on problems concerned with modern materials and technologies in electronics (film technologies, assembling technologies in electronics, and materials for electronics). She is an author or co-author of more than 250 research articles in international journals or conference proceedings, 5 patents and 5 books. She is the head of Department of Technologies in Electronics and vice-dean at Faculty of Electrical Engineering and Informatics Technical University of Košice responsible for research and PhD study.

Tomas Girasek was born in 1989. In 2014 he graduated (MSc) with distinction at the Department of Technologies in Electronics of the Faculty of Electrical Engineering and Informatics at Technical University in Košice. Now, he is a PhD student at the same department. His scientific research is oriented to thermal management, multilayer structures, ceramic circuits and joints in power electronics.

Tilo Welker, born in 1984, received his Diploma degree in computer engineering specialized in integrated hard- and software systems 2009, from the Ilmenau University of Technology, Germany. He is a scientific co-worker at the Institute of Micro- and Nanotechnologies at the Ilmenau University of Technology, Germany. Main interest of his research includes thermal management, packaging, ceramic circuits and 3D integration, having 12 papers published as author and more than 20 as co-author.

Jens Müller, born September 1965, received his diploma degree for electrical engineering and the doctoral degree from Ilmenau University of Technology, Ilmenau, Germany, in 1992 and 1997 respectively. From 1997 to 2005, he held managing positions in development departments at Micro Systems Engineering GmbH, Berg, Germany. In 2005, he returned to Ilmenau University of Technology to establish the junior research group Functionalised Peripherics. In July 2008 he was assigned full professor at the Department of Electronics Technology at the same university. His particular research interest covers functional integration for ceramic based System-in-packages considering aspects of harsh environmental use, and high thermal / high-frequency requirements with a strong focus on LTCC materials and its combination with Silicon by a proprietary process. Since June 2012 he has been the director of the Institute of Micro- and Nanotechnologies MacroNano and the director of the Center for Micro- and Nanotechnologies at Technische Universitt Ilmenau.