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PAPERS

A high electrical performance of DG-MOSFET transistors in 4H-SiC and 6H-SiC 130 nm technology by BSIM3v3 model

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In this paper, the electrical performance of double gate DG-MOSFET transistors in 4H-SiC and 6H-SiC technologies have been studied by BSIM3v3 model. In which the I–V and g_{m}–V characteristics and subthreshold operation of the DG-MOSFET have been investigated for two models (series and parallel) based on equivalent electronic circuits and the results so obtained are compared with the single gate SG-MOSFET, using 130 nm technology and OrCAD PSpice software. The electrical characterization of DG-MOSFETs transistors have shown that they operate under a low voltage less than 1.2 V and low power for both models like the SG-MOSFET transistor, especially the series DG-MOSFET transistor is characterized by an ultra low power. The different transistors are characterized by an ultra low OFF leakage current of pA order, very high ON/OFF ratio of and high subthreshold slope of order 0.1 V/dec for the transistors in 6H-SiC and 4H-SiC respectively. These transistors also proved higher transconductance efficiency, especially the parallel DG-MOSFET transistor.

K e y w o r d s: 4H-SiC, 6H-SiC, BSIM3v3, DG-MOSFET, nm technology, $4\,I-V$ characteristics, subthreshold operation

1 Introduction

In the last decade, modern technology has been concerned with the study of mini components electronic at the nanoscale, especially the Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) [1]. This is what led to the development of devices and integrated circuits (ICs). However, despite all this development, MOSFET transistors have suffered from the serious effects of the Short Channel Effect (SCE) on her electrical behavior [2, 3]; this necessarily affects the characteristics of CMOS integrated circuits. In order to reduce this influence, Double-Gate (DG) structure, has been proposed as a promising solution to replace the conventional MOSFET structure in nanoscale technology [3–5]. Having two gates ensures excellent control of short channel effects (SCE) and improves the capacity of the control of the current through control of the channel.

The DG-MOSFETs transistors in Silicon technology have been shown to be more optimal for ultra-low power circuit design due to the reduced leakage current and the improved subthreshold slope compared to bulk CMOS [6].

In addition, many materials have been proposed to replace silicon technology, among these materials Silicon Carbide (SiC) [7], this is due to their distinctive char-

Table 1. Basic parameters of 4H-SiC and 6H-SiC at $T = 300$ K

Materials / Parameters	4H-SiC	6H-SiC
E_g (eV) Energy gap	3.36	3.02
μ_e (cm^2/Vs) Electron mobility	1000- 1140	400-800
μ_h (cm^2/Vs) Hole mobility	115	90
N_i (cm^{-3}) Intrinsic carrier concentration	8.2×10^{-9}	2.3×10^{-6}
Dielectric permittivity (ε)	6.63	6.58
$V_{\mathrm{sat}} \times 10^7$ (cm/s)	2	2
Thermal conductivity $\mathcal{K}$ (W $\mathrm{m}^{-1}\mathrm{K}^{-1}$)	4.9	4.9

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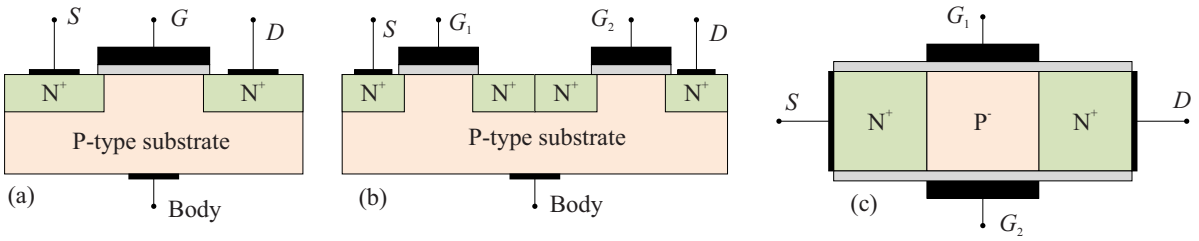

Fig. 1. Different structures of transistors: (a) – SG-MOSFET, (b) – series DG-MOSFET, (c) – parallel DG-MOSFET

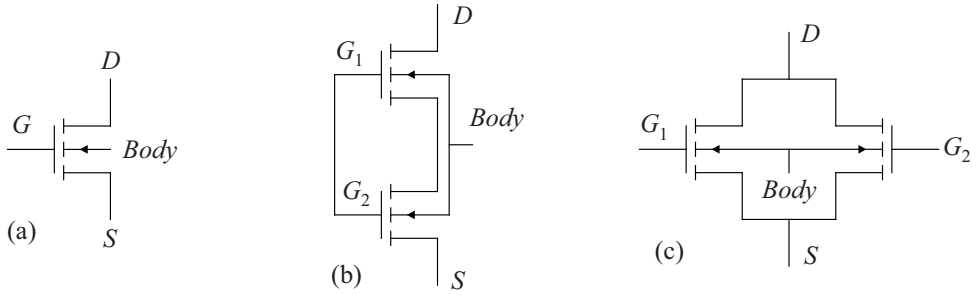

Fig. 2. (a) – SG-MOSFET transistor, equivalent electronic circuits, (b) – series DG-MOSFET, (c) – parallel DG-MOSFET [20]

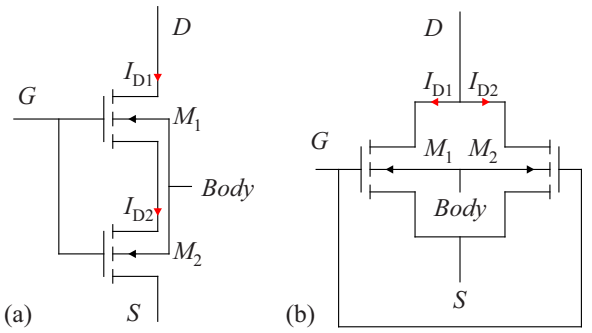

Fig. 3. Drain current of DG-MOSFETS transistors,(a) – series (model 1), (b) – parallel (model 2)

acteristics such as wide bandgap, high thermal conductivity, high breakdown field and high saturation velocity of electrons Table 1 [8]. This is why it is used in the manufacture of electronic devices with high-voltage, high-power, high-frequency and which operate within a wide range of temperature [9]. The SiC is characterized by many polytypes [8], the most important and most commonly used of which in electronic applications are 4H-SiC and 6H-SiC. In addition to using this technology in the MOSFET transistors, they were also used to manufacture the high-voltage and high-power DG-MOSFET transistors [7, 10, 11] or in the form of SiC/SiO_2 layer in these transistors [12, 13]. In the last few years, research has shown that the submicron electronic devices in SiC technology work well in low voltage and low power [14–17].

In this paper, we will study and characterize the electronic behavior of DG-MOSFETs transistors in 4H-SiC and 6H-SiC technologies with submicron scale in order to operate at low-voltage and low-power. Based on the Single Gate (SG) MOSFET transistor by BSIM3v3 Model and using two equivalent electronic circuits of DG-MOSFET transistor Series and Parallel models, we simulate the different $I-V$ characteristics (Output characteristic $I_D = f(V_{DS})$ and Transfer characteristic $I_D = f(V_{GS})$. Subthreshold operation (To find the different parameters in this region as I_{ON}/I_{OFF} ratio and subthreshold slope SS) and $g_m - V$ characteristic of our transistors, and then we will carry out a comparative study between SG-MOSFET and DG-MOSFETs transistors for 4H-SiC and 6H-SiC technologies.

Our work will be carried for 130 nm technology, 1.2 V supply voltage and we will use the OrCAD(PSpice) software to simulate the different characteristics of our devices.

2 DG-MOSFETs transistors structures and models

Figure 1 shows the different structures of the SG-MOSFET and DG-MOSFETs transistors. The series topology of a DG-MOSFET transistor (Model 1) is essentially a series arrangement of two separate channels [18–20], with each channel having an independent gate connection to control the flow of current as shown in the Fig. 1(b). For the second DG-MOSFET transistor topology (Model 2) [20], two MOSFET transistors are connected in parallel of the same substrate (Body) as shown in the Fig. 1(c). Figure 2 shows the two equivalent electronic circuits models (series and parallel) of DG-MOSFET transistor based on the SG-MOSFET transistor. As shown in Figs. 2(b) and 2(c), the two models of DG-MOSFETs transistors are based on the same SG-MOSFET transistor, this transistor carries the following descriptions: length and width of the channel

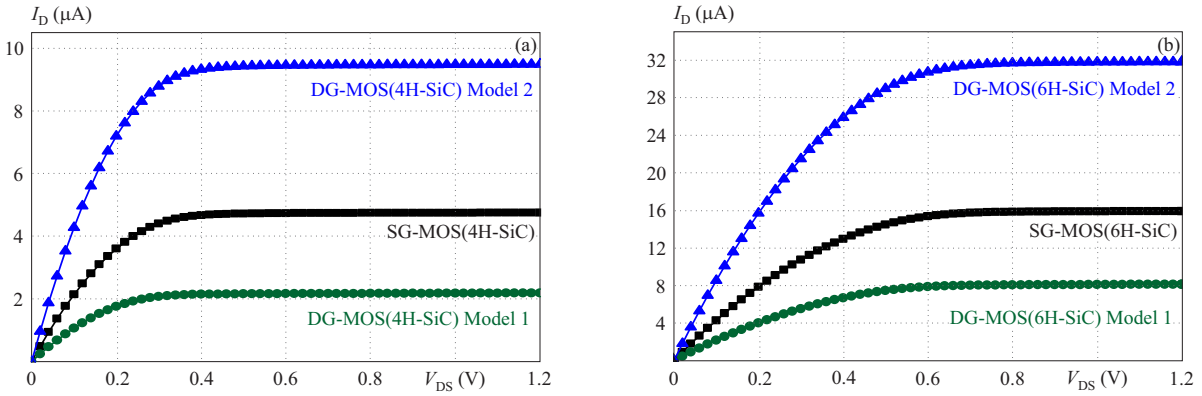

Fig. 4. Output characteristic of SG-MOSFET and DG-MOSFETS transistors in, (a) – 4H-SiC and (b) – 6h-SiC technology

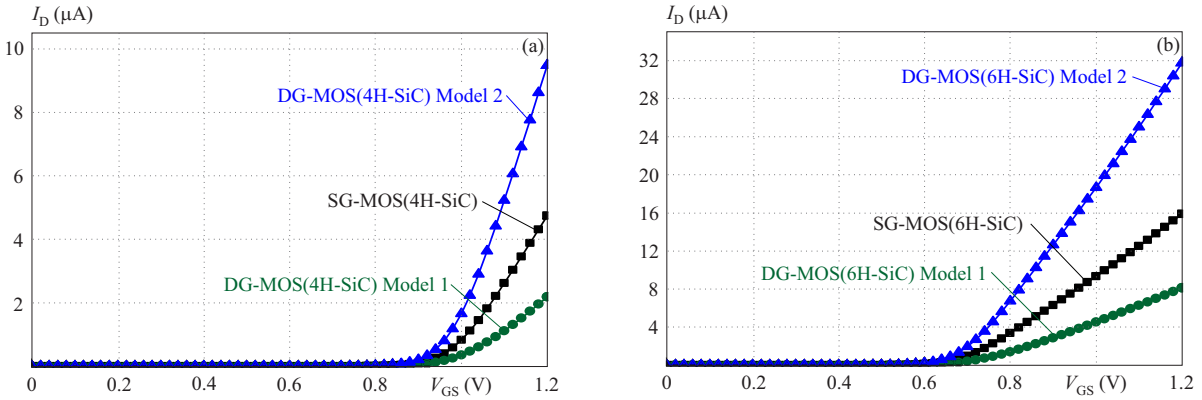

Fig. 5. Transfer characteristic of SG-Mosfet and DG-MOSFET transistors in: (a) – 4h-SiC, and (b) – 6h-SiC technology

$L = 130\,\text{nm}$ and $W = 160\,\text{nm}$, respectively, the thickness of the oxide layer (SiO_2) $T_{ox} = 2.3\,\text{nm}$ and using the same doping value of the source, the drain and the gate $N_S = N_D = N_G = 10^{20}\,\text{cm}^{-3}$). The doping of the channel and the substrate $N_{ch} = 2.3549 \times 10^{17}\,\text{cm}^{-3}$ and $N_{sub} = 6 \times 10^{16}\text{cm}^{-3}$, respectively. For the simulation of the MOS transistor by the model BSIM3v3, must be used the level 7 in the software OrCAD(PSpice) [15].

In this work, to study the electrical behavior of the different models of the DG-MOSFETs transistors, we will use polarization symmetry ($V_{GS1} = V_{GS2}$) in both cases of constant or variable as shown in Fig. 3.

For the series DG-MOSFET transistor, the (W_{eq}/L_{eq}) geometric equivalent ratio of the channel given by [21]

$$\frac{W_{eq}}{L_{eq}} = \frac{W}{L_{G1} + L_{G2}} = \frac{W}{2L}\,. \tag{1}$$

So the drain current of this DG-MOSFET transistor model can be expressed as

$$I_D^{(M1)} = \frac{1}{2} I_D^{(SG)}\,. \tag{2}$$

According to the equivalent circuit of the parallel DG-MOSFET transistor, the drain current expression of this model (M2) is given by

$$I_D^{(M2)} = I_{D1} + I_{D2}\,. \tag{3}$$

So

$$I_D^{(M2)} = 2 I_D^{(SG)}\,. \tag{4}$$

From (2) and (4), the relation between the drain currents of these models (M1, M2) can be expressed as

$$I_D^{(M2)} = \frac{1}{4} I_D^{(M1)}\,. \tag{5}$$

3 Results and discussion

3.1 I–V characteristics

Figure 4 shows the output characteristic $I_D(V_{DS})$ of the SG-MOSFET and DG-MOSFETs transistors in 4H-SiC and 6H-SiC technologies at room temperature. For this characteristic voltage $V_{GS} = 1.2\,\text{V}$ and $V_{GS1} = V_{GS2} = 1.2\,\text{V}$ for SG-MOSFET and DG-MOSFETs respectively, the VDS voltage is varied from 0 V to 1.2 V.

The drain current ID expression of a SG-MOSFET transistor by BSIM3v3 model is given by [22, 23]

$$I_D = \frac{\mu_{eff} C_{ox} W}{L + V_{DS}/E_{sat}} \left(V_{GS} - V_{th} - \frac{A_{bulk} V_{DS}}{V_{DS}} \right) V_{DS} \tag{6}$$

where μ_{eff} is the effective mobility, C_{ox} is the gate capacitance per unit area, the parameter E_{sat} corresponds

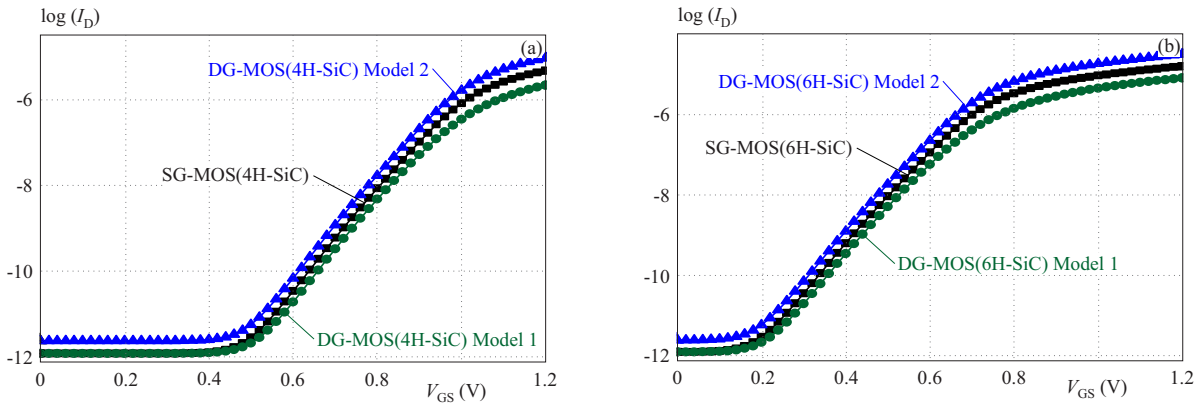

Fig. 6. LOG(I_D) with V_{GS} of SG-MOSFET and DG-MOSFET transistors in, (a) – 4h-SiC, and (b) – 6H-SiC technology

to the critical electrical field at which the carrier velocity becomes saturated, and the parameter A_{bulk} is used to take into account the bulk charge effect.

The different models of DG-MOSFETs transistors work correctly (Ohmic and Saturation regions) like the SG-MOSFET transistor in the 1.2 V voltage for the different semiconductor technologies as shown in Fig. 4. According to this characteristic ($I_D = f(V_{DS})$), the transistors in 4H-SiC technology are characterized by a low I_D drain current compared to the transistors in 6H-SiC technology for the different models (SG-MOSFET and DG-MOSFETs) because of the difference of the threshold voltage $V_{th(6H\text{-}SiC)} < V_{th(4H\text{-}SiC)}$ whhich is related to the energy band-gap $Eg_{(6H-SiC)} < Eg_{(4H-SiC)}$ in Table 1 of these semiconductors except the series DG-MOSFET transistor in 6H-SiC and Parallel DG-MOSFET transistor in 4H-SiC which are characterized by saturation currents I_{Dsat} of 8.119 μA and 9.489 μA respectively as shown in Table 2.

The parallel DG-MOSFET transistor (Model 2) is characterized by a drain current 2 times and 4 times greater than that SG-MOSFET and series DG-MOSFET (Model 1) transistors respectively for 4H-SiC and 6H-SiC technologies as expected from (2), (4) and (5). The low drain current of series DG-MOSFET transistor can be attributed to the channel length of this model compared to other transistors. In addition, the results of this characteristic show that the DG-MOSFETs transistors in 4H-SiC and 6H-SiC technologies work well in low power like the SG-MOSFET transistor at submicron technology [14], especially the series DG-MOSFET transistor which is characterized by an ultra low power compared to other transistors. Thus, the DG-MOSFET transistor in series structure is very suitable for low power applications.

Figure 5 shows the I_D current evolution as a function of V_{GS} voltage of the SG-MOSFET and DG-MOSFETs transistors in 4H-SiC and 6H-SiC technologies at the voltage of V_{DS} = 1.2 V and the voltages of V_{GS1} and V_{GS2} ($V_{GS1} = V_{GS2} = V_{GS}$) are varied from 0 V to 1.2 V.

The threshold voltage is directly proportional to the energy gap E_g and is inversely proportional to the carrier concentration n and according to the electronic properties of the 4H-SiC and 6H-SiC semiconductors in Table 1. This is what makes the SG-MOSFET and DG-MOSFETs transistor in 6H-SiC technology are characterized by a low value of the threshold voltage compared to others transistors in 4H-SiC technology as shown in Fig. 5.

For SG-MOSFET and parallel DG-MOSFET (Model 2) transistors with uniform substrate doping concentration, threshold voltage V_{th} is given by [22, 23]

$$V_{th}^{(SG)} = V_{th}^{(M2)} = V_{th}^{(id)} + \gamma\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) \quad (7)$$

where $V_{th}^{(id)}$ is the threshold voltage of the long channel device at zero substrate bias, γ is the body bias coefficient, and Φ_s is the surface potential.

The results of these characteristics ($I_D = f(V_{GS})$) show that the SG-MOSFET and parallel DG-MOSFET (Model 2) transistors are characterized by the same value of the threshold voltage for the different semiconductor technologies (4H-SiC and 6H-SiC). The SG-MOSFET transistor is characterized by a single Φ_s surface potential, but the series DG-MOSFET transistor (Model 1) is characterized by two surface potentials following the two contacts of each gate as shown in the following expression [20]

$$V_{th}^{(M1)} = V_{th}^{(id)} + \gamma\left(\sqrt{2\Phi_s - V_{bs}} - \sqrt{2\Phi_s}\right). \quad (8)$$

From this, the series DG-MOSFET transistor (Model 1) is characterized by a high value of the threshold voltage compared to parallel DG-MOSFET and SG-MOSFET transistors for the different semiconductor technologies (4H-SiC and 6H-SiC) as shown in Fig. 5.

3.2 Subthreshold DG-MOSFET operation

Among the features that demonstrate the quality of the electrical performance of the transistor is its operation in Sub-threshold. Figure 6 shows the evolution of LOG(I_D) as a function of the V_{GS} voltage for the different DG-MOSFETs and SG-MOSFET transistors in 4H-SiC and 6H-SiC technologies at the voltage of V_{DS} = 1.2 V.

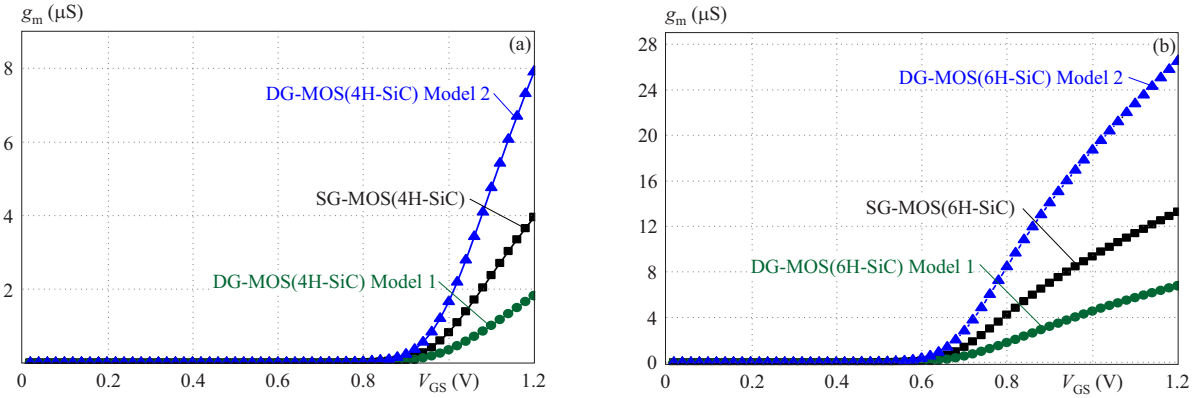

Fig. 7. Transconductance g_m with VGS of SG-MOSFET and DG-MOSFET transistors in: (a) – 4h-SiC, and (b) – 6h-SiC technology

The I_{ON}/I_{OFF} ratio of the SG-MOSFET and DG-MOSFETs transistors by BSIM3v3 model is defined by [15]

$$\frac{I_{ON}}{I_{OFF}} = \exp\frac{V_{DD}}{\eta V_T} \tag{9}$$

where $V_{DD} = V_{DS} = 1.2$ V is the supply voltage, V_T is the thermal voltage, and η is the subthreshold swing parameter.

Silicon-Carbide (SiC) is semiconductors with very low value for carrier concentration n. This is what makes the SG-MOSFET and DG-MOSFETs transistors of this technology are characterized by an ultra low I_{OFF} leakage current and are characterized by a very high I_{ON}/I_{OFF} ratio of order 10^7 and 10^6 for the transistors in 6H-SiC and 4H-SiC respectively as shown in Table 1. According to these results and based on (9), the transistors in 4H-SiC technology are characterized by a high η subthreshold swing parameter compared to the transistors in 6H-SiC technology, This allows it to be more optimal for the design of electronic devices that operate in subthreshold region.

The simulation results show that the series DG-MOSFET transistor (Model 1) is characterized by an I_{ON}/I_{OFF} ratio 10 times lower than that SG-MOSFET and parallel DG-MOSFET (model 2) transistors for 4H-SiC and 6H-SiC technologies because it is characterized by the highest value of the I_{ON} current compared to other types of transistors as shown in Fig. 6.

The Subthreshold Slope (SS) of a MOSFET transistor is defined by the following relation, and is considered among the most important parameters

$$SS = \frac{\mathrm{d}V_{GS}}{\mathrm{d}\log(I_D)}. \tag{10}$$

The results presented in Table 2 show that the transistors SG-MOSFET and DG-MOSFETs are characterized by a high subthreshold slope SS of order 86 mV/dec and 85 mV/dec for the transistors in 4H-SiC and 6H-SiC respectively compared to the ideal 60 mV/dec subthreshold slope in room temperature [24, 25], this value corresponds to the theoretical relationship $SS = \big(K_B T/q\big)\ln(10)$ [25]. This proves that these transistors are subject to tunnel effect in subthreshold operation, particularly the series DG-MOSFET transistor (Model 1) to distinguish it with the greatest subthreshold slope SS compared with the rest of the transistors; this is consistent with the properties of the BSIM3v3 model. And since the SS parameter illustrating the speed of the device to open [26], because he is considered an important physical quantity to measure the conversion speed of the transistor from the off state to the open state [25, 26]. So that whenever the SS is small, the transistor will open faster. According to this, the Series DG-MOSFET (Model 1) transistor is will open slow compared to other transistors for different semiconductor technologies as shown in our results, and transistors in 6H-SiC technology are faster ON-OFF switching compared to the transistors in 4H-SiC technology. That is what makes the parallel DG-MOSFET and the transistors in 6H-SiC technologies more suitability for digital applications.

3.3 g_m–V characteristic

In order to study of a SG-MOSFET and DG-MOSFETs transistors performances, the transconductance g_m must be studied, because it is considered among the most important analog performance parameter [27] and is determined by the following relation

$$g_m = \frac{\mathrm{d}I_D}{\mathrm{d}V_{GS}}. \tag{11}$$

According to (11) and based on the drain current (6), the transconductance g_m as a function of V_{GS} of a SG-MOSFET transistor for BSIM3v3 model is given by

$$g_m(V_{GS}) = \frac{C_{ox} W V_{DS} E_{sat}}{L E_{sat} + V_{DS}} \left(\mu_{eff} + V_{GS}\frac{\mathrm{d}\mu_{eff}}{\mathrm{d}V_{GS}}\right). \tag{12}$$

Figure 7 shows the effect of gate voltage V_{GS} variation on transconductance g_m evolution V_{GS} of the SG-MOSFET and DG-MOSFETs transistors in 4H-SiC and 6H-SiC technologies at Drain-Source voltage $V_{DS} = 1.2$ V.

The g_m–V characteristic is extremely related with the I_D–V_{GS} characteristic according to (11), and then both

Table 2. The different parameters of the SG-MOSFET and DG-MOSFET transistors in 4H-SiC and 6H-SiC technology

Transistors	4H-SiC technology			6H-SiC technology		
		Series	Parallel		Series	Parallel
	SG-MOSFET	DG-MOSFET		SG-MOSFET	DG-MOSFET	
Electrical parameters		(Model 1)	(Model 2)		(Model 1)	(Model 2)
V_{th} (V)	0.97	1	0.97	0.7	0.78	0.7
I_{Dsat} (μA)*	4.7449	2.188	9.489	15.903	8.119	31.806
$I_{\text{ON}}/I_{\text{OFF}}$ ratio	3.92×10^6	1.81×10^6	3.92×10^6	1.31×10^6	6.70×10^6	13.1×10^6
SS (mV/dec)	86.134	87.349	86,134	85.498	86.493	85.498
g_{m} (μS)**	3.954	1.823	7.908	13.253	6.773	26.505

*($V_{\text{GS}} = 1.2$ V), **($V_{\text{GS}} = V_{\text{DS}} = 1.2$V)

characteristics have the same form of evolution, that is to say the transconductance value of the parallel DG-MOSFET transistor is high compared to the other transistors for different semiconductor technologies.

The mobility μ_{eff} and derivative of mobility are very important parameters that are directly proportional to the variation of the V_{GS} voltage in the BSIM3v3 model [22, 23], and according to the expression of the transconductance $g_{\text{m}}(V_{\text{GS}})$, this characteristic is increased by increasing the VGS voltage for the SG-MOSFET and DG-MOSFETs transistors in 4H-SiC and 6H-SiC technologies as shown in the Fig. 7.

The g_{m}–V characteristic shows that the transconductance g_{m} of the different transistors in 4H-SiC technology is lower and more linear (Above-threshold region) compared to the transistors in 6H-SiC technology except the Parallel DG-MOSFET transistor in 4H-SiC and series DG-MOSFET transistor in 6H-SiC which are characterized by transconductance of 7.908 μS and 6.773 μS respectively as shown in Table 2. Since the transconductance g_{m} is considered a measure of the amplification given by these transistors [27]. That's what makes the transistors in 6H-SiC technologies and Parallel DG-MOSFET transistor in 4H-SiC and 6H-SiC technologies are characterized by more efficient amplification and more suitability for analog applications.

Table 2 is a performance summary of the SG-MOSFET and DG-MOSFETs transistors with Series and Parallel models in 4H-SiC and 6H-SiC technologies at room temperature. Table 2 shows a presentation of the different electrical parameters of the SG-MOSFET and DG-MOSFETs transistors, and shows the comparison of the electronic behavior between the two models of the DG-MOSFETs transistors and consequently the comparison with the SG-MOSFET transistors.

4 Conclusion

In this work, the electrical characteristics of series and parallel DG-MOSFETs transistors in 4H-SiC and 6H-SiC technologies have been investigated using equivalent electronic circuits based on a BSIM3v3 model with 130 nm technology. The structure type effect on electrical performances of DG-MOSFET transistor have been studied and carried out a comparative study between the results of the DG-MOSFETs and SG-MOSFET transistors. The DG-MOSFET transistor in series structure has high threshold voltage and ultra low power than all other transistors. As for the DG-MOSFET transistor in structure parallel it is characterized by high ON/OFF ratio of order 10^6 and faster ON-OFF switching like the SG-MOSFET transistor, high value of the transconductance and more efficient amplification compared to other transistors. The DG-MOSFETs transistors that were studied in this work showed the high electrical performances in the static characteristics and in the subthreshold operation. Therefore, these advantages make these transistors a suitable candidate for analog and digital applications in low voltage and ultra low power with submicron technology.

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