Journal of ELECTRICAL ENGINEERING, VOL 72(2021), NO2, 113–118

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PAPERS

Design and verification of a low-power AC/DC converter

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This paper deals with the development and experimental verification of a low-power AC/DC converter. The proposed solution is aimed at the sub 0.5 W output power domain, commonly encountered in applications such as always-on wireless sensing nodes. To implement the proposed converter topology, a prototype application specific integrated circuit was designed and manufactured in a high voltage 0.35 μm CMOS technology, able to handle the maximum voltage of up to 120 V. The proposed design was first analyzed by transistor-level simulations showing high power efficiency and low no-load consumption of the developed converter. To facilitate experimental verification and measurement, an printed circuit board with the necessary external components was developed, as the available technology is unable to handle the AC line voltage directly. While the developed converter operated well with decreased input AC voltage, reliability issues arose during operation with the full AC line voltage of 230 Vrms. These are linked to digital control circuitry of the implemented chip and could be addressed in the second manufacturing run in the future.

K e y w o r d s: AC/DC power conversion, CMOS integrated circuits, low-power design, power efficiency, ASIC, sensor nodes

1 Introduction

Recent advances in integrated circuit design methodologies as well as new semiconductor manufacturing technologies have enabled the development of integrated solutions with increased performance and extended functionality, while simultaneously becoming smaller, cheaper and more power-efficient. With these advancements, the deployment of wireless sensor nodes on a massive scale has become possible. Such sensor nodes can be utilized as parts of monitoring systems suitable for diverse commercial applications. These include smart home and home automation systems as well as infrastructure and industrial monitoring systems.

Battery-powered sensor nodes with the expected lifetime of 2–5 years are currently typical in such applications. However, for some applications, such as continuous monitoring systems for smart grid management, a battery with acceptable dimensions is not suitable as the main energy source. This is largely due to the increased power requirements of always-on sensor nodes. This creates a need for AC/DC conversion solutions with the output power requirement of below 1 W [1]. Currently available commercial solutions are typically designed with higher output power ranges in mind, and are thus not suited for operation in that power range, since typically suffering from poor power efficiency. Therefore, improved converter solutions are required with enhanced performance in these applications. This was the main motivation for the development of the AC/DC converter proposed in this paper.

The rest of the paper is organized as follows. Section 2 gives a brief overview of solutions that can be considered the state of the art. Section 3 describes the proposed AC/DC converter topology and gives more details on the main circuit blocks of the developed application specific integrated circuit (ASIC). Section 4 gives a detailed overview of the measurement methodology. It also provides the measured data as well as a discussion on the overall results of the experimental verification. In Section 5, conclusions are drawn.

2 State of the art

Commercially available solutions that can be deemed as the state of the art in low-power non-isolated AC/DC conversion are often based on a switch mode power supply solution utilizing the flyback topology, which has been proven to work efficiently under low power conditions [2]. These include solutions such as: TEA1721 from NXP [3], VIPer01 [4] and STCH03 [5] from ST-I, or UCC28720 [6] from Texas Instruments. Non-isolated AC/DC converter solutions based on these controllers provide peak efficiencies around 70–75 % for the output loads of 1–2.5 W. For output loads in the range of 200–500 mW, the efficiency drops to values around 65 %. This is partially caused by the fact that these circuits are targeting higher nominal output loads of up to 8 W. The TPS7A78 [7] from Texas Instruments is a non-isolated solution based on a dropper capacitor connected to an active rectifier, switched capacitor voltage convertor and a low-dropout (LDO) linear regulator. The efficiency of up to 75 % and a stand-by

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https://doi.org/10.2478/jee-2021-0015, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

Table 1. Average power consumption and efficiency obtained by simulations

Power consumption (W)					Load		
HV driver	LV analog	LV digital	MOS switch	Total	Power (W)	Resistance (Ω)	Efficiency (%)
330 μ	270 μ	9.7 n	47 m	74 m	405 m	1.5 k	84.5
4.5 μ	255 μ	5.8 n	18.5 m	37 m	215 m	3 k	85.3
530 n	225 μ	2.8 n	2 m	6 m	26 m	24 k	81.2

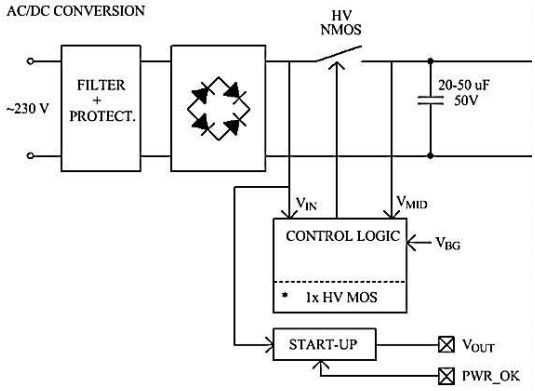

Fig. 1. Simplified blok diagram of the proposed AC/DC stage [13]

consumption of 15 mW are reported in the available documentation. These values are highly dependent on the dropper capacitor value, so while the circuit can be well optimized for a narrow output power range, its stand-by consumption largely depends on the dropper capacitor value. For the nominal output power of 0.5 W, this would result in > 200 mW of stand-by power consumption, according to the device datasheet [7]. This is a common shortcoming in dropper capacitor based solutions, as the value of the capacitor determines the input current of the device and any excess current has to be shunted, if the load current is smaller than the input current, to prevent over-voltage events. Academic research in this field was recently more focused on power factor improvement [8–12], as opposed to our focus on load load efficiency.

3 Proposed converter topology

The proposed AC/DC conversion stage topology was first presented in [13]. A brief description is also included here to improve clarity of the paper. The proposed topology is based on a synchronous rectification principle, where an energy storage capacitor is directly charged from the rectified but unfiltered AC line voltage using a high-voltage (HV) switch. The main objective of this approach is to minimize losses, thus improving the overall power efficiency. This is achieved by extending the switching period for low output power conditions, as the storage capacitor charge is depleted slowly. A simplified block diagram of the proposed converter is depicted in Fig. 1.

To implement the proposed AC/DC conversion stage, a prototype ASIC chip was designed and manufactured. During this process no technology available was capable of handling the required voltage range necessary to properly handle the AC line voltage directly. The technology chosen for the implementation is a 0.35 μm HV CMOS process with 50 V and 120 V devices available. Therefore, external HV MOS transistors are utilize as switches in the final design. The secondary switching circuit was added to the design in Fig. 1. The second (auxiliary) switch is used to control the input voltage monitoring circuitry that needs to be active only when an internal charging request is generated. This circuit functions as a quasi zero-voltage detector on the input, assuring correct charging behavior of the storage capacitor. As it is connected to the rectified AC line voltage, it contributes a large portion of the total power losses in the circuit. Thus, a switch was introduced into the sensing path, only allowing current to flow when necessary. This leads to power savings, especially at low output loads, when a charging request is generated rarely, and the converter is inactive for most of the time. A simplified block diagram of the proposed AC/DC stage is shown in Fig. 7. A detailed description of the internal building blocks of the proposed converter can be found in [14].

The final ASIC consists of:

- two HV MOS transistor switch drivers,
- low-voltage analog circuitry,
- digital control circuitry.

Both HV drivers utilize bootstrap capacitors to control the external HV NMOS transistor. They consist of a bootstrap capacitor charging circuits, level shifters, and a gate driver circuit. Both of them have separate supply voltages, enabling them to function independently and in different voltage domains. This is necessary since the two HV NMOS transistor switches operate at different voltage levels. The auxiliary sensing switch driver can also be disabled, if a continuous operation of the sensing circuit is desired.

The low-voltage (LV) analog part of the ASIC contains voltage management circuits providing the required voltage levels for the rest of the system. For this purpose, a band-gap style voltage reference is included. The reference is utilized by comparators monitoring the input and output voltages of the converter stage. The outputs of these comparators are fed to the digital control circuit for further processing and control of the HV driver stages.

The main purpose of the digital circuitry is to generate the required control signals for both HV driver circuits. An asynchronous digital circuit is utilized. This allows us to omit an oscillator circuit for clock generation, thus reducing power consumption. The digital control circuit

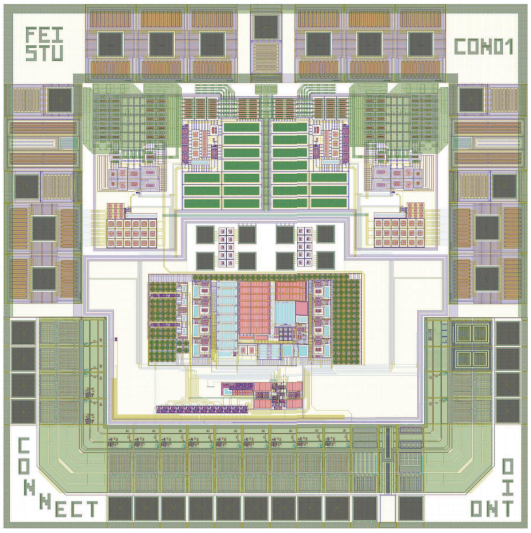

Fig. 2. Layout implementation of the AC/DC stage ASIC

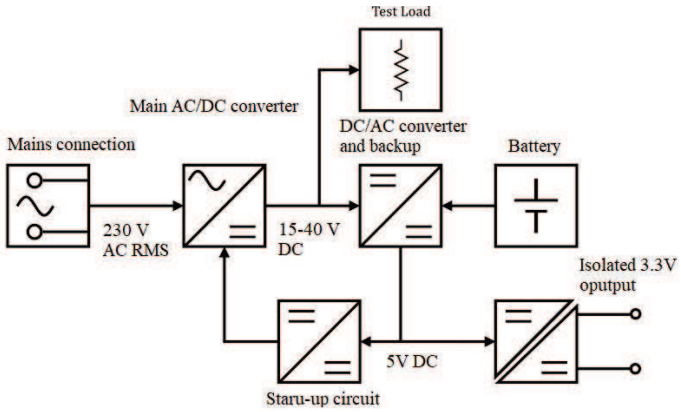

Fig. 3. Simplified block diagram of the AC/DC test module

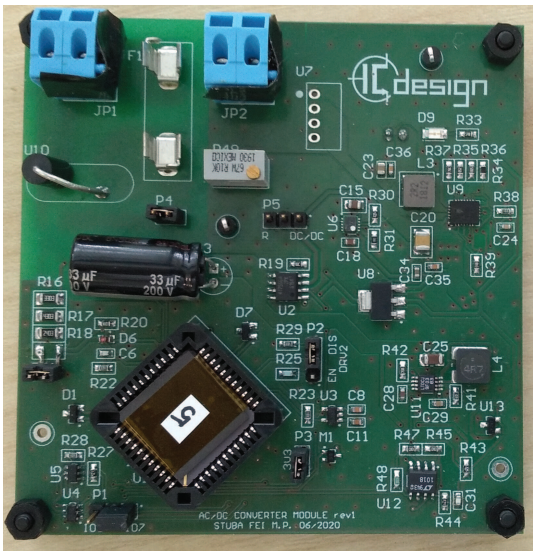

Fig. 4. Photograph of the developed AC/DC module PCB

is extended by a bidirectional input-output (IO) bus that enables monitoring and control of some internal signals. The purpose of this IO bus is mainly to ease the testing and debug phase of the digital part and is not essential for the final design of the converter.

The proposed topology was verified by transistor-level simulations in Cadence® Virtuoso® Analog Design Environment. During the design phase, each functional block was verified independently, targeting diverse circuit parameters. These simulations were also performed including parasitic elements extracted from the layout implementation. Once the design of all the building blocks was completed, verification was also performed on the top level. These simulations were focusing on functional simulations, so the AC/DC converter was configured in the intended operational mode. The overall power efficiency as well as the power consumption of the separate circuit blocks of the converter were also verified by simulations.

Table 1 shows the average power consumption figures in more detail. The total power consumption includes not only the consumption of the main blocks but also power consumption in other HV and LV parts of the circuit, leakage and various other sources of power losses. The total power consumption was evaluated assuming a scenario where both HV driver blocks are active (main and auxiliary). The final layout implementation of the converter full-custom chip is shown in Fig. 2.

4 Experimental validation

Preliminary testing of the developed ASIC was previously reported in [15]. Here, the ASIC itself was tested using a lower input voltage in order to evaluate the functionality of the prototype. During this testing, minor malfunctions in the digital control circuit were encountered, resulting in the secondary switch circuit not functioning reliably. The rest of the prototype functioned as expected, thus we moved on to the next stage of testing. The main goal of this evaluation phase was to obtain power efficiency measurements with real AC line voltage input levels.

4.1 AC/DC stage PCB module

To test the parameters of the developed AC/DC conversion stage, a PCB module with the necessary external circuitry with other specific test components was developed. It is based on the design presented in [15], which has been significantly reworked. The existing design was miniaturized, omitting the no longer necessary components previously used for the first functional testing. Significant amount of external circuitry was added in order to make the module compatible with the AC line input levels and ensure proper start-up behavior. The major circuit blocks of the developed PCB module are the following:

- developed AC/DC converter stage block,
- DC/DC conversion block with input power fail backup circuitry,

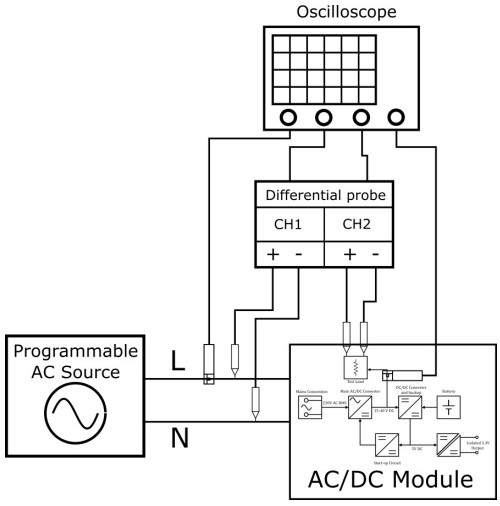

Fig. 5. Block diagram of the measurement setup

- external start-up circuitry block,
- resistive load (for test purposes),
- 3.3 V isolated output voltage converter.

A simplified block diagram of the module is shown in Fig. 3 and a photograph of the module can be seen in Fig. 4. The AC/DC stage consists of the developed ASIC, the external components necessary for the function of the AC/DC stage, and over-voltage and over-current protection on the mains interface. The internal topology of this circuit block is similar to the previously developed PCB used for functional verification of the ASIC in [15]. Some additional circuitry was necessary, to ensure proper integration with the newly developed start-up circuit. A reset signal generation circuit for the ASIC and a load enable switch circuit were added, to ensure the necessary start-up sequence is followed automatically.

The DC/DC conversion with backup circuit block has several functions. Firstly, during standard operation of the AC/DC stage, its output voltage is regulated by a DC/DC buck converter inside this block to form an internal 5 V power rail for the whole module. An additional 3.3 V rail is also provided using an LDO regulator. Secondly, if the AC/DC stage is not operating, a backup circuit powers the 5 V rail from a battery. This is mainly used during start-up of the AC/DC stage but can also provide power to the output of the module if the mains voltage were to be interrupted or significantly disturbed. A LED is used as an AC/DC stage failure state indicator, mainly for ease of functional verification.

The main function of the start-up block is to precharge the storage capacitor in the AC/DC stage and generate a reset pulse for the ASIC. This is done by the means of a boost converter, comparators, and a few logic circuits.

To provide enhanced protection as well as increased flexibility of possible types of load, an isolated DC/DC convertor was included. It is powered from the 5 V rail and provides a 3.3 V isolated output voltage rail. This could be substituted with a non-isolated solution, or omitted completely, if deemed unnecessary.

The test load is represented by a simple trimmer resistor used to easily adjust the output power of the AC/DC stage.

4.2 Test setup

A test setup for measuring the power efficiency of the proposed AC/DC stage was implemented. It is capable of measuring the input and output power of the proposed converter. The realized setup consists of:

- developed AC/DC module PCB,
- programmable AC source (Chroma 61503),
- 2-channel differential voltage probe (Metrix MTX 1032–C),
- 2-current probes (Keysight N7026A),
- 4-channel oscilloscope (Keysight DSOX 3054T).

These components were connected as shown in the block diagram in Fig. 3. This setup provides the measurement of the input/output voltage and current waveforms, allowing us to calculate the power efficiency of the developed AC/DC stage using one 4-channel oscilloscope. The programmable AC source offers the ability to test the module under various input amplitudes, and also provides galvanic isolation from the mains voltage. The differential probes are necessary to provide additional galvanic isolation between the input and output. This is needed because of the use of a bridge rectifier in the AC/DC stage itself. This does not apply to the current probes, as these utilize magnetic sensing elements and are therefore, isolated from the circuits under test.

4.3 Achieved results

Initial testing was done at a lower input voltage amplitude of 45 V. A screenshot of the oscilloscope in Fig. 7 shows the waveforms of the input/output voltages and currents: the input voltage – yellow, the output voltage – green, the input current – blue, the output current – pink. From these the input power, output power, and power efficiency was calculated. Measurements were taken for output power in the range between 25 to 614 mW. The results from this test are shown in the graph in Fig. 8.

When attempting to re-measure the power efficiency with the stardard main voltage of 230 Vrms at the input, we encountered major issues. These resulted in the developed ASIC of the AC/DC module not functioning reliably. Thus, relevant results for the full input voltage range cannot be provided. However, this issue will be addressed in the next development and prototyping run.

4.4 Discussion

Since we were unable to obtain measured efficiency values for the input voltage of 230 Vrms, the expected difference of static power loss on the input divider was added to the measured input power. The adjusted efficiency is shown in Fig. 8, and provides a more realistic result for the input voltage of 230 Vrms. The data shows

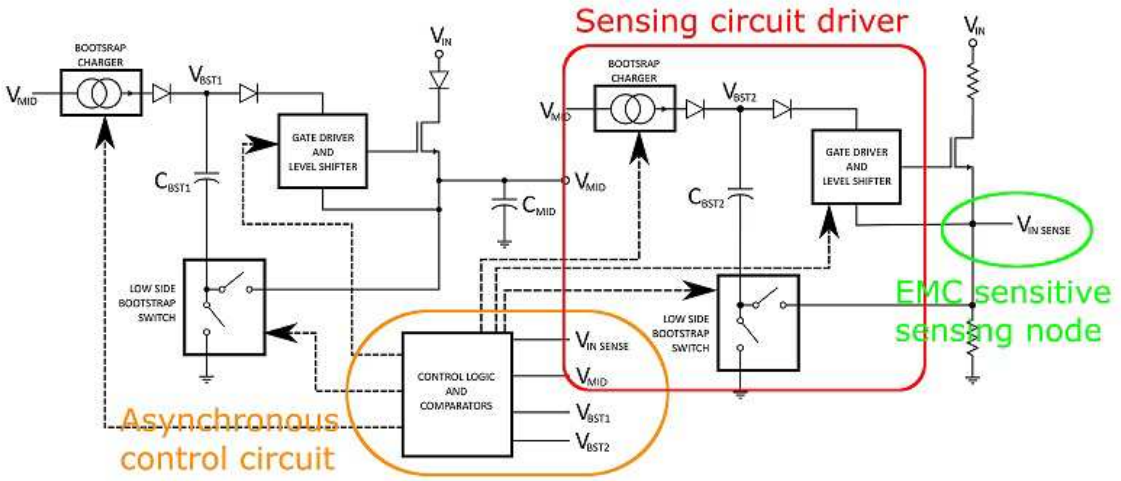

Fig. 6. Block diagram of the AC/DC stage with the main parts highlighted

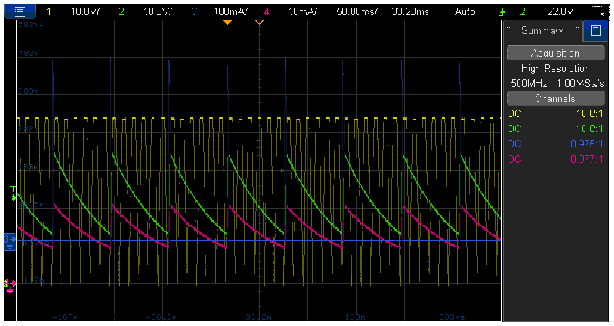

Fig. 7. Screenshot of the input and output current and voltage waveforms during measurement

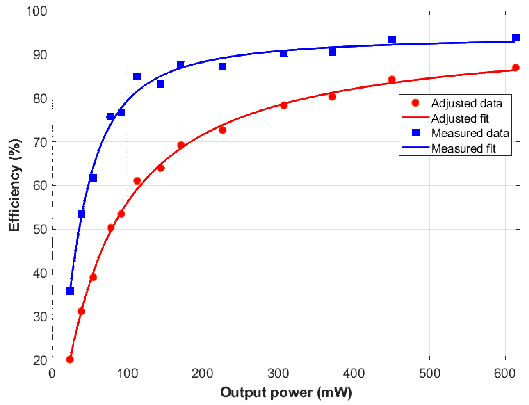

Fig. 8. Measured and adjusted power efficiency of the AC/DC converter

a decrease in the efficiency between 10–20 % compared to the measured data. This is due to previously identified malfunctions in the control circuitry (highlighted orange in Fig. 6), resulting in the input sensing circuit not being disconnected between switching cycles of the main power transistor, as discussed in Section 3. This resulted in decreased overall efficiency when compared to the simulation data in Tab. 1, where the input sensing switching circuit (highlighted red in Fig. 6) appeared functional. In this case, the overall efficiency did not drop below 80 % for output loads down to 26 mW. This suggests that if the error in the control circuit was to be corrected, the no-load power consumption of the converter would drop significantly, further improving its efficiency under low-load conditions.

As mentioned above, the malfunctions of the prototype ASIC can be attributed to the asynchronous control circuitry (highlighted orange in Fig. 6). While having the minimum power supply requirements, it did prove unreliable during testing. The first issues were detected in preliminary functional tests, when the secondary input sensing divider switch (highlighted red in Fig. 7) failed to function. Further issues were detected when the input voltage amplitude was raised, likely the result of increased EMC caused by switching noise. As the input voltage sensing node (highlighted green in Fig. 6) is high impedance to reduce power consumption, it proved sensitive to these effects. This likely resulted in the comparator connected to this node to not have a stable output value, inhibiting the main switching transistor from turning on. Attempts to remedy this issue by adding filtration capacitors to this node were not successful, as the maximum allowed capacitance in this node is limited by the increase of propagation delay in the input sensing circuitry. Further increasing the value of capacitance would result in the main switch turning on while the input voltage is too large, causing an over-voltage event and likely damaging the ASIC and any connected circuitry. To improve the reliability of the ASIC, further redesign of the control circuitry is necessary. This could be achieved by replacing the asynchronous digital part of the circuit with a more standard solution based on a fully synchronous digital controller. Some improvements in the input sensing circuit would also likely be necessary. The downside of this approach is increased power consumption, most notably caused by the addition of an oscillator to provide the clock signal for the controller.

5 Conclusion

An AC/DC conversion solution aimed at the sub 0.5 W output power domain was presented in this pa-

per. To implement the proposed converter topology, a prototype ASIC was designed and manufactured. The proposed design was first analyzed by transistor-level simulations. These simulations show a conversion power efficiency above 85 % for the output load of 500 mW, as well as a no-load power consumption below 5 mW. This shows improved properties of the proposed solution when compared to existing commercially available solutions, where efficiencies of 65–70 % are reported. For the purpose of testing, an PCB with the necessary external components was developed. This was needed as no manufacturing technology available was able of handling the AC line voltage directly. During preliminary functional testing, issues in the control circuitry began to arise. This resulted in the converter ASIC performing at lower efficiencies than anticipated by the simulations. In later stages of testing the control circuitry proved too sensitive to EMC. This resulted in unreliable operation with the full AC line voltage on the input. This is likely caused by the use of power-efficient asynchronous control proved being unreliable. This could be remedied in a future manufacturing run by substituting the existing control logic by more robust synchronous design.

Acknowledgements

This work was supported in part by the Slovak Research and Development Agency under grants APVV 19-0392 and APVV 15-0254, the Ministry of Education, Science, Research and Sport of the Slovak Republic under grant VEGA 1/0731/20, and ECSEL JU under project PROGRESSUS (Agr. No. 876868).

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Received 15 February 2021

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