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*PAPERS*

# Analysis of SMT component land pad discontinuity effect on the overall transmission line impedance in high-speed applications

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High-speed and high-frequency PCB interconnect solutions with the slightest discontinuities in the physical geometry along the microstrip transmission line can significantly degrade the integrity of the signal being transferred. This paper presents an analysis of SMT component pads and their impact on the successive transmission line impedance. During 0805, 1206 and 2512 package size SMT component pad discontinuity evaluations it was spotted, that the increasing deviation from target impedance affects the microstrip impedance segment following the discontinuity. A 25 Ω impedance offset at the SMT pad reduces the line impedance afterwards by up to 7 Ω. A 37 Ω impedance offset results in a microstrip impedance reduction by up to 15 Ω, whereas a 45 Ω impedance change leads to a reduction of successive segment impedance by up to 30 Ω. This effect is also present in multiple evenly-spaced discontinuities. But a single reference plane cut-out, which is twice as wide as the SMT component discontinuity, substantially improves the overall impedance of the transmission line, including the successive line segment impedance drop.

K e y w o r d s: SMT discontinuity, land pad discontinuity, impedance compensation, cut-out

## 1 Introduction

As signal bandwidths increase and radio frequency (RF) systems become even more widely used for data transmission, microstrip line signal integrity becomes uncompromisingly significant in printed circuit board (PCB) design [1]. When implementing high-speed or high-frequency interconnect solutions on a PCB, even the slightest discontinuities in the physical geometry along the microstrip transmission line can significantly degrade the integrity of the signal being transferred. This signal integrity degradation can be observed when various signal parameters are extracted, including additional reflections and impedance changes, loss of signal amplitude, reduction of signal rise/fall times, increased jitter, overshoots/undershoots and others. For the latter reasons, it is necessary to recognize these high-speed or RF channel discontinuities and provide ways to eliminate or mitigate their effects for better signal transmission. One of the most common causes of transmission line discontinuity is that surface mount technology (SMT) component pad widths are usually much wider than the width of the transmission line, resulting in excess shunt capacitance and causes transmission line discontinuity. These SMT components are simply necessary to match transceiver circuits with antennas, to provide common-mode suppression, DC-blocking, electrostatic discharge, short-circuit protection or other necessary engineering solutions. The latter effect influences an unwanted change of transmission line impedance. Therefore, to compensate for this unwanted impedance drop, the ground plane region under the SMT pads should be properly removed to minimize the impedance change in the signal propagation path.

In the scientific and engineering literature, there are a number of recommendations on how to deal with the reference (ground) plane in order to reduce impedance changes. For example, many engineering recommendations guidelines suggest creating a cut-out in the ground plane without specifying its width, or the same width as the pad [2], [3], [4]. There are also engineering works that indicate that the width of the cut-out of the ground plane should be a corresponding amount of mils wider than the pad [5], or making the pad of the SMT component at least three times the width of the cut-out [6].

In the scientific literature, there are a number of studies that investigate the influence of AC coupling SMT capacitor pads and cutouts under them on the change of impedance of the differential line [7], [8], [9]. These studies address ways of improving high-speed interconnects [7], analyze improvements of the digital signal eye-diagram when cut-out compensation is employed [8] and also how the shape of the cut-outs affects the impedance [9]. There are also research papers that investigate the effect of cut-out shape on impedance compensation specifically for 0201 size SMT components [10]. According to this work, the best test characteristics of the differential 85 Ω line were characterized by larger circular-outlined cut-outs. However, in this case, the cut-outs are formed under the differential pair SMT components.

This paper presents an analysis of how SMT component discontinuity pads affect the microstrip transmission line following it by providing single-pad discontinuity

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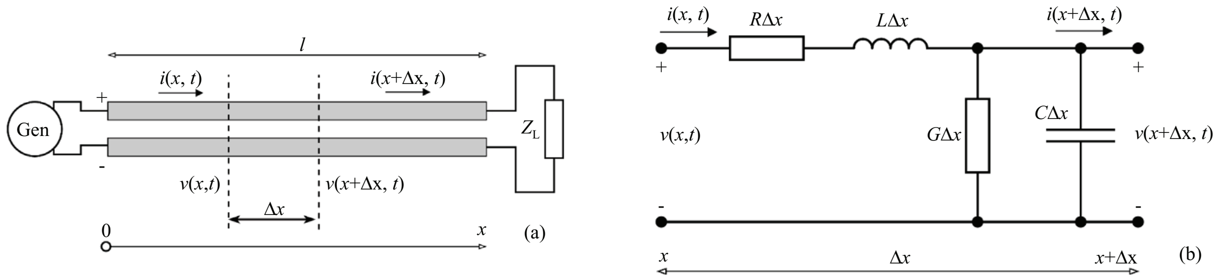


**Fig. 1.** Microstrip discontinuity: (a) – without, and (b) – with reference plane cut-out compensation

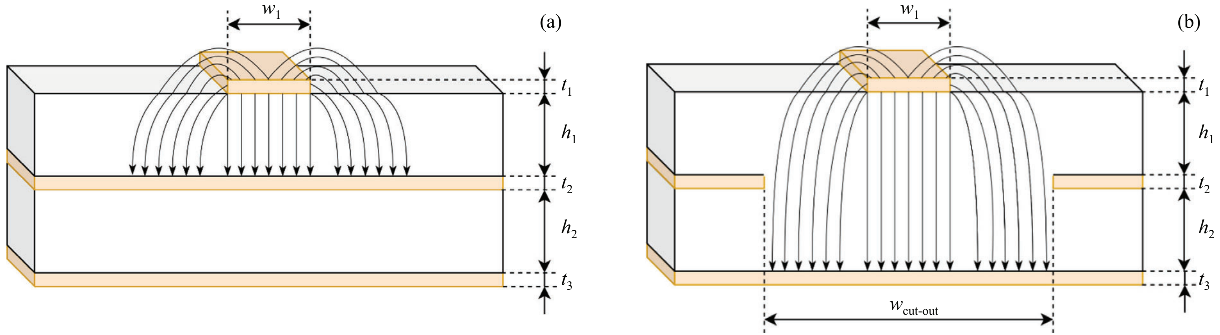


**Fig. 2.** Microstrip discontinuity: (a) – without, and (b) – with reference plane cut-out compensation

analysis as well as analyzing a practical layout containing multiple pads. This paper also compares the uncompensated discontinuity transmission line results to those with the proposed optimal reference plane cut-out.

## 2 Theoretical evaluation

Low-frequency alternating current does not require specific interconnect characteristics. Simple conductors cannot efficiently pass high-speed or RF because of signal energy losses and in order to. For these reasons transmission lines are used, which are two parallel conductors separated by a layer of dielectric material. An infinitely short segment $\Delta x$, presented in Fig. 1 (a), can be analyzed as a lumped component circuit Fig. 1 (b) containing active resistance $R$ and conductance $G$, inductance $L$ and capacitance $C$. These parameters are defined per segment length $l$. The series inductance $L$ represents the total inductance of both conductors, the parallel capacitor – total capacitance between these conductors. Resistance $R$ describes the losses in the line due to the finite conductance and conductance $G$ describes the losses due to the imperfections of the dielectric material.

In order to avoid solving Maxwell equations when describing the structure presented in Fig. 1 (a). Circuit theory analysis can be applied to Fig. 1(b) and an equation for the characteristic impedance can be found

$$\mathcal{Z}_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}} = \sqrt{\frac{L}{C}}\Bigg|_{\substack{R=0\\G=0}} . \tag{1}$$

The latter equation can be presented for a lossy transmission line, including $R$ and $G$, but as these parameters are very small, they can be neglected, resulting in a simplified equation. It should be noted, that both $L$ and $C$ are inductance and capacitance per unit length [11]. According to (1), in order to change the characteristic impedance, either unit length capacitance or inductance can be altered. When dealing with specific SMT component packages, there are restrictions on the pad size widths for a proper solder joint to occur, thus there is a limit to how much inductance can be tuned. On the other hand, multi-layer PCBs provide a possibility to change capacitance by adding a reference plane cut-out under the transmission line segment. This is presented in Fig. 2.

Reducing capacitance by means of removing a reference plane cut-out equal to the width of the segment proves to be efficient, but the more optimal approach is to have the cut-out twice as wide as the transmission line segment. By doing so, the fringing fields on both sides of the transmission line shown in Fig. 2 do not form fringe capacitance, thus increasing the impedance according to (1). It should be also noted, that in order to apply a reference plane cut-out to any trace segment, shown in Fig. 2(a), multiple stackup parameters (dielectric thicknesses $h_x$, dielectric permittivity $\epsilon_r$, trace thickness, *etc.*) have to be taken into account in order to properly compensate the impedance change as presented in Fig. 2(b). Simply applying a reference plane cut-out as a rule of thumb without taking into account the stackup details might lead to overcompensation, which might not be crucial if the resulting absolute deviation from the target impedance is smaller than that without applying the cut-out compensation [12].

| Layer | Description |
|---|---|
| Top layer 1 | Copper, thickness 35 µm |
| Prepreg | Material 7628, thickness 210.4 µm, dielectric con. 4.6 |
| Inner layer 2 | Copper, thickness 15.2 µm |
| Core | Material 7628, thickness 400 µm, dielectric con. 4.6 |
| Inner layer 3 | Copper, thickness 15.2 µm |
| Prepreg | Material 7628, thickness 210.4 µm, dielectric con. 4.6 |
| Bottom layer 4 | Copper, thickness 35 µm |

**Fig. 3.** Standard 1 mm 4-layer PCB stackup and thickness for JLC7628 configuration provided by JLCPCB company

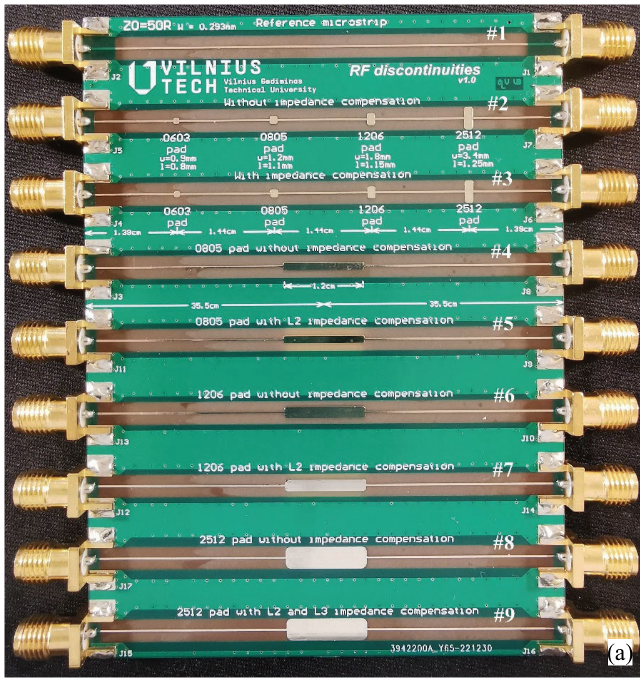


**Fig. 4.** Fabricated DUT board

### 3 Test-bench and measurement results

As previously mentioned, the device under test (DUT) has to be a multi-layer PCB with separate transmission line segments. In order to control trace segment capacitance, a known stackup with properly described layer thicknesses and PCB laminates has to be applied. The one used in the design of the PCB is presented in detail in Fig. 3.

The fabricated DUT PCB is presented in Fig. 4. Each micro-strip line is marked with a number that corresponds to a certain situation. A total of 9 different microstrip lines are implemented on this DUT PCB. For example, 1 corresponds to the reference 50 Ω line, 2 and 3 respectively correspond to the line with different SMT component contact pads, 4 and 5 respectively correspond to the contact pads width of the 0603 component with and without cut-out compensation, 6 and 7 – the 0805 SMT component with and without compensation, 8 and 9 - 1206 SMT component with and without compensation respectively. It should be noted that these contact pads are made 12 mm long, so that with a 58 ps rise time resolution VNA, it is possible to accurately determine the impedance of such a contact pad. The width of the pads, on the other hand, is standard to the mentioned SMT component land pad recommendations. Measurements and experimental analysis were performed using a calibrated 8.5 GHz bandwidth LA19-1304B VNA. The fabricated DUT PCB was connected directly to the VNA, avoiding the use of additional cables that introduce additional insertion losses and possible reflections.

Figure 5 presents TDR measurement results for different DUT sections. All graphs are organized in the same way, where the dashed line is the reference line 1 impedance compared to the red line of the uncompensated pad impedance and the green line where the pad had a reference plane cut-out compensation with a width of twice as large as the pad width. Figure 5, (a), (b) and (c) depict 0805, 1206 and 2512 package-size SMT component responses respectively. All three cases show a deviation from the reference transmission line impedance from 30 Ω to almost 45 Ω without compensation. According to Fig. 5(a) and (b), a single reference plane cut-out under the discontinuity which is twice its width either almost eliminates the impedance mismatch. As for the wide pad in Fig. 5(c), the impedance drop is reduced in half when using a single reference plane cut-out. This is because the capacitance of such a large pad has to drop even more, hence this could be done by introducing another reference plane cutout in the successive layer below [12]. Moreover, even though the length of the discussed discontinuities is around 17% of the length of the whole 50 Ω microstrip transmission line, the introduced reflections affect and worsen the impedance the segment of the line following it. This can be clearly depicted in the TDR response from 0.8 ns to 1 ns. In both cases, the 50 Ω microstrip transmission line following the discontinuity changes impedance by up to 50% of the target and acts as if it is mismatched. This is shown in the hatched area of each TDR response. This can also be spotted in TDR measurements, presented in other works [13] [14]. This effect is important to understand while analyzing the TDR response presented in Fig. 5(d). It corresponds to a practical topology design situation, where multiple different size components form an RF path and multiple discontinuities occur. The components have been removed from this chain for the cleanliness or this experiment and to avoid unwanted resonances which can occur due to component main parameter (ex. the capacitance of a capacitor or inductance of an inductor) value along with parasitic parameters of SMT packages. The distance of each successive SMT pad is the same and equal to 1.44 cm, but observing the peaks, they are spread out unevenly.

The theoretical time delay, corresponding to the mentioned distance is 0.17 ns, but the spread of minimums in the uncompensated TDR plot in Fig. 5(d) increases from 0.18 ns by 0.1 ns. Introducing reference plane cut-out, which is twice as wide as the SMT component discontinuity, a mismatch at the discontinuity still occurs, but the compensation mitigates any further transmission line impedance degradation. $S$ parameter measurements for

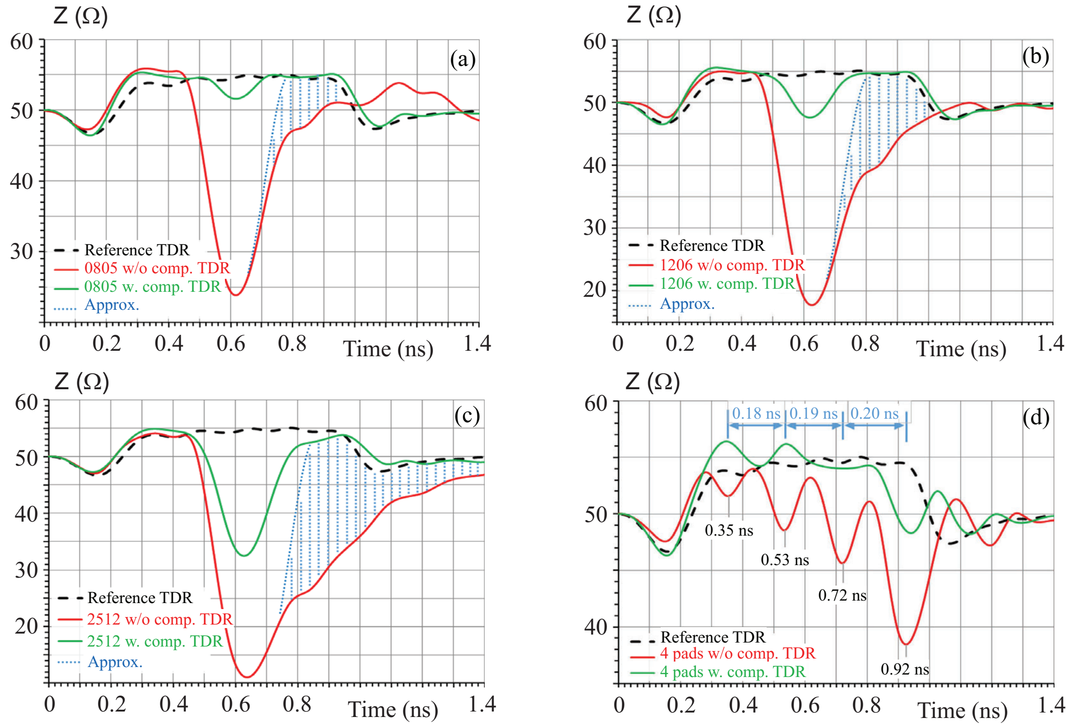


**Fig. 5.** Fabricated DUT board TDR measurement results: (a) – 0805 size SMT pad TDR plot, (b) – 1206 size SMT pad TDR plot, (c) – 2512 size SMT pad TDR plot, (d) – TDR plot for a transmission line with multiple SMT pads

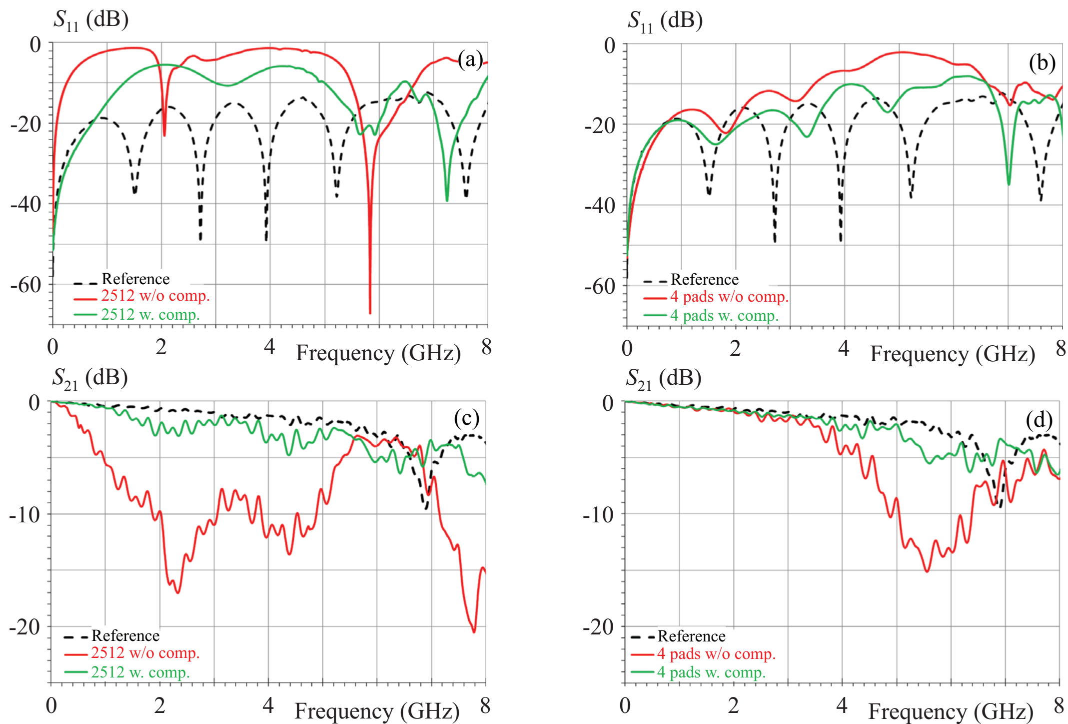


**Fig. 6.** Fabricated DUT board $S$-parameter measurement results: (a) – $S_{11}$ of 2512 size SMT pad, (b) – $S_{11}$ of a transmission line with multiple SMT pads; (c) – $S_{21}$ of 2512 size SMT pad, (d) – $S_{21}$ of a transmission line with multiple SMT pad

2512 size SMT pad and a transmission line with multiple pads are shown in Fig. 6. Dashed curves represent reference microstrip line with no discontinuity reflection coefficient $S_{11}$ and transfer coefficient $S_{21}$ measurement results, whereas red and green curves present the non-compensated and compensated microstrip structure measurement results accordingly. Only the 2512 pad scattering parameters are presented in order not to overwhelm

the plots, taking into account, that the tendencies are the same for all cases.

Analyzing the reflection coefficient $S_{11}$ measurement results, presented in Fig. 6(a) and (b), it can be concluded, that the introducing compensation to the pad reduces signal reflections over the whole 8 GHz frequency span by at least 5 dB. Transfer coefficient $S_{21}$ measurement results show, that when compensated, even a transmission line with a component requiring a large soldering pad losses differ from the reference by up to 3 dB.

## 4 Conclusion

This paper presents an analysis of the SMT component land pad discontinuity effect on the overall transmission line impedance in high-speed applications. As a result of this analysis, it was spotted that each successive discontinuity affects the impedance of the line which follows it and the bigger the deviation from the target impedance is, the more the line gets mismatched. During 0805, 1206 and 2512 package size SMT component pad discontinuity evaluations it was spotted, that the increasing deviation from target impedance affects the microstrip impedance segment following the discontinuity. When the discontinuity makes up 17% of the length of the whole $50\,\Omega$ microstrip transmission line, a $25\,\Omega$ impedance offset at the SMT pad reduces the line impedance afterwards by up to $7\,\Omega$. A $37\,\Omega$ impedance offset results in a microstrip impedance reduction by up to $15\,\Omega$, whereas a $45\,\Omega$ impedance change leads to a reduction of successive segment impedance by up to $30\,\Omega$. This effect is also present in multiple evenly-spaced discontinuities, where the TDR minimums are shifted successively by 0.1 ns. But a single reference plane cut-out, which is twice as wide as the SMT component discontinuity, substantially improves the overall impedance of the transmission line, including the successive line segment impedance drop. S-parameter measurements also confirmed improvements in compensated transmission line parameters up to 8 GHz. Even if it is not enough to fully compensate the discontinuity, this type of compensation is still beneficial as it mitigates any further transmission line impedance degradation due to successive SMT pad occurrence.

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