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PAPERS

Automatic test-bench for SiC power devices using LabVIEW

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This paper is devoted to the improvement existing models of electronics devices, which are used in powers electronics as switching devices, and investigate a LabVIEW-based automatic test-bench for Silicon carbide (SiC) power devices. In recent years, power electronic devices are required to be capable handle with higher voltage, leads to development of new generation of power electronic devices, such as SiC devices. However, using a simulation platform, such as Spice, to diminish the complexity of power electronic design with these new devices is hindered by the lack of precise models. The proposed test-bench enables not only measuring static characteristics of SiC power devices, but also extracting key parameters required by simulations. These extracted parameters are then employed in the existing device model, and the simulation results which are based on the model with original parameters and models with extracted parameters are compared with measured results. The comparison clearly demonstrates that parameters obtained from the proposed test-bench significantly enhance the Spice model.

Keywords: power electronic devices, SiC, LabVIEW, PSpice, Spice model

1 Introduction

Recent advancements in semiconductor technology and microelectronics and significant expansion of electric propulsion applications have spurred interest in power electronics, leading to requirement of improving features of controllers, and enhancing device load-bearing capabilities, such as higher operating voltage and temperature, and higher switching frequency. For instance, the electrical systems in modern transport applications including automotive, rail transport, or aircraft power systems all expect power electronic systems capable of handling high power levels (up to megawatt). As a result, the operating voltage level must be sufficiently high to minimize current levels. Further requirements for these systems are achieving the highest possible efficiencies. These requirements and expectations lead to the necessary development of a new generation of power electronic devices [1-5].

Conventional silicon-based (Si-based) electronic devices, however, face limitations of not only operating voltage but also switching frequency, operating temperature, and other factors. In detail, Si-based MOSFETs excel in high-frequency switching (up to MHz) but have lower blocking voltage (some hundreds of Volts). By contrast, Si-based IGBTs can operate with high voltage (up to kV), but their switching frequency is limited to a few tens of kHz due to the bipolar current conduction mechanism. In general, increasing switching frequency improves power density and minifies converter size, but increases switching losses. Another loss contribution in power electronic converters is conduction loss, which dependent on state-on drop voltage of switching devices. Electronic devices in switch mode converters, hence, must be able to operate at high frequencies and have low state-on voltage drops to achieve optimal performance [3-6].

Regarding the power electronics' evolution to obtain higher power density and lower loss, using new wide bandgap (WBG) semiconductor materials, such as silicon carbide (SiC), or gallium nitride (GaN), become a promising solution. For instance, SiC MOSFETs provide fast switching speed (due to the voltage-controlled mechanism), low drop voltage (due to small on-state resistance), low switching losses and high operating voltage (due to wide bandgap property of SiC). Moreover, SiC not only enables operation at more elevated temperatures (property of WBG materials), but also has higher thermal conductivity compared to Si (up to 2-3 times). These advantages contribute to a reduction in the physical size of converters [1-7].

The complexity of power electronic design and electronic circuit design in general requires of using simulation platforms, such as Spice-based simulation. A crucial factor in enhancing the conformity of simulation outcomes with actual behaviour is the accuracy of used models [8-12]. Practically, there exist

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issues of lacking precise models for electronic devices. Models of new SiC electronic devices are even not always available in all cases. The aim of this study, therefore, is to design an automatic test-bench to evaluate the characteristics of SiC power devices and extract parameters for creating or improving the Spice model of these devices. A subcircuit equivalent model of MOSFET using in Spice-based simulations can be seen in Fig. 1.

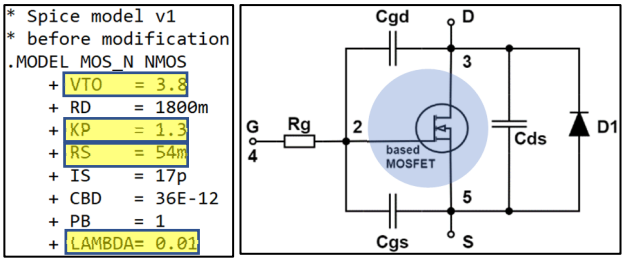


Fig. 1. Spice subcircuit model of MOSFET

As shown in Fig. 1, in Spice-based simulations, an actual MOSFET is modelled by an ideal-based MOSFET with parasitic components. Figure 1 also highlights main parameters of the ideal-based MOSFET and puts emphasis on extracted parameters. This paper solely addresses the measurement static characteristics of SiC MOSFETs and extraction of parameters for Spice static (DC) analysis. These parameters principally are parameters of based MOSFET, such as threshold voltage, source resistance, channel-length modulation coefficient, transconductance coefficient. Other parameters of the MOSFET Spice model in Fig. 1, such as C_{gd}, C_{gs}, C_{ds}, etc are devoted to the dynamic behaviour of devices, but considering the scope of this article, we focused mainly on static parameters.

2 Test-bench design for MOSFET measurement

2.1 Design of test-bench

This paper presents the design of a LabVIEW-based test-bench for measuring static characteristics of SiC MOSFETs. The test-bench comprises two variable DC voltage sources, two voltmeters, and an amperemeter. The variable DC voltage sources are used to set the voltages between transistor's gate and source (V_{GS}) and between transistor's drain and source (V_{DS}). The voltmeters are connected in parallel to voltage sources to measure the actual values of V_{GS} and V_{DS}, and the amperemeter measures the MOSFET's drain current I_D.

These discrete instruments can be substituted with source measurement units (SMUs), which integrate sourcing and measurement functions within the same instrument's terminals. The simplified circuit diagram of SMU consisting of a DC voltage source, voltmeter, and amperemeter is illustrated in Fig. 2. It is also crucial that the amperemeter of SMU 1 is not employed for measurement because of the neglect of the MOSFET gate current.

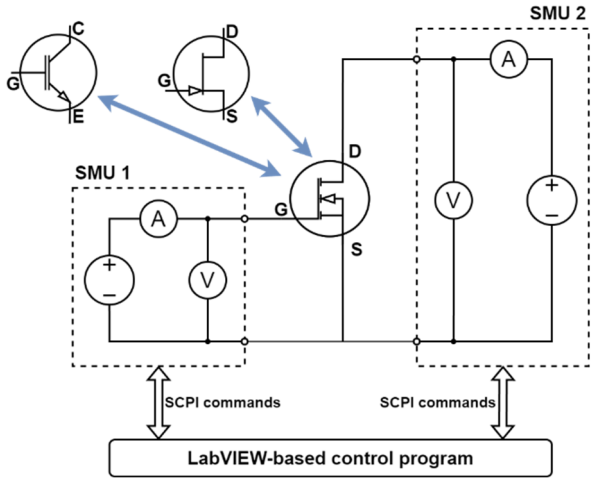


Fig. 2. Test circuit for measuring static *I-V* characteristics of MOSFET using SMUs

Figure 2 also shows that the test circuit can be used for measuring static characteristics of other power electronic devices such as IGBT, JFET, etc. The proposed test bench, therefore, is flexible to measure various devices. However, as mentioned above, this paper will focus on the system for MOSFET measuring and parameter extraction. Similar systems for other devices can be built based on the same principle, and only by changing mathematical blocks appropriate to mathematical models of measured devices.

2.2 Description of measurement process

The process of measuring static characteristics of SiC MOSFET is shown in Fig. 3. Firstly, the output voltages of SMUs are set equal to minimum values. After stabilization of SMUs' output voltages, the actual values of V_{DS}, V_{GS} and I_D are measured. To eliminate the measurement statistical uncertainty, these values are measured multiple times to calculate the average values, as well as the statistical uncertainty of measurement.

As can be seen in Fig. 3, before performing measurement and parameter calculation, the proposed test-bench allows selecting measured device to set suitable mathematical models. The mathematical model will be used to extract device's parameter. In this paper, a power MOSFET is used to verified approach, and functionality of the proposed test-bench. Detailed description of MOSFET mathematical models and parameter extraction will be discussed in the next part of this chapter.

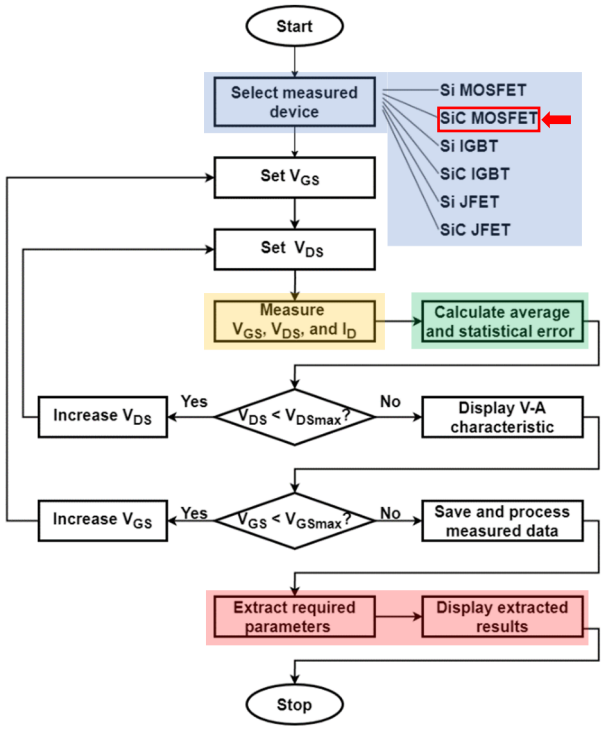


Fig. 3. Flowchart diagram of measuring static *I-V* characteristics of SiC MOSFET

In subsequent steps, the set value of V_{DS} (output voltage of SMU 2 in Fig. 2) is increased if it remains smaller than V_{DSmax}. The V_{DS} increment is pre-assigned prior to the measurement process. At each operating point, the actual values of V_{DS}, V_{GS}, and I_D are measured. In the flowchart shown in Fig. 3, the measurement of device's operating points is mark in yellow. As mentioned above, the measurement will be repeated more times to eliminate statistical uncertainty. The measurement uncertainty is also addressed by the test-bench, as marked in green colour in Fig. 3. The measurement uncertainty of each operating pointing is calculated according to the number of measurement repetitions, used instruments, measurement range, etc. Detailed discussion about the measurement process, as well as measurement uncertainty classification and calculation will be presented in Section 3. The outcome of this process is the static output characteristic of the SiC MOSFET at a certain V_{GS} value.

Similarly, the set value of V_{GS} (output voltage of SMU 1 in Fig. 2) is increased until it reaches or exceeds V_{GSmax}. The increment of V_{GS} is also assigned before the measurement process. At each value of V_{GS}, these preceding steps are repeated to obtain the static output characteristics of the SiC MOSFET at required V_{GS} values. Based on the values of V_{GS} and I_D, the static transfer characteristic of MOSFET is also acquired.

As mentioned above, the proposed test-bench is designed with the capability to automatically calculate the required electric parameters of measured device from measured results based on device's mathematical models. In Fig. 3, the red colour marks steps of calculating and displaying device's parameters. In this paper, mathematical model and parameter of power MOSFET is discussed. Employing the LabVIEW-based mathematical operations, crucial MOSFET parameters can be extracted immediately following the measurement process. The assembly of LabVIEW mathematical blocks to calculate MOSFET parameters will be presented in the next chapter. For additional processing, the complete set of measured results is also preserved for future analysis at the conclusion of the measurement procedure.

2.3 MOSFET parameters extraction

As mentioned above, the LabVIEW-based program was developed with the function of automatically extracting the required electric parameters, which are important for modelling and applying SiC MOSFET. These extracted parameters are expected to precise the Spice model of the measured SiC MOSFET.

The most fundamental and important electric parameter in MOSFET modelling is threshold voltage V_{TH}. Among the numerous approaches, the most preferred method for defining this parameter is the level of V_{GS} at which MOSFET operations transit between strong and weak inversion[12-15]. A variety of methods have been proposed for extracting V_{TH} based on the static transfer characteristics of MOSFET. Comprehensive reviews and comparisons of these methods have been presented in [13-17].

The LabVIEW-based test bench presented in this paper uses the linear extrapolation method in both linear and saturation operating regions, which is the most popular method to extract V_{TH} [14]. The basis of this method are simplified MOSFET equations in the linear region – Eqn. (1), and in the saturation region – Eqn. (2). It is obvious that in the linear region, the static output characteristic $I_D(V_{GS})$ at a certain V_{DS} forms straight line that intersects the V_{GS} axis at the point $V_{TH} + \frac{V_{DS}}{2}$. By locating this intersection, the threshold voltage value can be easily calculated. In the saturation region, it is necessary to use the characteristic $\sqrt{I_D}(V_{GS})$. The intersection between this characteristic and $I_D^{1/2}$ axis then directly determines the threshold voltage [12-17].

$$I_{D,lin} = K_P \cdot \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) \cdot V_{DS} \qquad (1)$$

$$I_{D,sat} = \frac{K_P}{2} \cdot \frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (2)$$

As evident from these equations, the transconductance coefficient K_P of MOSFET can be also extracted using the acquired static transfer characteristics, with the known W/L ratio. Furthermore, the $\sqrt{I_D}(V_{GS})$ characteristic in saturation can be considered as a straight line while neglecting the effect of MOSFET source resistance R_S. In fact, the $\sqrt{I_D}(V_{GS})$ characteristic is not a straight line but curved at high current levels. By calculating the departure between measured curve and calculated straight line, it is capable of extracting the R_S value [16-19].

Moreover, both simplified equations neglect the channel-length modulation. The effect of channel-length modulation can be presented by coefficient λ, the MOSFET equation in saturation region then is modified to Eqn. (3). Coefficient λ can be extracted by finding the intersection V_A of the extrapolated static output characteristic $I_D(V_{DS})$ with V_{DS} axis. The relationship between λ and V_A is given in Eqn. (4).

$$I_{D,sat} = \frac{K_P}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}) \qquad (3)$$

$$1 + \lambda \cdot V_A = 0, or\ \lambda = \frac{-1}{V_A} \qquad (4)$$

Another principal parameter, especially in the case of power MOSFETs, as discussed above, is the drain-source on-resistance $R_{DS\text{-}ON}$ which decides the power loss when MOSFET functions as a switch. This resistance is obtained using the static output characteristic of MOSFET in the linear operating region. The slope of the characteristic's tangent line in this region can be considered as the $R_{DS\text{-}ON}$ value at a specific V_{GS} value [12,18,19]. To bias the MOSFET to operate in the linear region, V_{DS} values below 50 mV are usually used. In this paper, the V_{DS} values below 20 mV are applied to the MOSFET to measure the static characteristics in the linear region.

3 LabVIEW program design

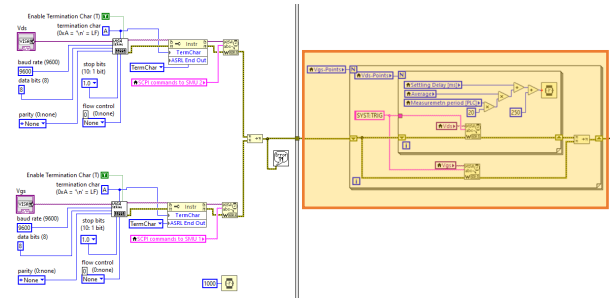
The designed LabVIEW program is structured into two main modules. The first one is the measurement module, which drives the connected instruments to conduct measurements aligned with the methodology outlined in Fig. 3. The measured data is stored in the instruments' buffer. The second module, named the processing module, is responsible for acquiring measured results, computing average value and statical uncertainty of measurement, as well as visualizing these data. This module is also in charge of extracting the required MOSFET parameters, such as V_{TH}, K_P, and $R_{DS\text{-}ON}$, as specified in Section 2.3.

3.1 Design of the measurement module

The measurement module is designed to send to the connected instruments SCPI commands, which are used for both configuring these instruments and triggering them to perform measurements. Primary configuration parameters, including maximum and minimum sweep voltages, the number of sweep steps and the number of measurements carried out in each step for averaging among others, are user-defined values input through the graphical user interface (front panel). These parameters are then converted into strings and concatenated into SCPI commands for each instrument.

After properly configuring connected instruments, the main measurement process commences. As presented in Fig. 3, the main measurement process contains two loops for sweeping V_{DS} and V_{GS} values. In each loop, the connected instruments are activated to set appropriate output voltages and conduct measurements by SCPI command. After triggering instruments, the test bench is held back for an appropriate period to enable instruments to perform the measurements. The measurement time is also shortened in this stage by parallelizing the independent process.

In particular, in the case shown in Fig. 4, two SMUs are simultaneously triggered. The hold-back period is calculated based on the settling time of output voltage, the number of averaging samples, and integration time.



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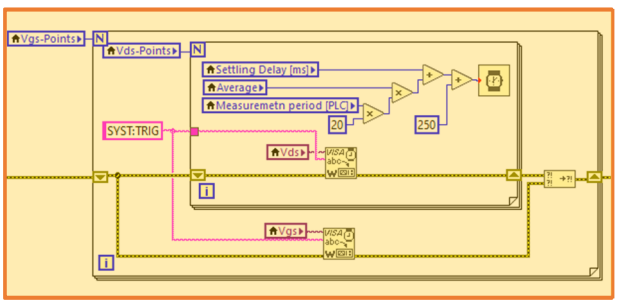


b)

Fig. 4. Block diagram of measurement module

It is important to state here that the number of samples for averaging, and integration time are important parameters from the perspective of measurement uncertainty. Generally speaking, the larger the values of these parameters are, the higher the measurement accuracy is. On the other hand, higher values of these parameters take a longer time to perform measurement. Therefore, the selection of these parameters is a compromise between measurement accuracy and measurement time.

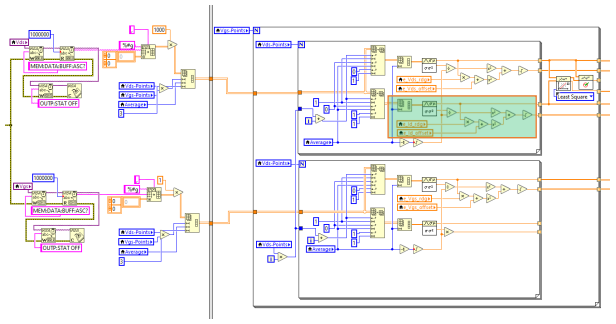
3.2 Design of the data processing module

The tasks performed by data processing block can be classified into 4 main tasks:

- Data acquisition
- Data saving
- Parameter extraction
- Data visualization

The data acquisition block is responsible for acquiring measured results saved in instruments' buffers, converting them into proper data formats, and calculating measurement uncertainties. The block diagram of the data acquisition block is shown in Fig. 5. Measurement uncertainty calculations using mathematics block in LabVIEW are also presented, using drain current I_D as an example. Measurement uncertainty can be categorized into two main types – type A uncertainty (u_A) and type B uncertainty (u_B). The total uncertainty is then calculated using relation showed in Eqn. (5).

$$u = \sqrt{u_A^2 + u_B^2} \tag{5}$$



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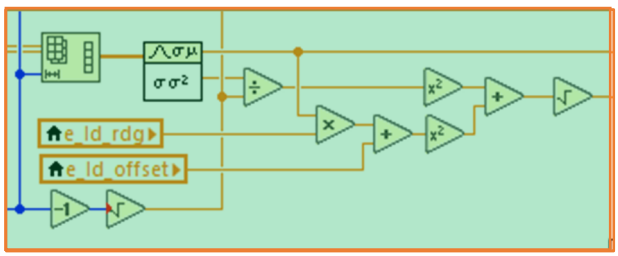


b)

Fig. 5. Block diagram of data acquisition block

Type A uncertainty is calculated as a statistical analysis of repeated measurement using Eqn. (6), where n is the number of measurement repetitions, X_k is measurement results in individual measurements, $\overline{X}$ is averaging, σ is standard deviation of measurement results set, and k_s is expansion coefficient. The value of coefficient k_s is dependent on the number of measurement repetitions n. Generally, k_s assumes values larger than 1 when n is smaller than 10 and takes the value of 1 in other cases.

$$u_A = k_s \cdot \sqrt{\frac{1}{n(n-1)} \cdot \sum_{k=1}^{n} \left(X_k - \overline{X}\right)^2} = \frac{k_s \cdot \sigma}{\sqrt{n-1}} \tag{6}$$

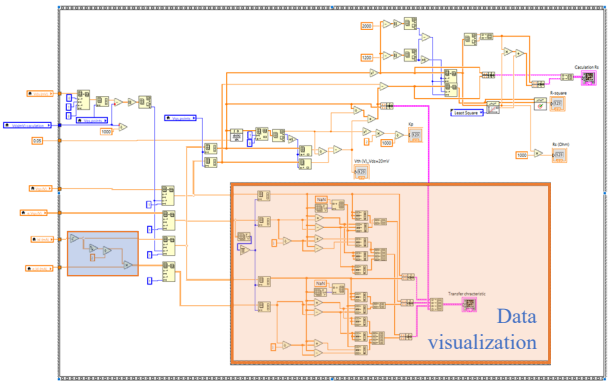
Type B uncertainty can be considered as inaccuracy of instruments, which is usually presented as percentages of reading value and measurement range. Equation (7) summarizes the most commonly used forms of this inaccuracy, where δ_M gives the percentage of reading value X_M, and δ_{MR} gives percentage of measurement range X_R. In the case of constant measurement range, the percentage of measurement range remains constant and can be expressed as measurement offset ε.

$$u_B = \delta_M \cdot X_M + \delta_R \cdot X_R = \delta_M \cdot X_M + \varepsilon \tag{7}$$

Values of these coefficients ($\delta_M, \delta_R, \varepsilon$) are dependent on several factors, including measurement range, integration time, warm-up time, and calibration among others. These coefficients are usually provided by the manufacture. In Fig. 5b, coefficients δ_M and ε are presented by local variables *e_Id_reading* and *e_Id_bias*. Values of these variables are assigned based on selected measurement ranges.

Data saving block then oversees the preservation of these acquired measured results and calculated uncertainties to a computer for further processing and analyses. Figure 6 shows a block diagram of extracting MOSFET threshold voltage V_{TH}, transconductance coefficient K_P, and source resistance R_S using measured results in saturation region, using relations in Eqn. (2). Here, one can also see the block of calculation uncertainty $u_{\sqrt{I_D}}$ of $\sqrt{I_D}$, using relation shown in Eqn. (8).

$$u_{\sqrt{I_D}} = \frac{\delta\sqrt{I_D}}{\delta I_D} \cdot u_{I_D} = \frac{1}{2} \cdot \frac{u_{I_D}}{\sqrt{I_D}} \tag{8}$$



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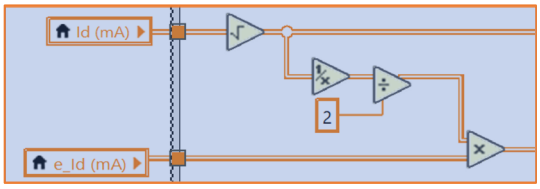


b)

Fig. 6. Block diagram of parameter extraction block

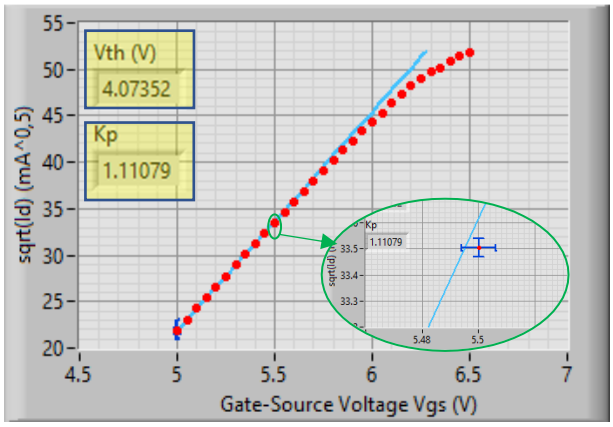
The data visualization block is responsible for creating visual representations of measured and calculated results. Measured results are depicted in the form of static MOSFET output and transfer characteristics, with the calculated uncertainty of measurement, as shown in Figs. 7 and 8.

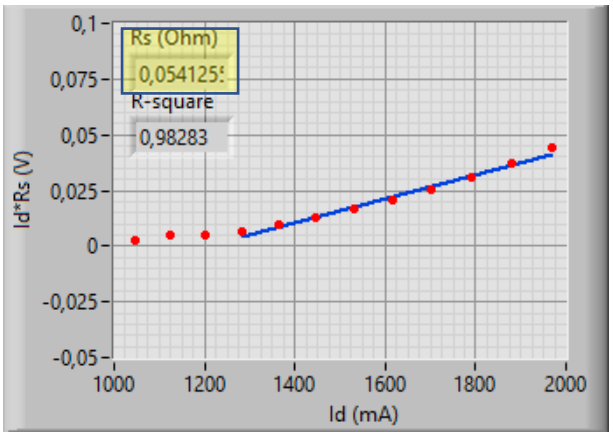
4 Verification of LabVIEW-based system design

4.1 System design verification

A power MOSFET is used to functionally verify the proposed test bench. MOSFET measurement and parameter extraction in the saturation region are performed. Based on the measurement results in saturation region, parameters V_{TH}, K_P, R_S, and λ are extracted. The obtained results are presented in Fig. 7.

MOSFET is also measured in the linear region. Measured results are then processed to extract parameters V_{TH}, and the dependence of $R_{DS\text{-}ON}$ on V_{GS}. The results of measurement and extraction process are shown in Fig. 8. It is evident that the measured results are consistent with theoretical equations. However, it is important to state here that the extracted value of MOSFET threshold voltage using measured results in saturation region is larger than using measured results in linear region. These values, therefore, are needed to compare by applying to Spice model for using in simulation. Detailed comparison and discussion is presented in the next part.





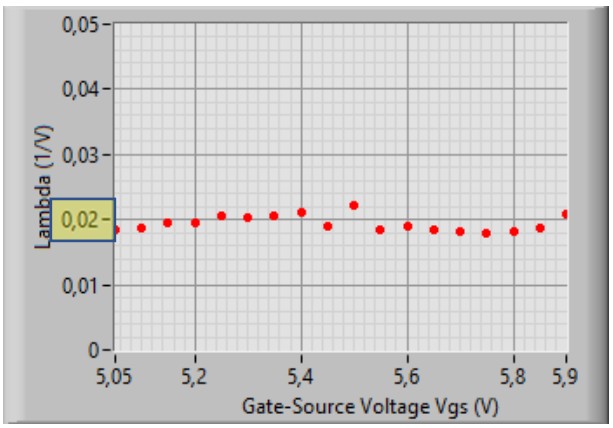


Fig. 7. Measured and extracted results – saturation region

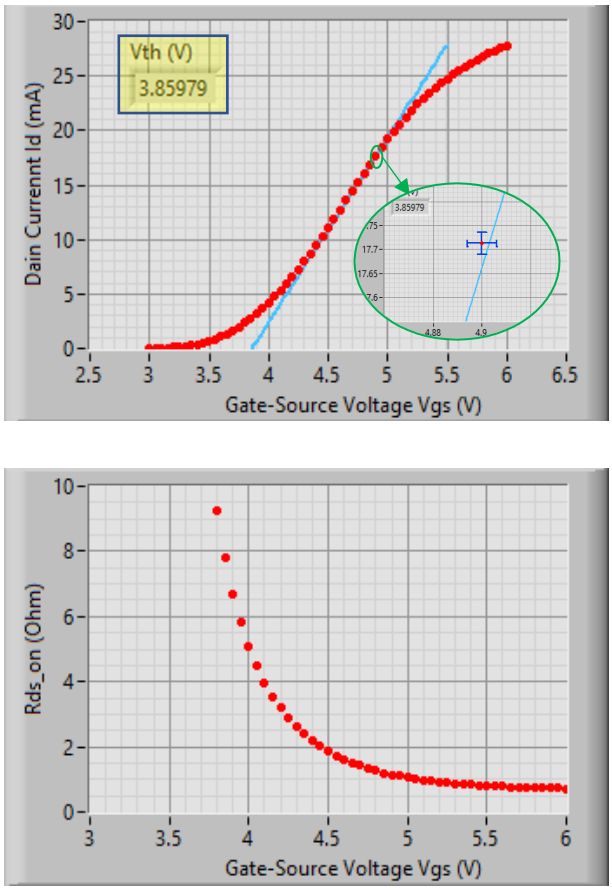


Fig. 8. Measured and extracted results – linear region

4.2 Result discussion

The extracted results from measurement in saturation and linear regions are used to verify and modify the Spice model. The original and modified models are put into simulation to compare the similarities between simulated and measured results. Comparisons are shown in Fig. 9. It is obvious that the modified model exhibits a closer correspondence to measured results. The value of R_S in the original model can be deemed as suitable value. The most modified parameters in this case are threshold voltage V_{TH} and transconductance coefficient K_P. The original model is proposed with an excessively large value of K_P, leading to an overly elevated I_D saturation level, in comparison with measured results. Moreover, the original V_{TH}, is too low, causing the simulated value of $V_{DS,sat}$ to be higher than the measured value, as can be seen in Fig. 9.

As discussed previously, it can be seen that the extracted value of threshold voltage based on measurement in the linear region is still too small to accurately reflect the measured results. The dependence of $R_{DS\text{-}ON}$ on V_{GS} is also calculated. It is discernible that extracted values of $R_{DS\text{-}ON}$, when MOSFET is open, are in order of a few Ohms, which is in accordance with common values of power MOSFET in practice.

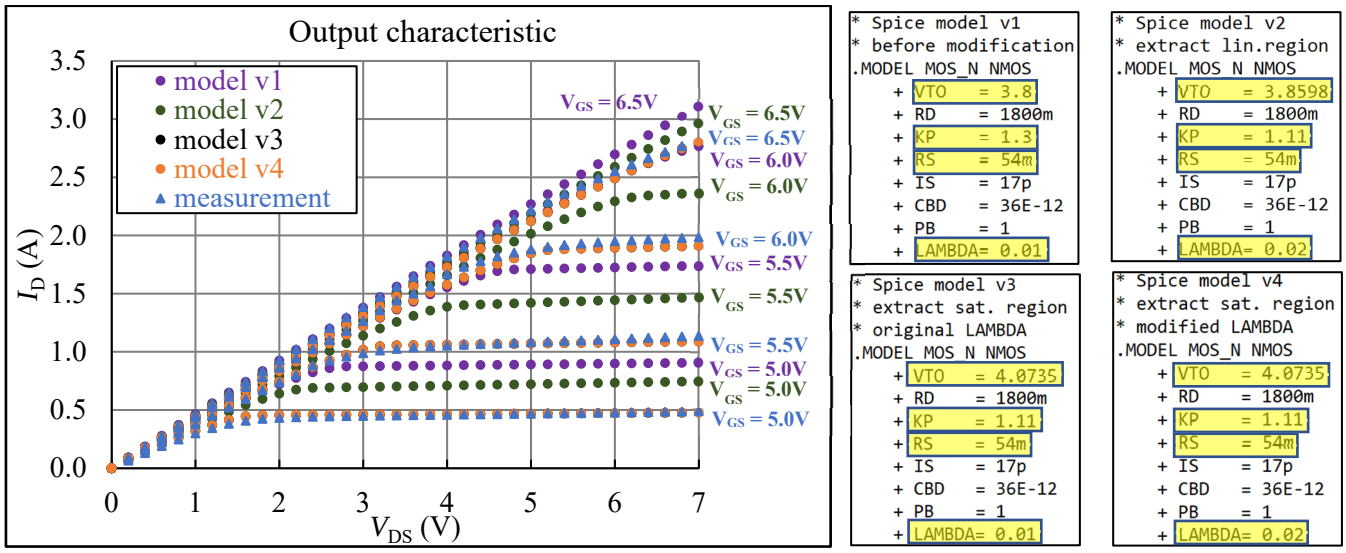


Fig. 9. Modification of Spice model

The effect of λ is not clearly visible in Fig 9, as the characteristics of the model with the original λ value (model v3) and the model with the modified one (model v4) are very similar, and it is difficult to qualitatively compare. To effectively compare simulated models, a quantitative comparison of these models is carried out by relative root mean square error (RRMSE) of MOSFET drain current. The formula used for RRMSE calculation is presented in Eqn. (9). The calculated values of RRMSE are shown in Table 1. It is apparent that Spice models with extracted parameters are more in line with measured results, the RRMSE value can be

significantly improved by using extracted values of the main parameters. The effect of λ value can be also clearly seen. The model with extracted λ value has a better fit to the measured results better. As discussed earlier, it is noticeable here that the threshold voltage value extracted from measurement in the saturation region matches the actual value better.

$$RRMSE = \sqrt{\frac{1}{N} \cdot \frac{\sum_{i=1}^{N} \left(I_{D,sim} - I_{D,meas}\right)^2}{\sum_{i=1}^{N} \left(I_{D,meas}\right)^2}} \qquad (9)$$

Table 1. RRMSE of Spice models

Spice model	v1	v2	v3	v4
RRMSE	0.0216	0.0125	0.0028	0.0025

5 Conclusion

This paper presents a test-bench for measuring static characteristics of SiC power devices to automatically calculate fundamental parameters for the creation (or improvement) Spice models of measured devices. Measurement of a power MOSFET is performed to verify the proposed test-bench. The proposed system, however, is also flexible, and can be applied for measuring and extracting parameters of other SiC power electronics device such as SiC IGBT, SiC JFET, etc. The principle can be utilized with only small modified in mathematical blocks, which represent mathematical models of measured devices. The type and technologies of measured devices can be chosen to define suitable mathematical models

The proposed test-bench is designed using the LabVIEW programming environment. The measurement uncertainty calculation is also considered. The calculated measurement uncertainty is also visualized in graphs that display the measurement results. To minimize statistical uncertainty, it is recommended that measurements be repeated more times (at least 10 times). The measurement process, therefore, is quire time-consuming. To reduce the time required for the entire measurement process, LabVIEW's ability to parallelize independent tasks is employed in the proposed test-bench.

Extracted parameters of measured MOSFET are used to improve its existing Spice model. Results of Spice simulation using models with original and extracted parameters are qualitatively and quantitatively compared with measured results to justify the suitability of the proposed approach. The comparisons clearly present a higher concordance degree of simulation characteristics using models with extracted parameters with measured characteristics than the original model, that prove the appropriateness of the approach, as well as functions of the proposed test-bench.

Future development of the test-bench will be measuring dynamic characteristics of SiC power electronic devices to calculate parameters of Spice model required by time-dependent simulation. The results are expected not only to improve existing Spice models, but also to create models of new SiC devices for purpose of lessening complexity of power electronic design by simulation.

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