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A Ku band low-voltage and low-power CMOS low-noise amplifier with bulk isolation techniques

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In this paper, a broadband(12-18G) low-noise amplifier (LNA) using 65-nm CMOS technology for satellite communication is presented. This LNA was designed in a cascode common source with inductive degeneration topology. In addition, the bulk isolation technique is employed to make the proposed LNA have a higher gain. Furthermore, a two-stage cascaded configuration combined with inductive parallel peaking technology is utilized to make the LNA achieve a wide operating band. For validation, we design this LNA in a 65nm CMOS technology. The simulated results show that S21 of 17.7dB ± 0.5dB, the input/output return loss of -10dB to -33dB and -12dB to -23dB, respectively. It offers the minimum noise figure (NF) performance of 3.33dB, reverse isolation(S12) better than 60dB, and third-order input point (IIP3) of -22.8 dBm obtained over the band of interest. Excluding the output buffer stage, the LNA is consuming 5.1 mW at a supply voltage of 0.8V and its layout area occupies 0.205 mm^2.

Keywords: broadband, low power, low-noise amplifier (LNA), bulk isolation

1 Introduction

With the rapid development of the communication field and the gradual increase in the number of communication devices, the problem of power consumption has become a focus of attention. Thus, more stringent requirements have been placed on the performance of power consumption with the aim of extending the battery life [1].

According to the IEEE 521-2002 standard, Ku-band refers to the radio wave band with the frequency of 12-18 GHz, which is extensively exploited in satellite communications and radar [2-5]. Compared with the previous C-band analogue satellite broadcasting, Ku-band digital satellite broadcasting has its outstanding features due to the use of higher frequency Ku-band and advanced digital compression technology.

The design of a broadband, low-noise amplifier often involves trade-offs between gain, input matching, noise figure and linearity. The bottleneck, therefore, is how to overcome these limitations so that performance improvements can be implemented. In traditional broadband LNA designs, they typically use a common gate stage or a common source structure with resistance feedback as the input stage [6-9]. Even though broadband input matching can be easily achieved, the loss of gain and noise figure are quite noticeable. A noise cancelling structure is usually inserted, which introduces an additional noise cancellation stage, resulting in higher power consumption and the additional noise brought in by this extra part of the circuit [10-13]. An alternative approach to achieve broadband characteristics is through the use of a two-stage cascade that combines inductive parallel peaking technology. This method not only achieves broadband capability but also enhances the flatness of the in-band gain by generating two resonance points at the low and high frequencies, which can be controlled to optimize performance [14]. Hence, this paper proposes a two-stage cascade structure integrated with inductive parallel peaking technology to achieve broadband characteristics while enhancing both gain and reverse isolation simultaneously. Furthermore, under the premise of ensuring that all MOS tubes reach saturation, power consumption is reduced by selecting the lowest possible supply voltage and bias voltage, while simultaneously combining with substrate isolation technology and inductance peaking technology to maximize gain under the premise of meeting power consumption [15, 16].

The paper is organized as follows. Section 2 primarily focuses on the analysis of input impedance and input matching of source-degraded cascode circuits, body-floating self-biasing technique, substrate isolation technique, noise analysis, and other related principles. Section 3 demonstrates the circuit design process, encompassing the selection of MOS tube size, bias voltage size, and low power consumption design ideas. Section 4 presents the simulation results of the key parameters of the designed low-noise amplifier, including the process angle and Monte Carlo simulation outcomes. The conclusion is summarized in section 5, encapsulating the main findings.

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2 Analysis of basic principles

2.1 Input matching

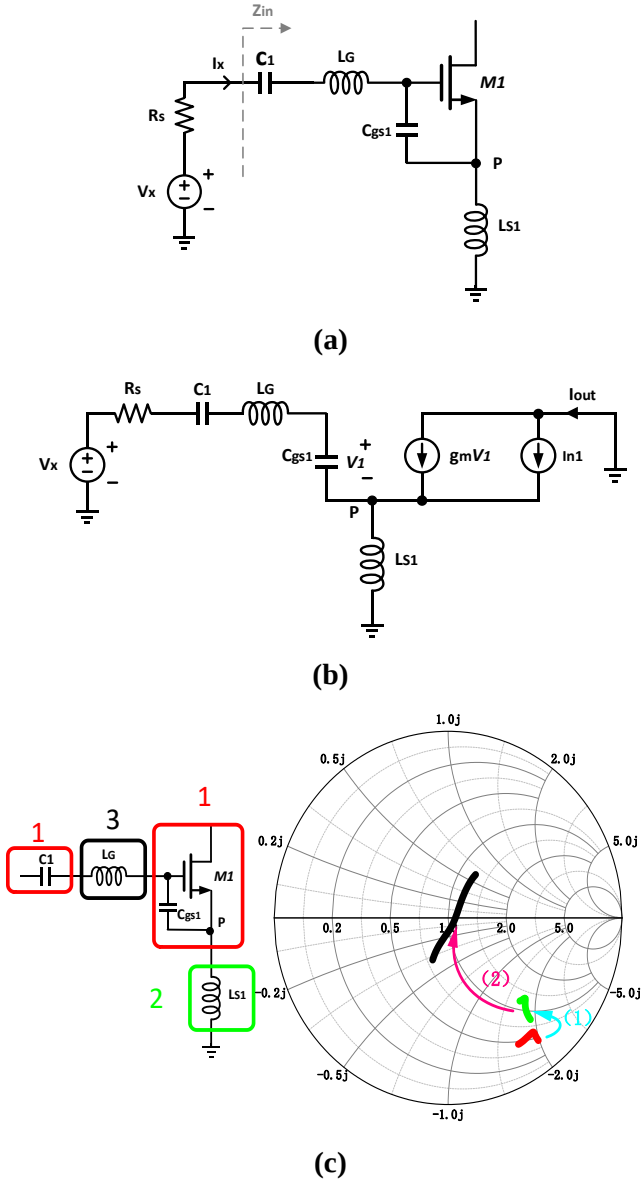

Fig. 1. (a) Input impedance of inductively-degenerated CS stage, (b) equivalent circuit for computation of NF, (c) the process of input matching is reflected on the Smith chart

The primary objective of impedance matching is to optimize the effectiveness of energy transmission. When the impedances of different components in a circuit do not align, it can lead to reflections and energy dissipation, which can ultimately degrade the quality of the signal and potentially harm the circuit. By achieving impedance matching, the signal can be optimized for transmission within the circuit, consequently enhancing the overall performance and stability of the system. The subsequent analysis explores how the inductively degenerated CS stage circuit which is shown in Fig. 1(a) achieves impedance matching across a broad frequency range. Based on the circuit analysis, the position of point P and the relationship between the input voltage and the input current can be obtained as follows:

$$V_P = \left(I_x + \frac{g_m I_x}{C_{gs1} s}\right) L_{s1} s \tag{1}$$

$$V_x = I_x \times \left(\frac{1}{C_1 s} + L_G s + \frac{1}{C_{gs1} s}\right) + V_p \tag{2}$$

Substituting Eqn. (1) in Eqn. (2), input impedance Z_{in} can be given as

$$Z_{in} = \frac{V_x}{I_x} = \frac{C_{gs1} + C_1}{C_1 C_{gs1} s} + (L_G + L_{s1}) s + \frac{g_m L_{s1}}{C_{gs1}}, \tag{3}$$

where g_m and C_{gs1} are the transconductance and gate-source capacitance of transistor M1, respectively. Capacitor C_1 is used as an isolation capacitor to prevent DC signals from flowing into the port terminal. The resonant frequency of input matching network expressed by f_0 depends on C_1, C_{gs1}, L_G and source inductor L_{s1}. The resonant frequency at which Z_{in} is real can be determined as

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{C_1 + C_{gs1}(L_{s1} + L_G)}{C_1 C_{gs1}}}. \tag{4}$$

Although the above equations show which variables are involved in the real and imaginary parts of the impedance, they do not give an intuitive picture of the matching characteristics of the broadband. It should therefore be analyzed more intuitively in conjunction with Fig. 1(c). The initial task is to ascertain the dimensions of the MOS tube M1 and the capacitor C_1. Afterward, adjust the real component near 50 ohms using L_{s1}. Lastly, fine-tune the matching characteristics within the desired frequency range by manipulating the size of L_G.

2.2 Noise analysis

Ideal inductors and capacitors in circuits do not generate noise, and although parasitic resistors are present in the actual components to exacerbate the noise, the main source of noise is from MOS tubes, mainly due to channel thermal noise, flicker noise and gate resistance. As the design frequency band is Ku-band, the effect of flicker noise will be small and can be neglected. As for the noise introduced by the equivalent resistance of the gate, it can be minimized by the use of multi-finger structures. Hence, the dominant factor contributing to the noise in the MOS tube is the channel thermal noise. Finding ways to minimize the channel thermal noise in the MOS tube is crucial for reducing the overall noise figure. By analyzing the noise in the small signal circuit of Fig. 1(b) in conjunction with Eqn. (4), the following equation can be introduced

$$V_x = I_{out} \times \left(j\omega_0 L_{s1} + \frac{j\omega_0 R_s C_{gs1}}{gm}\right) - I_{n1} \times \frac{jR_s C_{gs1}\omega_0}{gm}, \quad (5)$$

where $\omega_0 = 2\pi f_0$, I_{n1} denotes the thermal noise current of the channel. If we assume is equal to zero, we can establish the correlation between I_{out} and I_{in}, and then deduce the expression of the noise factor, which in turn gives the following noise figure expression

$$NF = 1 + \frac{(C_1 + C_{gs1})C_{gs1}R_s\gamma}{C_1(L_{s1} + L_g)g_m}, \quad (6)$$

where γ represents the excess noise coefficient of the MOSFET. The value of γ is 2/3 for long-channel transistors and may rise to even 2 in short-channel devices. According to Eqn. (6), it can be inferred that to decrease the noise figure, it is essential to enhance the dimensions of either the inductor or the MOS tube. However, both approaches will impose constraints on other performance factors like power consumption and area. Therefore, it is crucial to carefully evaluate the trade-offs in performance when determining the size.

2.3 Bulk isolation techniques

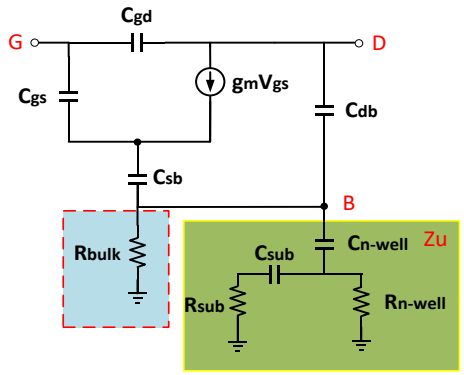

Fig. 2. Small-signal modeling of nmos RF transistors

Figure 2 illustrates the small-signal model of the nmos RF transistor, where Zu represents the impedance values consisting of R_{sub}, C_{sub}, $C_{n\text{-well}}$ and $R_{n\text{-well}}$. To enhance the amplification of the transistor at high frequencies, it is necessary to decrease the impact of C_{sb} as well as C_{db}. In the high-frequency band, the impedance values of C_{sb} and C_{db} are drastically reduced, which is to some extent equivalent to connecting the S-terminal to the D-terminal, leading to increased power consumption. To achieve a low-power design, the primary strategy is to separate the substrate by inserting a high-value resistor between the substrate and the ground. This arrangement enables the impedance values of Z_u and R_{bulk} in parallel to have a significant magnitude in the frequency range. As a result, there is an approximation of an open circuit between C_{sb} and C_{db} [17].

2.4 Body floating and self-bias technique

The body floating and self-biasing techniques are different from the substrate isolation technique. In this technique, the substrate is connected to the drain side of the MOS transistor using a large resistor. By adjusting the resistance of the resistor, the voltage (V_{bs}) between the substrate and the source side of the MOS transistor can be changed. This allows for the adjustment of the threshold voltage, which in turn improves the gain and noise performance [18].

3 Circuit design

As the MOS channel length decreases, the threshold voltage decreases correspondingly. Consequently, a lower bias voltage can be employed to drive the MOS transistor into saturation. Moreover, a shorter MOS channel length enhances the on-state capability of the MOS tube and diminishes parasitic capacitance. Consequently, the MOS tube exhibits a higher cut-off frequency (f_T) and operates at a faster speed, rendering it more suitable for high-frequency band design. However, reducing the MOS channel length also results in a decline in the intrinsic gain and noise performance of the MOS tube. This presents a challenge in guaranteeing superior performance in the high-frequency band. The cascode topology, owing to its higher gain, provides enhanced gain and input/output isolation compared to a single tube amplifier. Furthermore, the cascode structure effectively mitigates the Miller effect of the input common-source stage, thereby significantly improving the bandwidth. This is precisely why the proposed design incorporates the cascode topology. Nevertheless, it is important to acknowledge that the gain flatness of this structure is not as superior as that achieved with an amplifier featuring a resistor-parallel feedback structure. Figure 3 depicts the schematic of the proposed LNA.

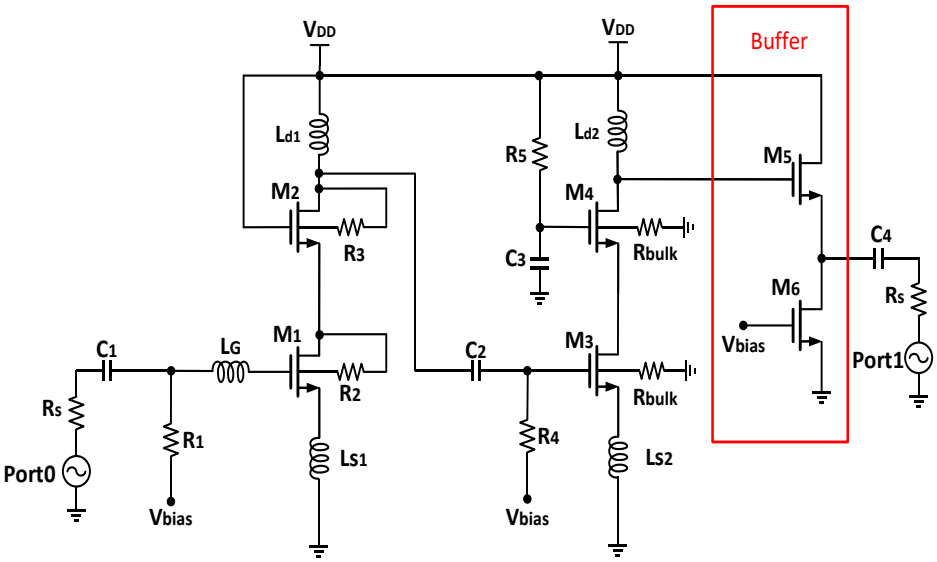

Fig. 3. Schematic of the proposed CMOS wideband LNA

The proposed LNA comprises two cascode stages connected by a capacitor. A buffer is linked to the output to enhance the ability to handle the load and to achieve wide-range output compatibility. In the first cascode stage, the body floating and self-biasing technique is employed to decrease the MOS threshold voltage and enhance the performance of S21 and *NF*. The second stage utilizes a bulk isolation technique to achieve lower power consumption compared to the first stage and to amplify the high-frequency band by increasing the resistance of the resistors. In the source-degraded cascode structure, achieving low power consumption and large gain can be accomplished by utilizing a larger LG and smaller transistor size. However, the presence of significant intrinsic parasitics in the LG adversely affects the noise performance. Conversely, employing a smaller LG and larger transistor size ultimately leads to improved noise performance, but at the expense of increased power consumption. Therefore, in this paper's low-power design, the former approach is adopted to reduce power consumption while simultaneously ensuring satisfactory noise performance.

To further enhance the noise performance, it is crucial to avoid setting the value of LG excessively large. Additionally, maximizing the number of fingers of M1, as permitted by the Process Design Kit (PDK), effectively reduces the thermal noise generated by the physical resistor of its gate. In terms of the noise contribution from the first-stage cascode transistor M2 at the input, it can be observed that the noise of the M2 is reduced. This reduction is attributed to the noise equivalence theorem, which states that the noise equivalence of the M2 to the input is divided by the intrinsic gain of the M1, as per the analysis. Regarding the noise contribution from the second cascode level, the overall noise figure (NFtot) of a cascaded system with *n* stages can be determined using the Friis formula, as shown in Eqn. (7). Here, NF_m and AP_m represent the noise figure and gain of the m stage, respectively [17].

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots \\ \cdots + \frac{NF_m - 1}{A_{P1} \cdots A_{P(m-1)}}. \qquad (7)$$

Analysis of the Eqn. (7) reveals that the noise in the second stage is divided by the gain of the first stage, indicating that the primary source of noise originates from the first stage. However, it is important to note that the gain of the first stage gradually diminishes as the frequency increases. Consequently, this leads to an increase in noise in the high-frequency band. Therefore, body floating and self-bias techniques are introduced in the first stage to enhance the gain of the first stage and thus reduce the noise introduced by the second stage. To further decrease the amount of noise in the high-frequency range, it is possible to include a bypass capacitor C3 at the gate of M4. The function of capacitor C3 can be illustrated by referring to Fig. 4.

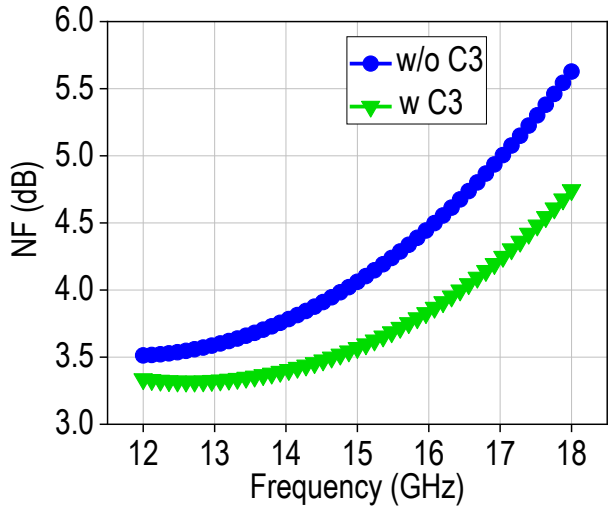

Fig. 4. Comparison of simulation results of noise figure with or without capacitor C3

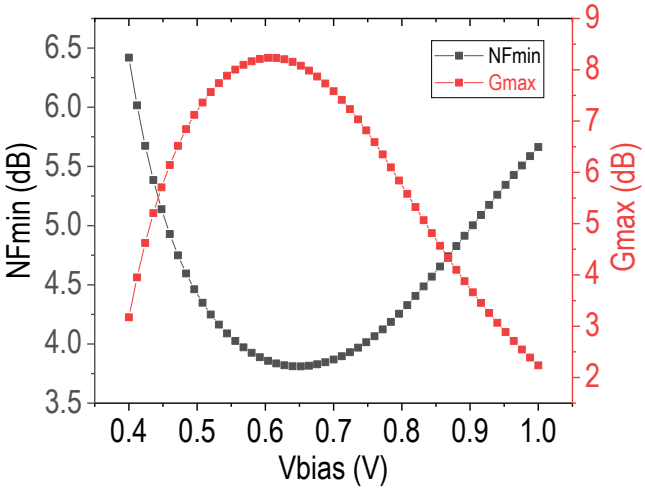

Fig. 6. Curves depicting the relationship between bias voltage and both minimum noise figure and maximum available gain

Directly biasing the gate of M4 by connecting it to VDD can result in instability and inadequate output matching due to the parasitic effects of the lead inductors. To address this issue, it is recommended to incorporate a resistor in series with the M4 gate and a parallel inductor. This configuration effectively reduces crosstalk and mitigates the adverse effects of the parasitic elements. Based on the results of a static DC simulation of the circuit depicted in Fig. 5, it was discovered that the threshold voltage of the 65 nm RF NMOS transistor is approximately 550 mV. To ensure optimal performance in the saturation region and minimize power consumption, a biasing voltage of 600mV has been chosen.

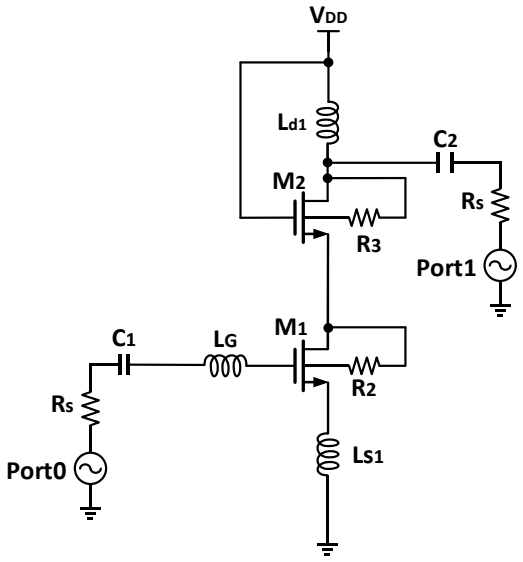

Fig. 5. The first stage of the proposed circuit

Moreover, based on the information presented in Fig. 6, it is evident that the optimal performance, characterized by the highest gain and lowest noise figure, can be achieved when V_{bias} is set to 600 mV. This observation suggests that adjusting the bias voltage to this specific value can result in a more favorable and desirable outcome. After determining the bias voltage, the width (W) of the MOS transistor needs to be selected based on power consumption. In this case, the minimum length (L) is set to 65 nm, and the maximum number of fingers is chosen as 32. Therefore, W should not be excessively large to avoid increasing power consumption and introducing large parasitic capacitance that could reduce the speed. For more details, refer to Fig. 7.

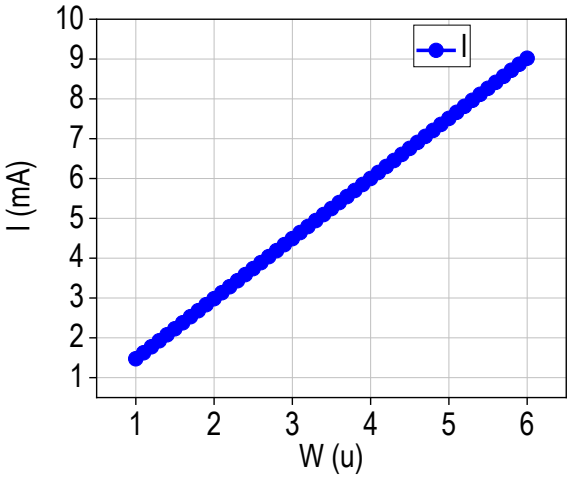

Fig. 7. The relationship curve between the width (W) of the MOS transistor and the corresponding current

In this design, the width (W) of the MOS transistor is configured as 3.1 μ to constrain the current to be below 5 mA, thereby reducing power dissipation. To reduce power consumption, the power supply voltage (VDD) is chosen to be 0.8 V, while ensuring the MOS transistor operates within its normal working range. Due to the limited VDD of 0.8 V, to further enhance the output swing, it is possible to increase the size of the cascode transistor M2. In this design, the dimensions of M2 are chosen to be identical to those of M1. The selection of the dimensions of LG and LS1 can be considered based on the analysis of input matching in the second part. Ld1 and Ld2 are responsible for generating gain peaks at low and high frequencies respectively. To ensure optimal performance in the frequency band of interest, Ld1 and Ld2 should be chosen to have as high a Q value as possible, because the Q value will be attenuated with frequency, which will deteriorate the characteristics of the noise, gain, etc. To further improve the flatness of the gain and achieve inter-stage energy transfer, it is advisable to choose a slightly larger capacitor for C2. To reduce power consumption, R2 and R3 can be selected with a higher value. In this design, it is recommended to choose a standard 10k resistor. Similarly, the Rbulk resistor can also be chosen as 10 kΩ to increase the gain at high frequencies, as shown in Fig. 8.

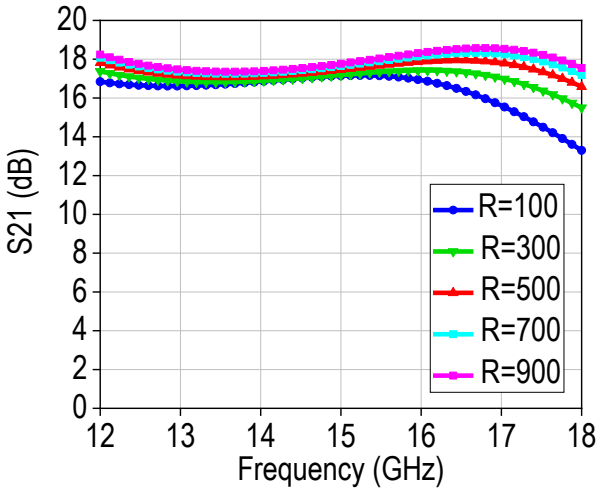

Fig. 8. The curve of Rbulk resistance value as a function of S21 gain

After completing the design of the first stage, the second stage design method is similar to the first level. However, for power consumption considerations, the size of the MOS transistors in the second stage is reduced to achieve a better trade-off between gain and power performance. Table 1 demonstrates the final value of the proposed LNA components.

Table 1. Values of components of the proposed LNA

Component	Value	Component	Value
M_1	$\frac{32 \times 3.1\ \mu m}{60\ nm}$	L_{s2}	70 pH
M_2	$\frac{32 \times 3.1\ \mu m}{60\ nm}$	C_1	1 pF
M_3	$\frac{32 \times 2.1\ \mu m}{60\ nm}$	C_2	1.2 pF
M_4	$\frac{32 \times 2.1\ \mu m}{60\ nm}$	C_3	1 pF
M_5	$\frac{16 \times 2\ \mu m}{60\ nm}$	C_4	1 pF
M_6	$\frac{16 \times 2\ \mu m}{60\ nm}$	R_1	10 kΩ
L_G	1.3 nH	R_2	10 kΩ
L_{d1}	1.3 nH	R_3	10kΩ
L_{d2}	1.5 nH	R_4	10 kΩ
L_{s1}	170 pH	R_{bulk}	10 kΩ

4 Simulation results

The LNA, as described in this paper, undergoes schmatic-level design using Cadence Virtuoso. It is then simulated using Cadence Spectre. The extraction of parasitic parameters and the layout drawing, depicted in Fig. 9, are carried out using Cadence Calibre.

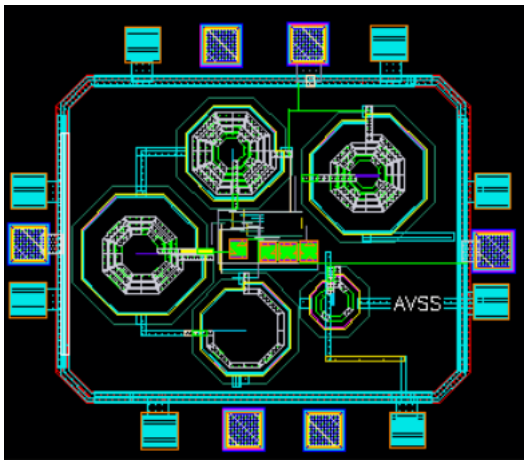

Fig. 9. Layout of the proposed LNA

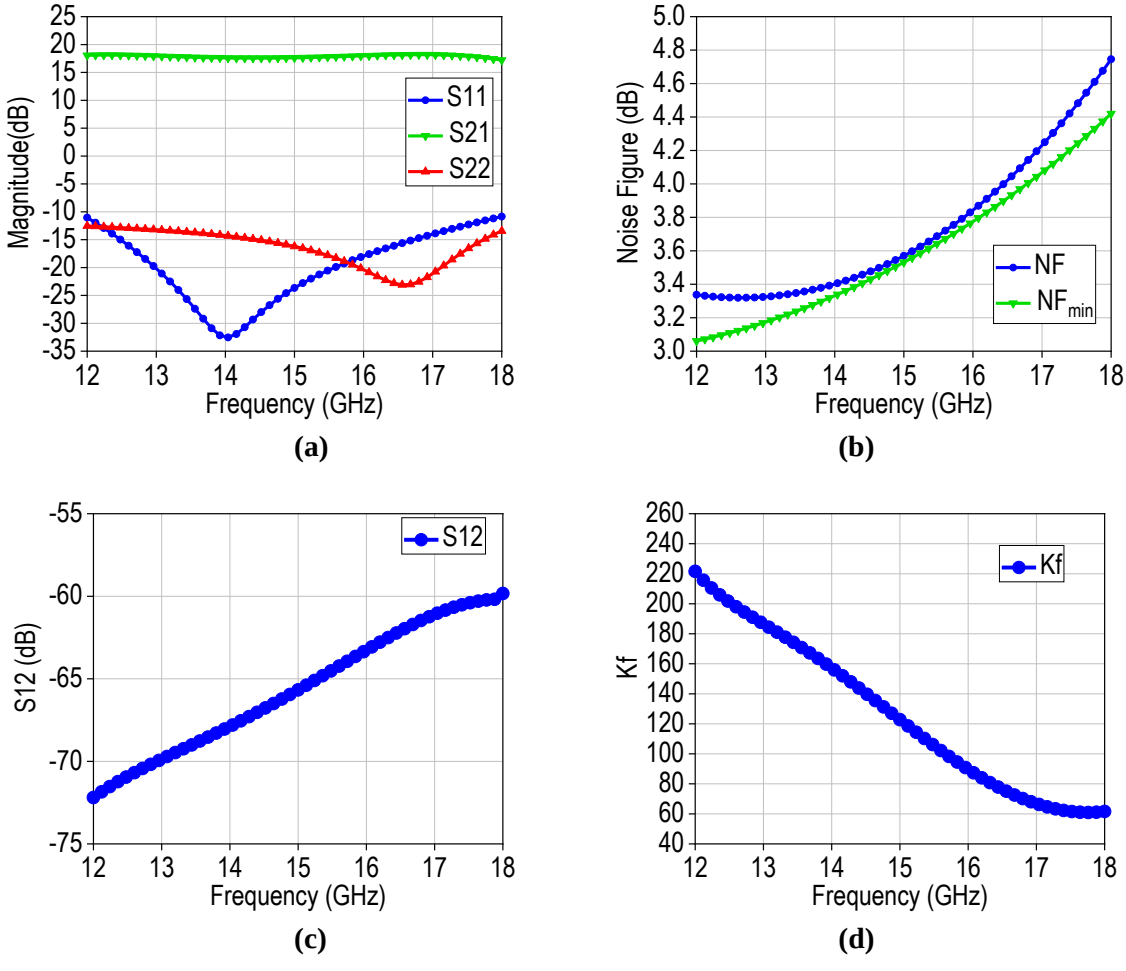

Fig. 10. Simulated (a) S_{11}, S_{21} and S_{22}, (b) NF and NFmin performance, (c) S_{12}, (d) stability factor K_f

The performance metrics of input/output matching, noise figure, gain, stability, and reverse isolation of the LNA are simulated as shown in Fig. 10. Figure 10(a) displays the forward gain S21, as well as the input and output reflection coefficients (S11 and S22, respectively). What can be observed is the good flatness of the gain in the Ku-band, and the reflection coefficients of the inputs and outputs are less than –10 dB in the band. Figure 10(b) depicts the variation of the noise figure (*NF*) and the minimum noise figure (NF_{min}) with frequency. At a frequency of 15 GHz, NF is approximately equivalent to NF_{min}. Figure 10(c) shows the circuit with a significant level of reverse isolation, while Fig. 10(d) demonstrates that the circuit possesses a high stabilization factor. This implies that the circuit can typically be maintained in a stable condition as long as the value of K_f is greater than 1.

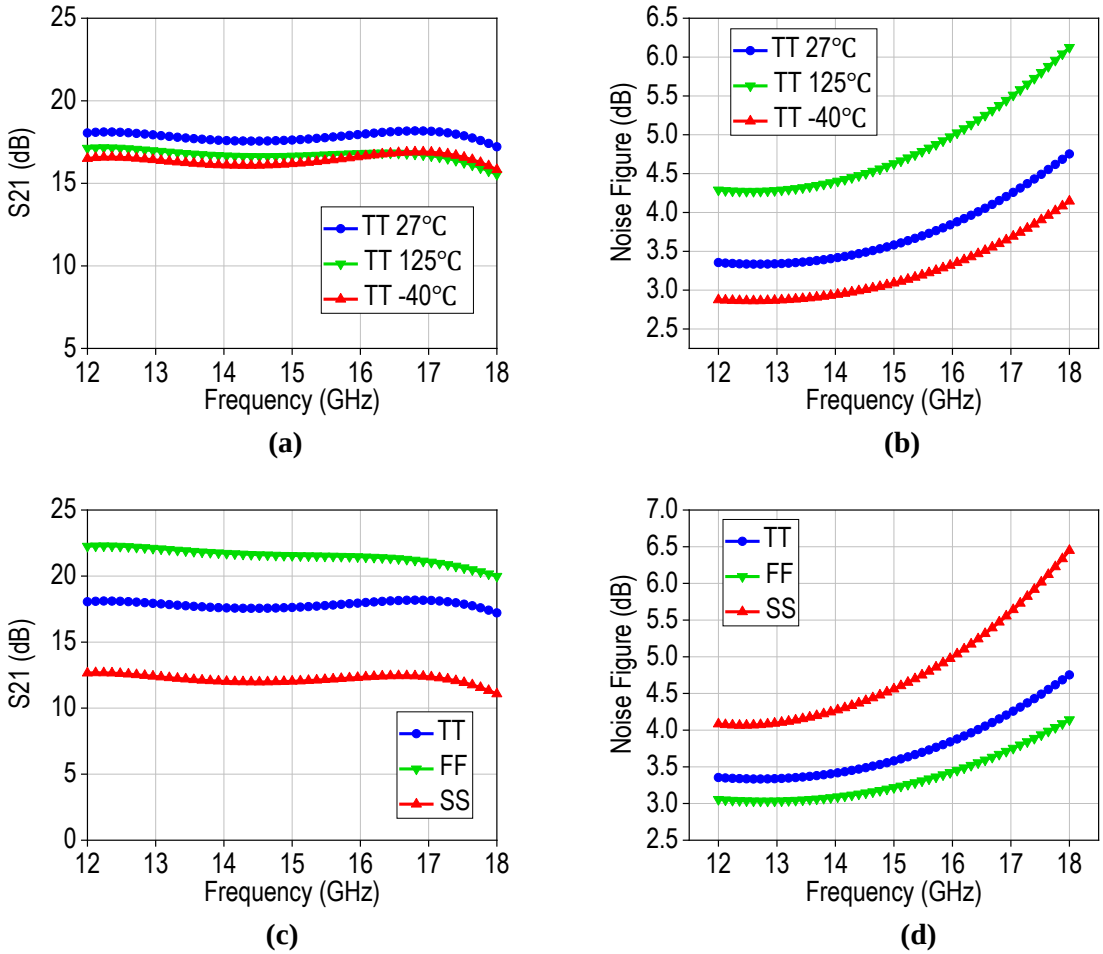

Fig. 11. (a) S21 and (b) NF simulation results at different temperatures at TT process corner, (c) S21 and (d) NF simulation results at the same temperature with different process corners

Figure 11 demonstrates how both temperature and process corners impact the S21 and NF of the LNA. It can be seen that the effect of temperature on the gain is relatively small at the TT process corner, whereas the deterioration of temperature on the noise figure is more serious, and this phenomenon is more pronounced, especially in high-temperature environments. The results of the simulation at various process corners indicate that there is a significant deviation in both the S21 and NF of the LNA. The primary factor contributing to this deviation is the variation in MOS transistor characteristics and the process parameters of the inductor and capacitor. The analysis of the third-order cross-modulation point involves the use of a 1 MHz two-tone signal, which produces two harmonic components at 15 GHz. The simulation results as shown in Fig. 12 indicate that the third-order input intercept point (IIP3) is equal to –22.8 dBm.

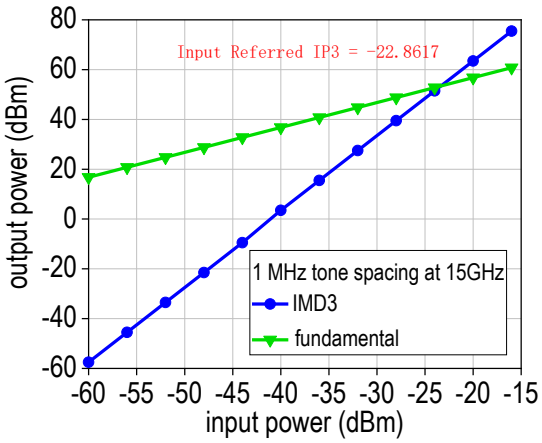

Fig. 12. Input third order intercept (IIP3) of the proposed LNA

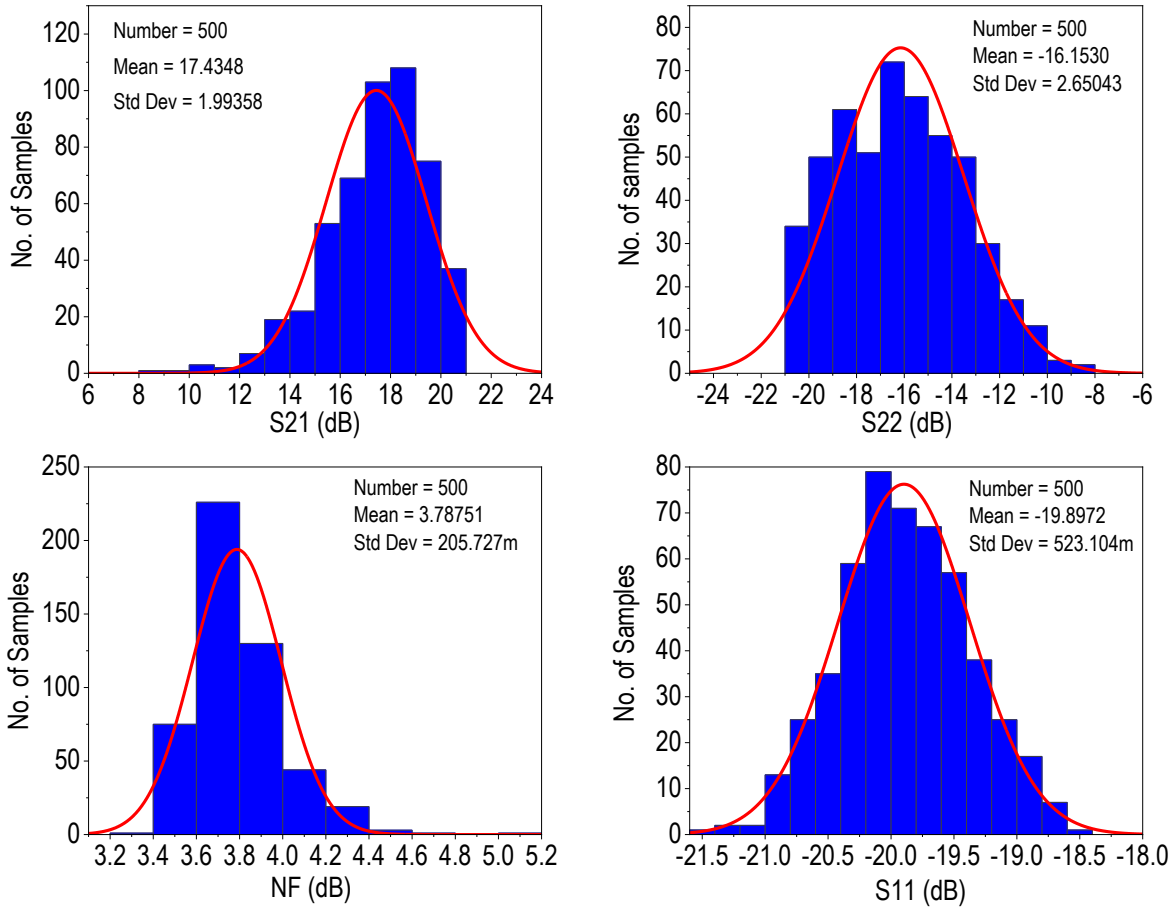

Fig. 13. Monte Carlo results for 500 samples of the proposed LNA

To achieve a more precise analysis of the circuit's characteristics and ensure reliable circuit performance, Monte Carlo simulation is introduced. This simulation technique plays a crucial role in accounting for the inherent variations that occur during the production of integrated circuits, thereby enhancing the accuracy and reliability of our analysis. To ensure the reliability and robustness of our findings, a Monte Carlo analysis was conducted with a sample size of 500. This analysis aimed to verify that the results remained within an acceptable range.

The histograms in Fig. 13 depict the input return loss, output return loss, gain, and NF (noise figure) of the circuit, and the red curve shows the overall distribution

of trends. Notably, all samples exhibited an input return loss exceeding 15 dB, while the majority of samples demonstrated an output return loss surpassing 10 dB. The maximum available again ranged from 17 to 19 dB, and the NF was concentrated in the range of 3.4 to 4.0 dB for the majority of samples. Table 2 provides an overview of the performance results obtained from the simulated implementation of the designed LNA, as well as a comparison with previously published works. The proposed LNA in this study exhibits superior performance compared to existing LNAs in terms of gain and noise characteristics within the same frequency range. This notable improvement can be attributed to the incorporation of body floating and self-biasing techniques. Furthermore, the LNA presented in this paper offers the advantage of lower voltage and power consumption in comparison to similar works in the field.

Table 2. Comparison with similar LNA work available in the literature

Ref.	Techno-logy	Frequency (GHz)	Supply (V)	S11 (dB)	S21 (dB)	NF (dB)	Power (mW)	IIP3 (dBm)	Area (mm^2)
[6]*	180-nm CMOS	17.5	1.8	< –10	18(Max.)	3.6	12.6	–2***	0.48
[20]*	40-nm CMOS	10-14	1	< –10	11(Max.)	2.5	10	1.2***	0.162
[21]*	65-nm CMOS	9.2-12.2	1	NR	32.4(Max.)	1.66(Min.)	22	–25.3	0.24
[22]*	65-nm CMOS	6.7-15.3	0.8	NR	20(Max.)	2.08(Avg.)	12.8	–9	0.144
[3]*	180-nm CMOS	12-18	0.8	< –8.2	8.58~12.72	3.7 ~ 4.8	7.68	–7	0.67
[4]*	180-nm CMOS	12-18	1.8	–6.7 ~ –10.3	8.78–10.59	3.96 ~ 5.33	22.175	8	0.326
[5]**	65-nm CMOS	12-18	0.8	–7.5 ~ –32.7	11~11.66	4.6 ~ 5.47	2.2	–12.4	0.255
This work**	65-nm CMOS	12-18	0.8	< –10	17.21~18.25	3.33 ~ 4.74	5.1	–22.8	0.205

*Measurement results, **Simulation results, ***Calculated based on IIP3 = P1dB + 10 dB
NR = not reported, Max: maximum, Avg: average, Min: minimum

5 Conclusions

This paper presents a comprehensive analysis and design process of an LNA utilizing a two-stage cascode structure and 65 nm CMOS process technology. The proposed LNA, with its cascode structure, effectively achieves both favourable reverse isolation and stability. The final simulation results obtained by Monte Carlo analysis validate the exceptional performance of the proposed LNA, showcasing its remarkable broadband input matching characteristics, high gain with excellent flatness (17.7 dB± 0.5 dB), and low average noise figure of 3.78 dB. Moreover, the LNA exhibits outstanding low-voltage and low-power characteristics, consuming 5.1 mW at a supply voltage of 0.8 V. The paper further introduces a meticulous design methodology that emphasizes the selection of active device size and DC bias conditions. This method is devised with the objective of attaining the utmost reduction in noise figure (NFmin) and the highest achievable gain (Gmax). Furthermore, with the implementation of substrate isolation technology and body-floating self-biasing technology, not only the deterioration of the second-stage noise with the rise of frequency is suppressed, but the gain in the high-frequency band is improved.

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