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REVIEWS - LETTERS - REPORTS

A NOVEL METHODOLOGY FOR REDUCING THE POWER SUPPLY VOLTAGE DROP AT THE CORE OF IC'S CHIPS

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This paper proposed an efficient reduction method of voltage drop (IR) at the core of high density IC's chips. The presented method is based on branching out several layer of metals from the I/O bond-pads of power supply and feed them to the core of the chip through a data and other non power supply pads. Hence, the up most two layers of metals (M6, M7) for seven layers of metals technology are pass through all I/O bond-pads forming a ring structure. Furthermore, M6 and M7 are stripped through the data and control I/O pads with ground and high voltage connection to the core of the chip. Thus, increases the current density area of power supply through an increase of metal area without adding an additional count of power supply I/O pads.

K e y w o r d s: Bond-pads, I/O Pads, IR, M6, M7, Power Pads

1 INTRODUCTION

Continues improvements in base technology have increases the IC's densities to the order of million transistors per chip [8–13]. Moor's law states that the number of transistors per chip double every year [10], where a more confine results show that semiconductor technology has been roughly quadrupling every three years [12]. One aspect often overlook is the number of I/O pads with the increase density of the IC's from one side and decreasing the silicon geometry area through technology scaling from another side. Dice are usually bonded using the smallest possible diameter of wire, since this enables the use of the smallest bond-pads. These wires consist of either gold or aluminum, and they range in diameter from 20 μm to 250 μm in diameter attached to the die by means of ball-bonds. The placement of bond-pads also restricts the routing of adjacent metal leads. This limits and bounds the maximum available power supply I/O pads. In such a way we can state that, the available number of power supply I/O pads on a single IC might be safely limited by the given formula:

$$\begin{aligned}&\text{Total Minimum Number of I/O pads} = \\ &(\text{Minimum Requirements of Data and Control I/O pads}) \\ &+ (\text{Suggested Power Supply I/O pads that provide a} \\ &\quad \text{margin greater than 15 \% available IR Drop} \\ &\quad \text{at the Core}) \quad (1)\end{aligned}$$

In this brief, our focus is to construct a layout methodology that can reduce the IR drop at the core of the chip with minimum addition of power supply I/O pads. Thus, it is improving the IC's functional utilization and capabilities by allowing more placements of data and control pads, while maintaining the reliability of signal integrity with acceptable level of noise margin at the core of silicon chip [5–7].

Since most of the modern IC's uses seven layers of metals for the forming of bond-pads, it is found from an experimental fabrication point of view that the ball-bond presses against the first a few layer of metals with enough force and decreases gradually with the higher level of metals [1–3]. Hence, the effect of ball-bond contact is a quit minimum at metals M6 and M7. Therefore, metals M6 and M7 **vias** contact layers can be eliminated in most cases without affecting the instantiation process of bond-wires and bond-pads.

Furthermore, the bond-wires connected to bond-pads are widely consisting of either gold or aluminum, and they range in diameter from 20 μm to 250 μm attached to the bond-pads by means of ball-bonds. A gold bond-wire package in plastic can approximately conducts one amp of continuous current per 20 μm in diameter [3]. However, due to the limited layout geometry area of the I/O pad, the power supply pad with all its layer of metals utilizes about $100 \sim 500$ mA.

This pave the road for Viatechnology.com and S3garphics.inc to investigate ways of improving the utilization of current source to the core of IC's chips through a joint product called SavageXP graphic chip [14] with about one hundred million transistor products at 0.15 μm TSMC technology and seven layers of metals [15]. As a result, the technique improve timing performance and signal integrity with good noise margin and minimum decoupling value, which makes the product runs at 200 MHz with an acceptable number of I/O power supply pads.

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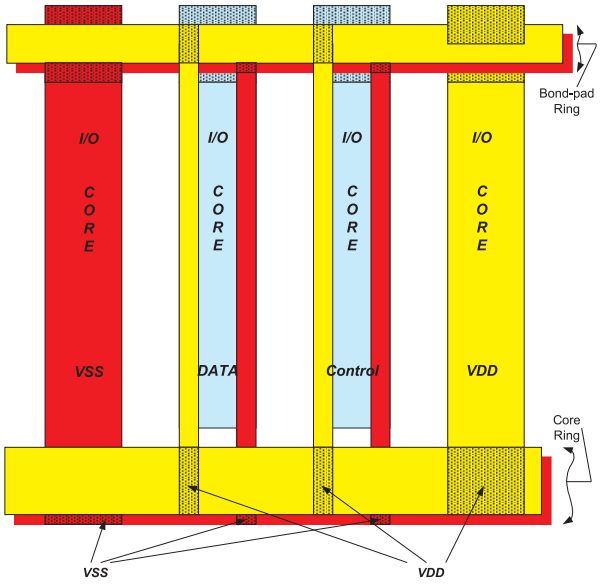

Fig. 1. Data and Control Pads layout routing topology.

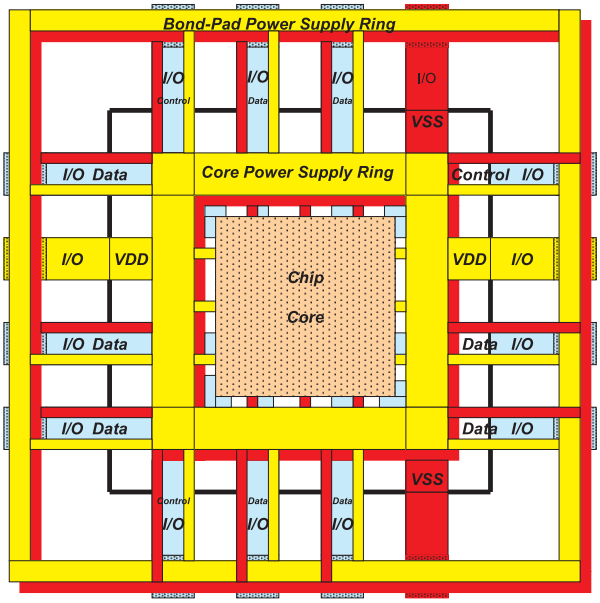

Fig. 2. Complete Chip layout routing topology.

2 LAYOUT DESIGN METHODOLOGY

Complementary Metal Oxide Silicon (CMOS) technology primarily increase rout ability of the circuits by providing two or more layer of metals. Notably, present technology provides seven or more layers of metals which can be used as signal and power-routing layers. The bounding pads usually contain all metal layers providing a large number of **vias** contact which are used in the connection. In general, power and ground pads are repeated on the perimeter of the IC to distribute power within the circuit since they have a limited width structure; although, they are constructed from all available metal layers. Our main objective is to minimize the number of repeated power supply pads (Vdd, Vgnd) with the increase of circuit density and functionality through technology scaling factor. The proposed idea is constructed by branching out from Vdd- and Vgnd- bond-pads the last two metals (M6, M7) and routing them through all available bond- pads (*ie* Data, Control, and mix Power) in a form of ring bus of two metals in parallel. Then, data and control pads are used to branch in metals M6 and M7 from their bond-pads to their I/O circuitry pads and then to the core of the chip as shown in Fig. 1. Metals M6 and M7 are combined and joint with all designated power supply pads at the core forming an internal ring of continuous power supply as shown in Fig. 2.

One thing to emphasis on is that the data and control bond- pads are not connected to metals M6 and M7 in a form of **vias** contacts; they allow metals M6 and M7 to pass through them and be stripped to the core. Then, adding an internal bus ring for Vdd and Vgnd-supply in order to collect and sum all currents to the core of the IC's. Thus, the method provides denser of current supply around 1 Amp per supply pad.

3 EXPERIMENTAL RESULTS

This work is thoroughly investigated by me during my work as a senior member of technical staff at Viatechnology.com and S3graphics.inc through a product called SavageXP which was targeted for graphic chip device. The SavageXP product is implemented at 0.18 μm TSMC technology with about on hundred million transistor core, and then later it shrinks to 0.15 μm TSMC technology with an operating frequency of 200 MHz. The product has all nature of I/O pads; such as, PCI, AGP2X, AGP4X, DDR, and analog pads [13, 14]. In addition, it has different mixed level power pads for digital and analog nature pads. The main difficulty was to clear I/O ring LVS net-list and avoids any short, many script were added to fully clear LVS and make sure no unwanted short and contact is placed. The chip was run successfully at a target operating frequency of 200 MHz and went to full production. In addition, the same chip was successfully shrink down to 0.15 μm TSMC technology with 0.18 μm base technology and also was successfully went to full production without the need of adding an additional power supply I/O pads.

4 CONCLUSION

The proposed methodology is targeted for many handheld IC's application devices and low power applications (*eg* 2 Watt), where the die is a quit dense with million of CMOS transistors technology and the geometry silicon area is limited with number of required power supply I/O pads, and on the other hand, the total power dissipation is less than the order of 2 watt. The method reduces the IR drop by branching out from the power supply bond-pads the topmost metals and feed them to

the core through non-power supply pads. This was due to the fact that the bond-wire conducts approximately one amp of continuous current per its won width of 20 μm, while the power supply pad conducts only about 50 % of bond-wire value. This, in general, is due to the limited geometry layout area of pads. Moreover, the ball-bond at the end of bond-wire stresses heavily on the lower metal than on the topmost metal during the bonding process, which allow the methodology to take advantage of the top metal without affecting the deforming process. The first successful product was SavageXP with about 100 million transistors chip and was targeted for graphic chip lab-top product market.

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