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MAGNETIC FET–BASED ON–CHIP CURRENT SENSOR FOR CURRENT TESTING OF LOW–VOLTAGE CIRCUITS

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A new built-in current sensor design using the magnetic force of a magnetic FET (MAGFET) is presented. Theoretical background together with special features and physical implementation of single individual parts of the sensor as well as specific shapes and their individual advantages are described in details. The proposed sensor is aimed to be used for current testing in deep-submicron circuits with ultra low-voltage power supply (below 2 V). The main advantage of the proposed sensor is elimination of the undesired supply voltage reduction, commonly created by standard current test methods. Description of two different sensor shapes, sensor design and its physical implementation on the chip is presented. The different sensor shapes evaluation results are finally compared in order to obtain the highest possible sensitivity of the structure. Both sensor versions were fabricated in a selected 1 μm BiCMOS technology.

K e y w o r d s: MAGFET, magnetic force field effect transistor, integrated magnetic sensor, built-in current sensor, IDD testing

1 INTRODUCTION

In the area of deep-submicron IC, new physical defects and failures are revealed, which might not be covered using regular conventional test methods. Rather a large fraction of those failures might be detected by novel and inventive current test methods. However, MOSFET leakage current is growing rapidly with the feature size scaling that causes vanishing of the difference between defect-free and defective supply current levels of the design under test (DUT). Due to this fact, the regular current test methods, based on voltage drop sensing over a resistive element, exhibit unwanted supply voltage degradation for the DUT. This voltage drop might be accepted at relatively high supply voltage technologies, but in technologies with low VDD, this might cause undesirable effects [1–3].

A novel supply current measurement technique using specific magnetic sensitive structures, such as magnetic MOSFET (MAGFET), is described in this article. The magnetic MOSFET device is a sort of magnetic sensor, which can sense the magnetic field and provide corresponding electrical signal (preferably current or voltage) on the output [4, 5]. The physical structure of the sensor is based on split adjacent drain terminals. The MAGFET senses the magnetic field, perpendicular to the channel. Since the structure of MAGFET is compatible with structures in standard CMOS or BiCMOS technologies, the sensor could be widely used as a common library item. Therefore, integration of the MAGFET based current monitor on a chip with other signal-processing circuitry requires no advanced technology. Combination of conventional built-in current sensors (BICS) and a MAGFET-based current monitor may cover a wider area of defects.

Because of the above mentioned on-chip integration availability, the MAGFET principle is attractive to research of built-in current testing. Even though the research on current sensors using MAGFET achieved promising results, none of the research groups tried to utilize MAGFET for sensing of very low currents, as low as the supply current of conventional circuit cells.

The power supply line, feeding the DUT, creates a certain preferably direct magnetic field. This phenomenon is described by the Ampere law. Respective magnetic induction is then sensed by a galvanic separated MAGFET sensor. This paper deals with the development, physical design and analysis of a new current monitor for on-chip IC testing, based on the above mentioned MAGFET sensor. The electric to magnetic (and backward) conversion can thus replace the resistive sensing element, necessary for current magnitude measurement, which is the main advantage of a MAGFET sensor. The rectangular MAGFET transistor is in shape and electrical parameters the same as any regular N-channel or P-channel MOS transistor, so it is easy to implement together with a DUT on the same chip. Although the rectangular shape is very common, recent studies shows that the sensitivity of MAGEFT depends on its geometrical parameters and structures different from to the rectangular shape achieve higher sensitivity. Several rectangular and sector structures were suggested, designed and implemented in order to select the most appropriate shape for the on-chip current sensing purpose.

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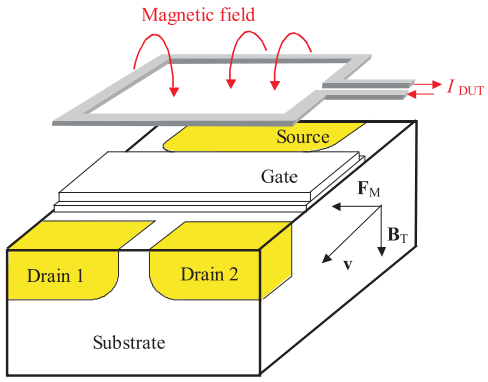

Fig. 1. MAGFET sensor with the DUT power supply line loop (above the structure)

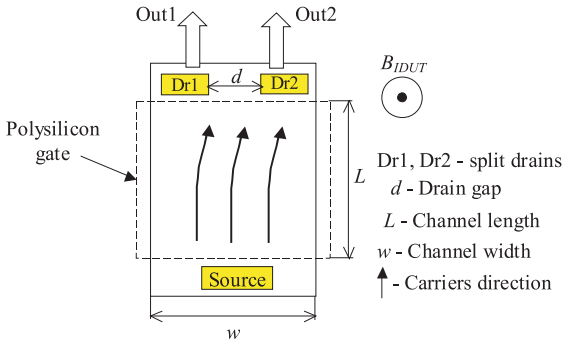

Fig. 2. Principle of split-drain MAGFET sensor

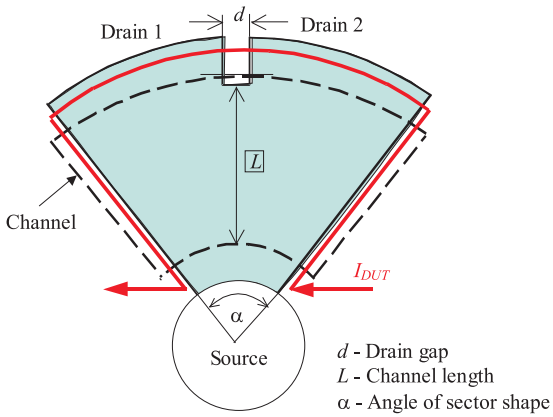

Fig. 3. MAGFET sector shape

2 SENSOR STRUCTURE

MAGFET is a sensor that is essentially a MOSFET having one source and two drains. The basic principle is illustrated below. The transistor drain is split into two separated parts so that the transistor could act as a magnetic field sensor based on the Hall-effect. The Lorenz force exerted on electrically charged carriers q_e, moving in magnetic field $\mathbf{B}$ with speed $\boldsymbol{v}$, is

$$\mathbf{F}_M = q(\boldsymbol{v} \times \mathbf{B}) = q\mathbf{E}_H \,, \tag{1}$$

where $\mathbf{E}_H$ represents the equivalent Hall electric field intensity. When a magnetic field B to the transistor surface is applied to the sensor, the carriers in MAGFET channel are deflected under the action of the Lorenz force, which leads to different numbers of carriers flowing through the first and second drains. This drain current difference is proportional to the intensity of the perpendicular magnetic field. The device works electrically like a standard MOS transistor, while its magnetic field sensing capability is due to a split drain.

In Fig. 1, Drain 1 and Drain 2 are the split drains, v – is the carrier speed, B_T – is the induction in direction of z axis, F_M Lorenz force, I_{DUT} the DUT supply current direction. The sensitivity of such a sensor depends on several factors, which are: the MAGFET channel length and width, drain gap, source and drain contact sizes as well as the biasing conditions of V_{GS} and V_{DS}. As the MAGFET shape is not necessarily rectangular, there are other different possible nonrectangular forms of this sensor, and sensitivity could depend on the angle of the shape.

The basic concept of sensors, introduced in this paper, consists of the transistor structure shape with split drains. The structure is surrounded (along the edges of the transistor active area) by the metallization line, supplying the DUT circuit in very close touch with the channel. The metallization line layout position contributes to the intensity of the magnetic field as the magnetic force source is very close to the transistor channel (Figure 2). The power supply metallization surrounds the active area of the transistor, which helps to increase the strength of the magnetic field. The magnetic flow density in the active area could be much stronger, since the metallization line could be laid out in many levels of metal loops, depending on the number of metallization layers available. Due to this fact, uniformity of the magnetic field direction is provided. Thus, a metal loop lies close to the active area but never crosses it.

Due to a strong magnetic field the impact on the carrier deflection is significant. The magnetic induction B in the vicinity of a long filament can be estimated as follows:

$$B = \frac{\mu I}{2\pi r} \,, \tag{2}$$

where I is the current of the metallization supply line feeding the DUT, r is the distance from the magnetic field source (filament), and μ is the magnetic permeability. The magnetic field force (Lorenz force) acting on a single carrier can be expressed as follows:

$$F_M = B_r v_x q = \left(\frac{\mu I l}{2\pi x(l-x)}\right)\{\sqrt{2xa_x}\}q \,, \tag{3}$$

where F_M is the Lorenz force perpendicular to the carrier flow direction, v_x is the carrier speed in the direction of the MAGFET current flowing from the source to drain, B_T is the overall magnetic induction of the metallization loop, q is the carrier charge, x is the position of the carrier in relation to the MAGFET source, l is the channel

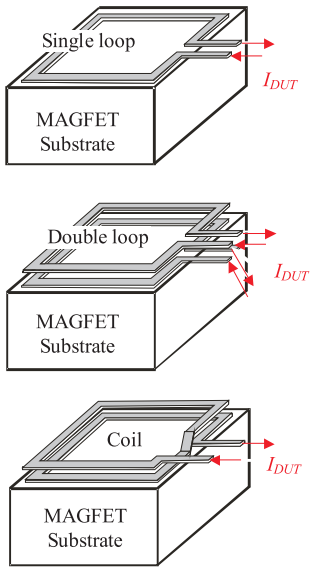

Fig. 4. Metallization supply line variations

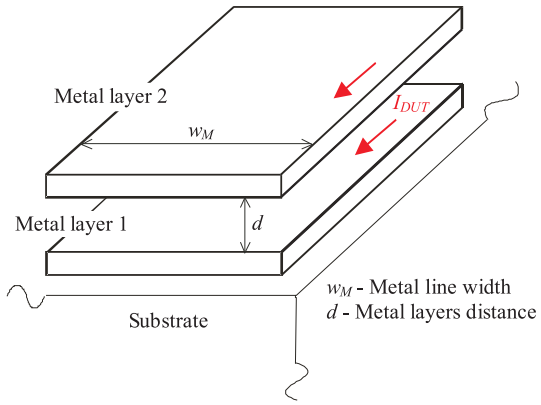

Fig. 5. Schematic view of doubled metal layer supply line

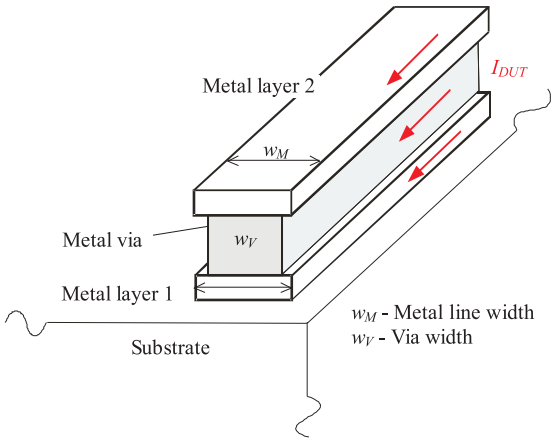

Fig. 6. Schematic view of supply line with metal layers connected by via

length and (lx) is the position of the carrier in relation to the MAGFET split drains, a_x is the acceleration of carrier in the direction of the MAGFET current.

With higher carrier deflection a higher sensitivity should be obtained. Thus, the sensitivity S of the MAGFET sensor could be defined as follows:

$$S = \frac{\Delta I}{I_0}, \tag{4}$$

where δI is the current difference between two drain currents of the MAGFET in the presence of B_T, and I_0 is the total drain current in the absence of B_T. The sensitivity S is a function of geometry factors as well as the biasing conditions of V_{GS} and V_{DS}.

In the first phase of MAGFET structure design research, both N-channels and P-channels were used, however, the P-channel structures present higher noise and lower carrier mobility. In order to enhance the sensitivity and minimize the impact of external magnetic field sources, the designed structures consist of two crossed paired structures of N-channel and P-channel MAGFET transistors. The MAGFET structures were sized to provide approximately the same conductance for the P-channel and N-channel devices. Transistor drains were connected in a way, where for a given magnetic field, the drain of one channel type (P) device with increased current is connected to the drain of the other channel type (N) device with decreased current, and vice versa. The applied bias voltage V_B defines the current magnitude and needs to be kept at the level, where the current reaches its maximum value. The higher current flowing through the source, the higher sensitivity of the sensor could be reached.

The second phase of MAGFET research is based on the results achieved in the previous phase. Differently shaped structures were proposed and designed, most of them in the sector form. An illustrative example of the structure shape is illustrated shown in Fig. 3. The aim of this phase was mainly to increase the sensor sensitivity. Since the P-channel MOS present higher noise, the new sector structures are either N-channel MAGFET structures, or structures using solely electrons as the charge carriers. The close touch of metallization and the active area is present again in order to increase the transversal magnetic induction as much as possible.

As the metallization supply line surrounds the chip, it creates magnetic induction, impacting on the carriers in channel. The shape of the metallization supply line is advantageous but, on the other hand, since it represents a loop or several loops, it might be invasive to the DUT because it could act as a parasitic filter. The shape of the metallization supply line could be built in several ways. Figure 4 illustrates possible variations of the metallization line design. As the two-loop (with the cross section illustrated in Fig. 5) coil generates advantageously higher magnetic induction than the one loop solution, this architecture is considered as good one. Although, it might be on the contrary disadvantage as being more invasive in terms of generated electric induction. Another disadvantage of the double-loop architecture is that the metal line should be dimensioned to withstand the high current

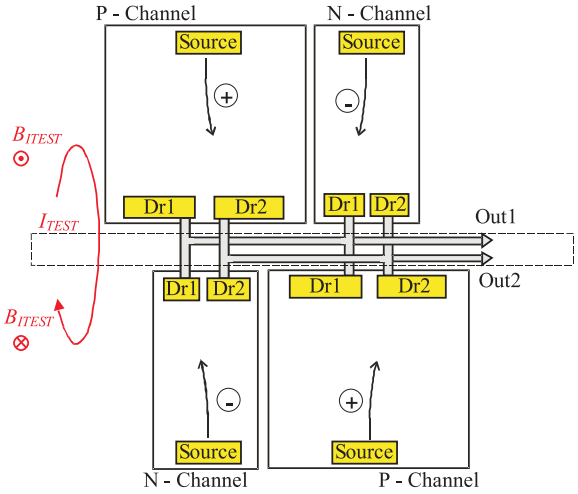

Fig. 7. Crossed coupled sensor architecture

drawn by a DUT (metallization twice bigger). This would affect the total size of the MAGFET structure because the metallization supply line covers at least over one third of the structure size. An interesting construction could be via an element between two or more metallization layers, since via itself withstands much higher current density per width unit (Fig. 6). This solution would substantially reduce the area of the magnetic sensing structure and make the cross-section more compact and the induction more homogenous.

One of the drawbacks of this sensor is its noise sensitivity. Two most significant types of electric noise appear in CMOS transistors. White noise, dependent on temperature, appears at any conditions (frequency, voltage, etc.) in semiconductor structures. The flickering noise is a function of frequency $(1/f)$ and mostly disappears at high frequencies. The electric noise is though not the only distortion source of the structure. The magnetic noise generated either by the earth or any other artificial source cannot be completely neglected. The values of external magnetic field (ground magnetic field, magnetic noise generated by devices in proximity of the sensor), however, reach around tens up to hundred T, so the field of the earth is basically weak enough to impact the sensor. Therefore, the magnetic noise sensitivity is narrowed to the magnetic induction generated by additional surrounding sources. The MAGFET output noise can be rather invasive and the results distorted.

Other two kinds of distortion sources in the design have to be taken to account. Firstly, there is an offset, introduced into the sensor signal because of the fabrication process variations. For example, the mismatch of the split drains will introduce an offset both in the presence and in the absence of magnetic field. Secondly, in the signal processing units, necessary either for MAGFET itself or additional circuitry function, the noise of the circuits might affect the sensor signals. To prevent this, there are several possibilities of noise cancellation that could be used.

Although simulations, based on spice models, may show relevant results at unidirectional magnetic field oriented transversally to the sensor, there is no relatively precise spice simulation of the real shape of sensors. However, rough results could be brought by structural simulators able to work with unidirectional magnetic fields.

3 SENSOR PART DESIGN AND MEASUREMENTS

First version of the sensor

A precise layout implementation of the proposed structures represents a very important part of the overall sensor design, since it strongly impacts the carrier deflection dependence on the magnetic field and the distortion caused by parasitic elements. The first version sensors were designed and fabricated in 1.0 μm BiCMOS technology with a single poly and triple metal layers. The second version of the sensor was realized in 1.0 μm BiCMOS technology, featuring a double poly layer and a double metal layer. As shown in Fig. 7, in the first sensor version, two P-channel and N-channel MAGFETs were organized in a cross-coupled structure in order to obtain higher current sensitivity and higher voltage gain, and to compensate the impact of the unidirectional parasitic magnetic field. In such a structure, the current differences between the two outputs are added to generate $2\Delta l$ I. On the other hand, the parasitic differential current caused by the parasitic magnetic field in one P-channel and N-channel couple, eliminates the parasitic current generated in other P-channel and N-channel couple. The common bias current I flows from the P-type to the N-type MAGFET. Each MAGFET is biased to be in saturation that enables maximum current flowing through the transistors.

Dimensions of selective N-channel MAGFET transistors are in the range from 50 to 250 μm. P-channel W/L dimensions are between 50 to 500 μm. The sensor uses regular transistor structures with a drain divided into two parts. Since the simulation results in [4–9] show that the size of the drain gap has no significant impact on the sensitivity, the gap was built as narrow as 3 μm. The metallization supply line is laid out in the first metal layer, so the distance of the current line and carriers to be deflected in the channel was minimized in two ways – using maximum enclosure of the channel vertically as well as horizontally. Three dimensional variations of this cross-coupled structure were placed on the test chip, each in different orientation. A low-pass filter was connected to all the outputs of these three various structures to cancel the noise appearing above a certain frequency level. The filter consists of two capacitors with capacitance of 45 pF integrated together with two resistors of the same size to filter frequencies above 1.5 kHz. Because of the large size, the remaining four capacitors necessary for the remaining filters are to be connected externally. Two filtered outputs of the third cross coupled MAGFET structure proceed to an integrated signal processing unit. The

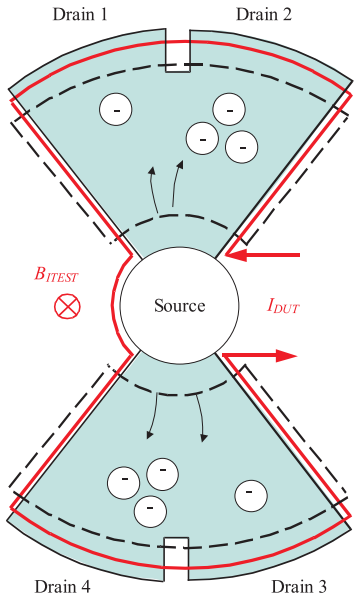

Fig. 8. MAGFET sector couple

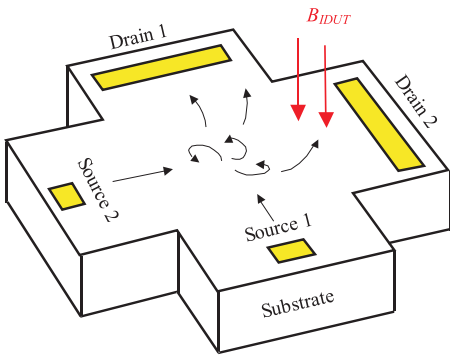

Fig. 9. Magnetic force sensing cross structure

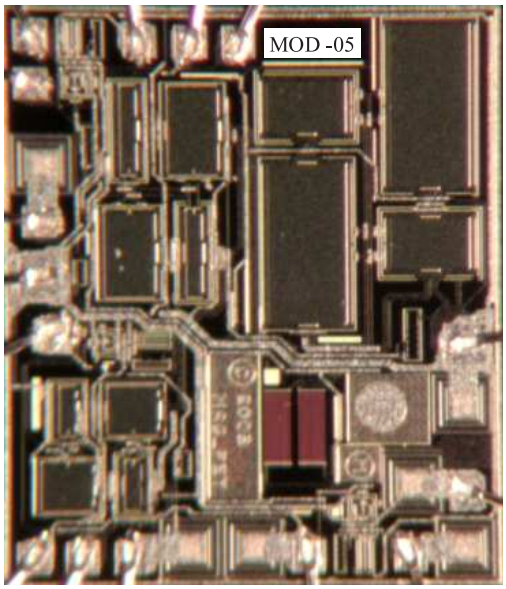

Fig. 10. Test chip microphotograph

outputs of crossed-coupled sensor cells lead towards additional signal processing circuitry implemented on chip.

Second version of the sensor

In relation to the results, acquired on the fabricated test chip of the first version design, several specially shaped MAGFET structures were designed in order to improve the sensitivity and define the most proper sensor dimensions. The sensitivity of MAGFET depends on several aspects. Sensitivity is primarily higher when the lateral width of the source region is reduced [10–11].

The sector MAGFET structures, described in this section, have basically the shape shown in Fig. 3. Parameters having a primary impact on the overall sensitivity are: channel length in radial direction L, radius of source region R, and the extension angle of source region α. Secondary impacting parameters are: the gap between two drain regions d, overlaps of poly-silicon gate at source and drain region u. All the structures were designed in 1.0 μm BiCMOS technology with dual poly and dual metal layers. Because of already mentioned higher noise and lower carrier mobility of p-channel MAGFET, an n-channel MAGFET structures were selected for the sensor design. Every sensor cell is composed of two MAGFET structures, which are in advantageous up and down connection, particularly in connection with common source. The split drains of these structures are in opposite sides. As the source to drains direction of the first and second transistors is opposite, the direction of carriers' motion is opposite as well. In the case of a homogenous magnetic induction, being generated by the metallization of the supply line, the carrier deviation direction is inverse as well. Therefore, when the drains of the two opposite transistors are connected diagonally (Fig. 8), the difference in the split drain currents is doubled. The supply line of metallization is placed in same manner as described in the first phase of the experimental work.

Most of the sensor cells have a coupled sector structure, although different geometry cells were designed as well. A single sector transistor is provided as a comparison target to the coupled sector transistor cell, so that the sensitivity of a single and couple cell transistor could be compared. Two rectangular structure cells were also designed as a sensitivity target. The first rectangular structure represents the same principle as the coupled sector cell, thus, the sensitivity difference might be evaluated. The other rectangular structure represents the same geometrical shape, however, the principle is different. The active layers of the cell consist of an n-well. In order to obtain as high concentration of carriers as possible (and as close as possible to the surface), a polysilicon gate covers the active area. Dense concentration of carriers in the region close to the magnetic induction, generated by the metallization supply line, will cause more carriers to deviate.

A cross structure as another non-sector cell was designed as well, as show in Fig. 9. The deviation is based on the spinning current offset cancellation technique, which requires a structure that is invariant to rotation by 90°.

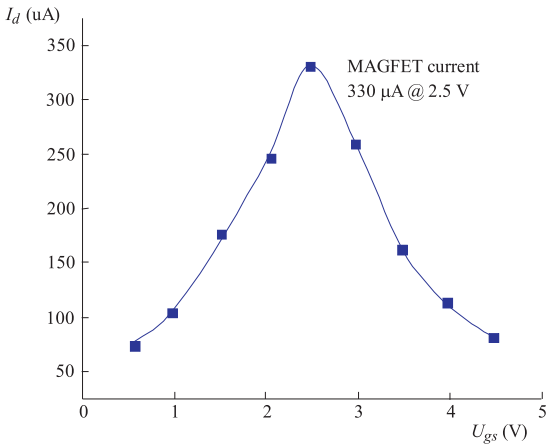

Fig. 11. MAGFET cell drain current vs. gate voltage

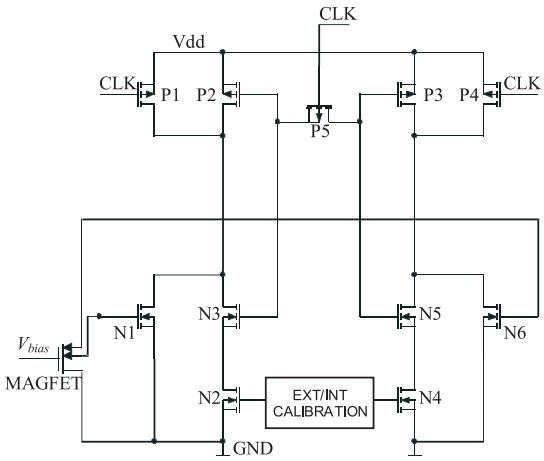

Fig. 12. Principal schematics of the stochastic sensor

The spinning current originates in the area, where two channels meet each other and the two current streams cross. The current is influenced by the magnetic induction and the carriers tend to deviate in dependence on the transversal magnetic induction direction and magnitude.

Figure 10 shows a microphotograph of the test chip of the size of 1.58 mm × 1.89 mm, which obtains 3 different double geometric n-channel sector sensor cells, one single cell sector sensor, a cross structure, and one rectangle sensor cell regarded as comparison target. The remaining area of the chip consists of evaluation circuitry pads, covering most of the area. The evaluation circuitry, designed for MAGFET testing differs from the circuitry implemented on the chip within the first phase of the sensor design. None of the cells is connected to any circuitry directly, and is to be connected externally. As long as the off-chip connections are short enough, noise generated by the antenna effect can be neglected. The chip evaluation circuitry described bellow, was designed and integrated on the same chip to provide a reliable small current sensing method. However, it needs to be connected externally using the dedicated pads.

4 TEST CHIP EVALUATION RESULTS

Several methods of MAGFET output signal processing and evaluation can be used. Two basic principles, current and voltage approaches, may be applied at a highest possible level of the drain current, as shown in Figure 11. After amplification of the signal using a differential amplifier, the nature of voltage dependence on the magnetic induction should become linear. However, this method might not be useful because for very small currents flowing through the metallization supply line to the DUT, the signal to noise ratio level may reach values deeply below 1. Therefore, another principle of low voltage evaluation was used. The regular differential amplification method could be carried out by discrete components externally, connected to test pads on the chip, while the on-chip stochastic test analysis should necessarily be integrated. In order to achieve a higher resolution and to detect smaller signal changes, a single stage using a flip-flop initialized to its metastable state was designed and implemented (Figure 12)

The output voltage signal is compared with the background noise to determine whether the flip-flop should resolve to a low or a high logic level. Thus, this circuit operates even when the signal is smaller than noise. The signal is repeatedly measured as many times as needed to ensure preciseness of the measurement. The resulting digital bit stream is fed into a microprocessor in order to form the voltage to magnetic induction dependence.

The circuit, shown in Fig. 12, operates in the following manner. When the clock is low and the inverted clock is high, the two flip-flop nodes equalize to an intermediate voltage. When the clock rises high, the flip-flop goes into the metastable state. Noise will flip it one way or the other. The calibration circuit ensures that when no input is present, the flip-flop has equal probability of flipping one way or the other. The differential MAGFET causes a slight imbalance on the nodes, biasing the flip-flop decision. Stochastic analysis is based on the stochastic evaluation of binary data coming from the binary decisions made when the flip-flop compares the input signal with random noise. The number of samples to estimate the signal by stochastic operation is dependent on the SNR. The higher is the SNR, the higher the number of samples is needed. The drawback of this method is the calibration, necessary to be made on each chip separately. This is a process, where at each magnitude of the current, the number of flips is counted and the calibration curves are subsequently created. Calibration can be done externally, or by an additional on-board circuitry.

As for practical measurements, external pads were used to determine the outputs signal difference. As previously expected, the difference voltage got below the threshold level of the amplifier and, thus, it could not be measured. Therefore, the implemented stochastic signal processing method was used. A dedicated PCB board was designed to evaluate the output of the flip-flop of the built-in signal processing and the evaluation unit. The test board comprised the additional circuitry and

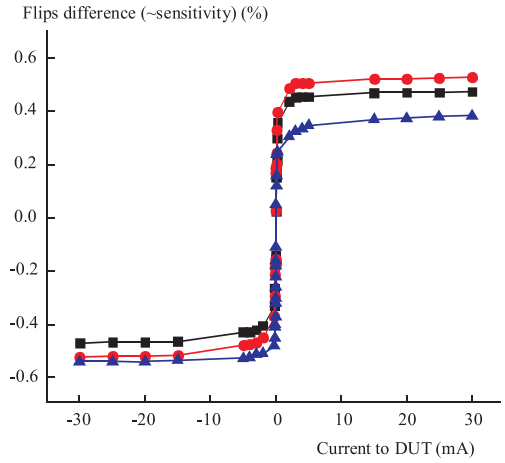

Fig. 13. Flips difference (sensitivity) diversity of different MAGFET cells

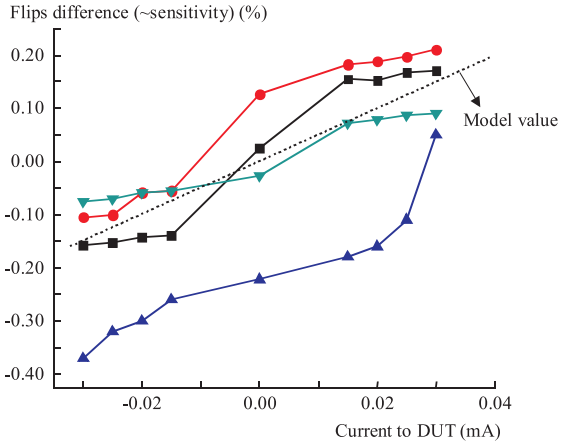

Fig. 14. Flips difference (sensitivity) diversity of single MAGFET cell selective measurements and model value at small scale current flow to DUT

the microprocessor. Using the processor, the external self calibration was programmed. The evaluation board automatically stores data of the stochastic evaluation sensor and sends the data to PC. Data might be, thus, latter processed and evaluated using a computer.

Ten fabricated chips were measured by these two techniques. As already mentioned, the first method, using a differential amplifier, could not sense the signal possibly because of high noise and high offset level. Using the stochastic evaluation method, the following evaluation results were observed. Firstly, a calibration voltage measurement is necessary to balance the two flip-flop outputs. Hence, to approximately balance the number counts on the first and second output. Afterwards, several sensitivity tests on each chip with different current flowing through the metallization were carried out. Every chip was measured under different conditions in different environment. The measurement took place in a regular laboratory, in a special EM shielded lab, and finally, in a special closed EM shield. Although the surrounding magnetic properties changed, the impact on the MAGFET sensitivity was not measurable. The output curves differed from each other respectively with different chips, as illustrated in Fig. 13.

Strong individual properties on different chips were observed. Besides this, a variation of the measured output curve occurred even within the same chip under the same conditions. As the curves were similar to each other but never matched, it could be assumed that EM noise, brought to the sensor by the circuitry itself, influenced the output signals and the sensing method. As shown in Figure 13, the approximate sensitivity is measurable particularly in the region of higher magnetic induction. Thus, the sensitivity of this method is good enough for sensing currents over several tens of milliampers, however, measuring of very small current would not be applicable by this evaluation method as resulting from Fig. 14. While voltage measurement is very sensitive to any kind of noise, current sensing methods tend to be less distorted. Such a method for measuring very small currents is described further. Although the electric and magnetic noise might affect the immediate current output, the noise affect will be minimized using long time integration of the signal. The principle of the proposed current measurement is based on several current mirrors, as illustrated in Fig. 15. The current difference ($\Delta I = I_1 I_2$) between two drains is mirrored into the output branch. An offset of the sensing MAGFET cell could cause the current to flow to or from the differential amplifier, while no current will be drawn by the DUT. This can be solved either by an additional couple of transistors eliminating the offset, or by a method that will set the actual current as the reference value and compare the real time current magnitude to the reference. A calibration process is needed in this method as well. The calibration curve represents the dependence of current drawn by the DUT on the current flowing out to the differential amplifier and, thus, the dependence on the magnetic induction.

The very precise current test method described above requires a small modification, if used for evaluation of the first phase MAGFET sensors. The two outputs were both connected to the active integrator, where the voltage integrated on the capacitor represents the voltage difference on both outputs. Taking into account the fact that the outputs were designed as voltage ones, the sensitivity of the evaluation circuit is rather low however, the results prove the expected shape of the output curves.

The solution using current mirrors to measure the current was proposed to be used in the evaluation of the second version of the chip. In this design version, sensor cells are not connected directly to any evaluation circuit, and all the inputs and outputs will be terminated either by bonding or probe pads. Thus, any of the MAGFET output signal evaluation methods might be used. The primarily expectation of this sensor version is, in comparison to the results obtained in the previous phase of this research, higher sensitivity and lower current threshold value measurable.

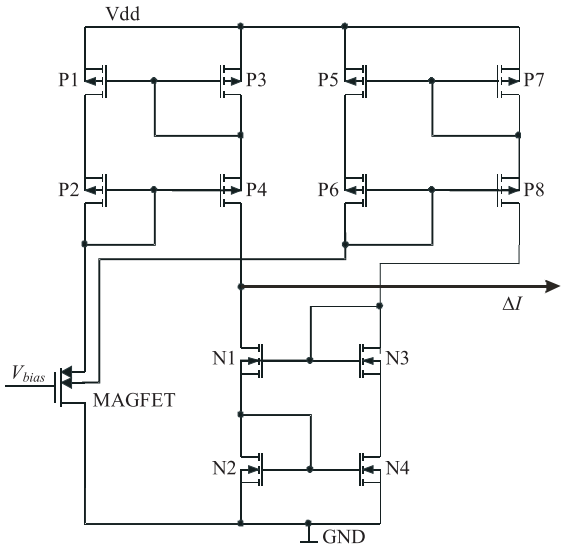

Fig. 15. Principal schematics of the proposed current difference ΔI evaluation block

5 DISCUSSION

The results obtained during measurements of the first phase MAGFET cells proved the expected sensitivity of the split drain structure and possibility of its utilization in the area of deep-submicron current testing. However, it is of great importance to define and design proper geometrical parameters to achieve the best ratio of sensitivity to the sensor cell size. This is only marginally satisfactory in the case of traditional rectangular MAGFET, which results from the measurements, and higher sensitivity would be appreciated. It could be caused by several factors, such as very wide source, where too few carriers appear in the sensitive area of the structure axis and, thus, very a low number of these is deviated. The narrower is the source, the more focused is the stream of carriers and the higher sensitivity is observed. A very short channel could as well cause that the deviation of carriers at the end of the channel is insufficient. A very small current flow through the structure cell might as well strongly affect the sensitivity.

There are naturally other impacting factors and, therefore, the second phase of MAGFET research was initiated and modified sensor cells were designed in order to eliminate the distortion elements. These cells, therefore, should offer a higher sensitivity with a at lower area of taken by the sensor.

6 CONCLUSION

A new approach to built-in current testing has been proposed and the current sensor based on a dedicated MAGFET structure has been developed and fabricated. Given by the sensor cells principle, the proposed sensor is considered as very useful in very low-voltage applications, since there is no power supply voltage perturbation observed. Three MAGFET structures of various dimensions were designed and implemented on a single chip in the first phase of the MAGFET research in order to investigate general and specific properties of various sensor sizes and define their selective sensitivity. Moreover, the measurement board and additional signal processing unit was developed to evaluate the overall feasibility of the proposed approach.

As the MAGFET research progresses, there is a sector MAGFET sensor compatible with BiCMOS technologies suggested in this paper, as the second phase research. The motivation of this phase was to achieve higher sensitivity and, thus, lower currents of the DUT measurable. Sensors alike could be in the future regularly used as a library components and built-in self test components on the chip. The sector and non-sector cells are primarily focused on geometric parameters such as the channel length, radius of source region, and the angle of cell if the sector structure is used. It is obvious, that in comparison with rectangular MAGFET sensors, a higher sensitivity could be reached by various shape structures. However, to confirm the theory, a necessary practical sensitivity evaluation has to be done.

As the chip of the second phase design was not fabricated yet at the time of the paper submission, for the next work, new test programs debugging and the new sensor cells evaluation will be carried out in a short time period in order to accomplish the main goals of our work. The methodology of MAGFET current cell adjustment technique for specific CMOS and BiCMOS technologies will be carried out as the final step of the research.

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