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A NEW TYPE OF CURRENT CONVEYOR AND ITS APPLICATION IN FULLY BALANCED DIFFERENTIAL CURRENT–MODE ELLIPTIC FILTER DESIGN

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This paper introduces a new type of CMOS-based current conveyor: current controlled fully balanced second generation current conveyor (CFBCCII) element which has a pair of differential Y terminals, a pair of differential X terminals and two pairs of Z terminals. The proposed circuit offers electronic tuning possibilities by means of a current adjustable intrinsic resistance at its X terminal. An elliptic filter realization is described as an example for its application in a current-mode fully balanced filter design, where the intrinsic resistors in CFBCCIIs are used for the electronic tuning of the characteristic filter frequency.

K e y w o r d s: current mode, differential, current conveyor, elliptic filter

1 INTRODUCTION

The interest in designing current-mode circuits mainly emanates from their speed advantages, higher bandwidth, wider dynamic range, and relatively simpler circuitry [1–8]. Current conveyor (CCII) element and its modifications can be used in single-ended [1–7] or differential filters [8]. Differential current mode filters play an important part in telecommunications due to their ability of suppressing even harmonics, as well as common-mode interference. In a previous work, Chiu *et al* proposed a differential difference current conveyor (DDCC) and a second-order filter which can realize low-pass and band-pass filtering function [9]. In 1997, Elwan *et al* proposed two CMOS-based differential voltage current conveyor (DVCC) circuits [10], and this element found wide applications [11]. A fully differential current conveyor (FDCCII) [12] presented by El-Adawy employs fully differential structure to suppress undesirable common mode signals, and it has two X terminals and four Y terminals. A new realization of FDCCII was proposed by Soliman [13], and the terminals X, Y and Z of this circuit are all differential.

In modern VLSI applications, balanced-mode structures are increasingly used. In a balanced circuit, output common mode (CM) signal is kept constant, and it is entirely independent of the input signal. Therefore, performance of a fully balanced structure (such as dynamic range, noise suppression, and harmonic distortion) can be largely improved. A fully balanced current conveyor proposed in [14] provides a pair of differential Y terminals and a pair of differential X terminals. The circuit introduces two common-mode feedback CMFB circuits which keep the common mode signal constant, while increasing the dynamic range of differential mode signals. In 2004, Alzaher introduced a CMOS fully differential current conveyor [15] also including two CMFB circuits. However, in all of these previously reported elements, there exists a relatively significant voltage tracking error from terminal Y to terminal X. This is because of the parasitic resistor in terminal X which leads to transfer function error in their application circuits. Several CCII circuits with reduced resistance in terminal X have been proposed these years [16–18], the CCII circuits in [16] and [17] result small input resistances in terminal X, the circuit in reference [18] employs four transconductance amplifiers, which makes circuit complicated. Although the above three circuits minimize the voltage tracking error in conventional CCII, these elements lack electronic programmability, which has become a key feature in recent applications.

In 1996, Fabre proposed a current controlled current conveyor (CCCII) [22] constructed by a bipolar translinear loop, by introducing the intrinsic resistor, this circuit can rectify the transfer error between X and Y terminals, at the same time, the intrinsic resistor in X terminal can be adjusted by the bias current. However, it has a crucial disadvantage of having only one high input voltage terminal, which is not convenient to process differential or floating signals.

Differential or balanced CCCII is more attractive in application, since they are more sophisticated in dealing with differential and floating signals. In 2005, a CMOS CCII was proposed in [20], this circuit has a pair of differential voltage inputs (Y_1 and Y_2), one current input (X), and two differential current outputs (Z_+ and Z_-), it can reduce the harmonic distortion in some extent and can be integrated conveniently in CMOS technology. However, this circuit is not fully differential realization since X terminal is not differential, moreover, the circuit does not employ CM feedback (CMFB) circuit which can ensure the output signals symmetric and

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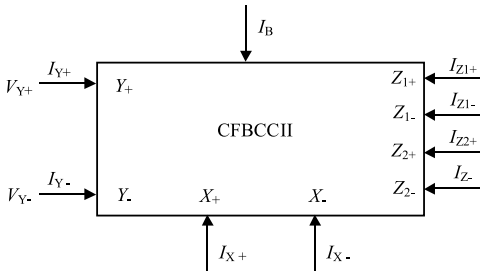

Fig. 1. Symbol of CFBCCII

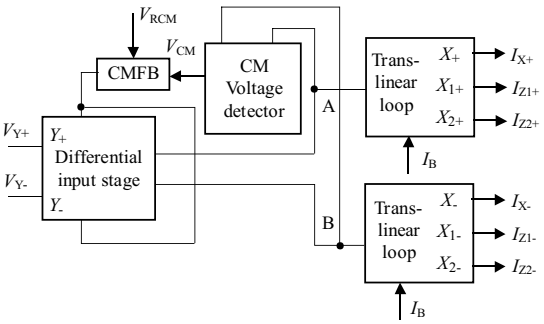

Fig. 2. Frame diagram of CFBCCII

make the CM signals independent of the input signal [15]. In 2006, a CMOS current controlled balanced integrator is presented in [21], this circuit is constructed by two CMOS translinear circuits and two floating capacitors, it has two differential voltage inputs and two differential outputs, but the current signal in X terminal can not be made differential, therefore, this circuit is not in fully balanced structure, moreover, the capacitors of the integrator are not grounded, and this would leads to large chip area when integrated in CMOS technology. The balanced tunable current conveyor presented in [19] has one voltage input, two differential current inputs, and two differential current outputs. The circuit introduced current tunability in terminals X and Z by changing the drain width of MOS transistors in the current mirrors, in this way, the current gain between terminal X and Z would be tuned. Obviously, the circuit is not fully balanced yet since terminal Y is single ended. Moreover, this circuit just realizes the controllability the current relationship between X and Z, but does not realize the controllability of the voltage relationship between Y and X, the voltage transfer error still exist. So its applications are limited.

On the other hand, the advantages of elliptic filters are well known, no other filters of equal order can have a faster transition in gain between the passband and the stopband, for the given values of the ripple, therefore, the selective character of elliptic filter is very attractive [23–28]. Various OTA based [23–25] elliptic filters were presented. However, the linearity and dynamic range of OTA based filters are not as good as CCII-based filters. On the other hand, the CCCII-based filters not only have better linearity, but also have easier electronic frequency adjusting characteristics. There are three different methods to implement analogue filters: cascade, multiple loop feedback (MLF), and LC ladder simulation. The LC ladder simulation has the lowest sensitivity and low component spread among the three methods.

This paper proposes a new element, so called a current controlled fully balanced second-generation current conveyor (CFBCCII) which employs a fully balanced structure to suppress common-mode signals. Compared with the circuit in [20], the proposed CFBCCII uses the fully balanced structure, and employs CMFB circuit to prevent the drift of CM signals. CFBCCII is also different from the circuit in [21], since all terminals of CFBCCII are differential, moreover, when connected as an integrator, the capacitors in the circuit can be grounded. By introducing a current adjustable intrinsic resistance at X terminal, CFBCCII eliminates the transfer error between X and Y terminals, moreover, it introduces the electronic tunability for itself and application circuits. So CFBCCII is different from the circuit in [22] in the manner of controllability, CFBCCII controls the voltage relationship between X and Y terminals, while the circuit in [22] controls the current relationship between X and Z terminals. Moreover, all terminals of CFBCCII are differential, while Y terminal is not differential in [22].

Based on the proposed element, this paper presents a fully differential current-mode elliptic filter realized by using signal flow graph approach to simulate a passive low-pass ladder network. The proposed filter employs 7 CFBCCIIs, and it has the frequency tuning characteristic by adjusting the bias current of the active block.

2 CFBCCII CIRCUIT AND ITS CMOS REALIZATION

The circuit symbol of CFBCCII is shown in Fig. 1. Here, Y_+, Y_- are differential voltage input terminals exhibiting high input resistance. X_+ and X_- behave as differential voltage tracking terminals, Z_{1+}, Z_{2+} and Z_{1-}, Z_{2-} are the current output terminals, the differential current at terminal Z is a replica of the differential current at terminal X. The number of current output terminal Z can be extended if necessary. I_B denotes bias current of CFBCCII. The port characteristic of CFBCCII is represented by (1), $R_X = f(I_B)$ denotes the controlled resistance which can be tuned by I_B.

$$\begin{aligned} &I_{Y+} = I_{Y-} = 0\,, \\ &V_{X+} - V_{X-} = (V_{Y+} - V_{Y-}) + (I_{X+} - I_{X-})R_X\,, \\ &I_{Z1+} - I_{Z1-} = I_{Z2+} - I_{Z2-} = I_{X+} - I_{X-}\,. \end{aligned} \tag{1}$$

The circuit frame diagram of CFBCCII is given in Fig. 2. The circuit is made up of four blocks: The differential voltage input stage, the translinear loop [20], common mode (CM) voltage detector, and the common mode feedback circuit (CMFB). The basic principle of the circuit is analyzed as follows: There are two signal-feed

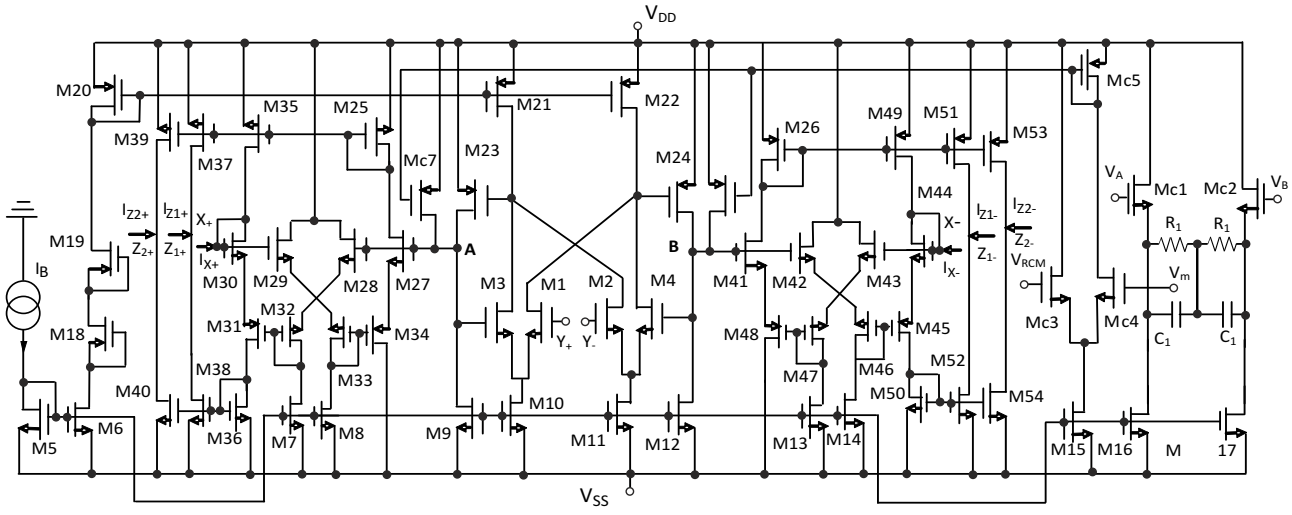

Fig. 3. Circuit realization of CFBCCII

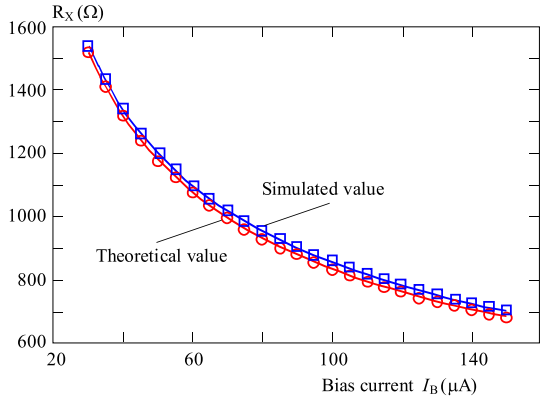

Fig. 4. Simulated relationship between R_X and I_B

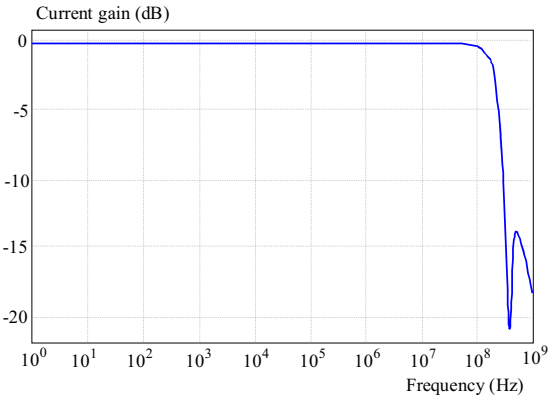

Fig. 5. Frequency response of Z–X current gain

paths in the circuit, the feedforward path, and the feedback path. The feedforward path consists of a differential input stage and two translinear loops. Differential voltage signals are added to the differential input stage, and the voltages would be transferred to the points A and B. The translinear loops are employed to transfer V_A and V_B to the output terminals. The feedback path consists of CM voltage detector and CMFB circuit. The voltages at the points A and B will be sampled by the CM voltage detector, where the common-mode (CM) voltage V_{CM} is generated. The CMFB circuit is employed to suppress the CM signals, by comparing V_{CM} and V_{RCM}, V_{CM} is forced to follow $V_{\mathrm{CM}} = V_{\mathrm{RCM}}$, in this way, the CM signal can be effectively suppressed. Here, I_B is bias current of translinear loop.

The realization of the CFBCCII circuit is illustrated in Fig. 3. M1-M4 constitute two pairs of differential inputs, the parameters of the transistors are symmetric. Y_+ and Y_- are differential voltage input terminals. The two pairs of differential transistors are loaded by M10-M11 which carry equal bias currents I_B. M27-M34 and M41-M48 constitute two CMOS translinear loops, M27-M34 transfer the voltage from point A to X_+, and M41-M48 transfer the voltage from point B to X_-. Now consider the translinear loop of M27-M34: M27 and M34, M28 and M32, M29 and M33, M30 and M31 constitute four compound transistors respectively. If the channel aspect ratios W/L of NMOS transistors in the four compound transistors are identical, and the ratios W/L of PMOS transistors are alike (all transistors operate in saturation region), one can get [26]

$$R_X = \left(2\sqrt{2K_{eff}}\sqrt{I_B}\right)^{-1} \tag{2}$$

where $K_{eff} = K_n K_p / \left(\sqrt{K_n} + \sqrt{K_p}\right)^2$ represents the compound transconductance coefficient of the compound transistors, K_n and K_p are the transconductance coefficient of the NMOS and PMS transistors respectively. R_X represents the parasitic resistance of terminal X, which is inversely proportional to the square root of bias current I_B. Namely R_X can be adjusted by bias current I_B.

To verify the proposed circuit performance, CFBCCII shown in Fig. 3 is simulated using HSpice program. 0.35 μm CMOS technology parameters are used. The dimensions of MOS transistors are listed in Table 1. Supply voltages used are ± 1.65 V. Figure 4 shows the relationship between R_X and bias current I_B, the comparison

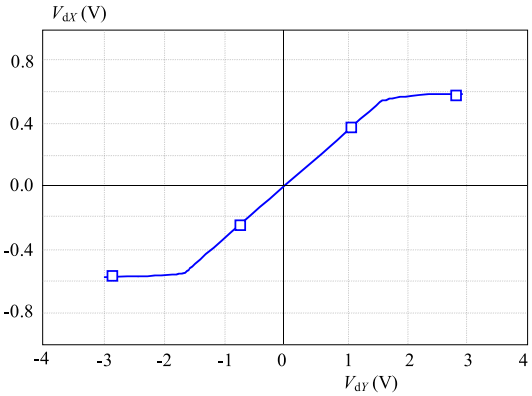

Fig. 6. Simulated Y–X DC characteristic

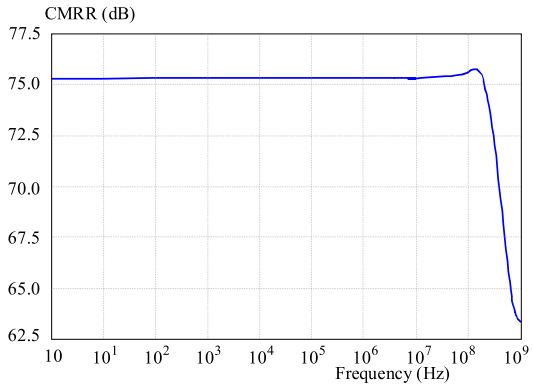

Fig. 7. Simulated CMRR of CFBCCII circuit

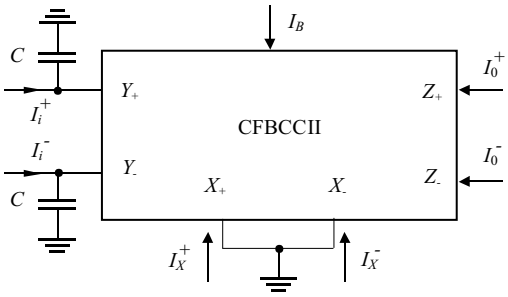

Fig. 8. CFBCCII based integrator

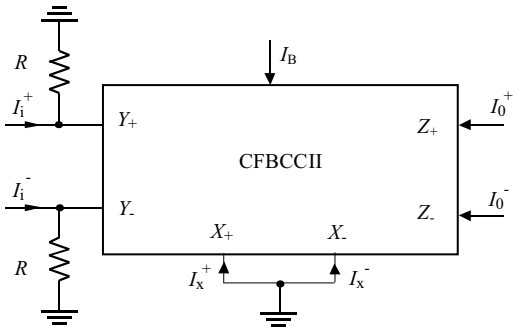

Fig. 9. CFBCCII based scaling circuit

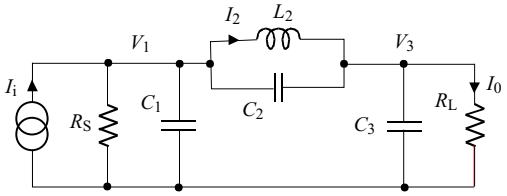

Fig. 10. The 3rd-order elliptic low-pass RLC ladder filter

Table 1. Dimensions (W/L) of MOS transistors in CFBCCII (μm)

MOS Transistors	W/L (μm)	MOS Transistors	W/L (μm)
M1∼M4	2/0.35	M5-M14	16/0.35
M15	80/0.35	M16-M17 M18-M19	10/0.35
M20-M22	14/0.35	M23, M24	20/0.35
M25-M28 M40-M43	10/0.35	M29-M32 M44-M47	40/0.35
M33-M36 M48-M51	80/0.35	M37-M39 M52-M54	4/0.35
Mc1-Mc4	1/0.35	Mc5-Mc7	2/0.35

of the theoretical result and the simulated result are also given. Bias current varies from 30 μA to 150 μA, while R_X varies from 700 Ω to 1540 Ω. Figure 5 shows the current transfer characteristics $(I_{Z+} - I_{Z-})/(I_{X+} - I_{X-})$ when nodes Y_+ and Y_- are grounded, an excellent bandwidth with -3 dB cutoff frequency of 200 MHz can be obtained. is consistent with the differential input current $(I_{X+} - I_{X-})$. Figure 6 shows the simulated DC transfer characteristic between Y terminals and X terminals, $V_{dY} = V_{Y+} - V_{Y-}$, $V_{dX} = V_{X+} - V_{X-}$, the transfer characteristic between Y and X ports can be written as: $V_{dX} = V_{dY} + (I_{X+} - I_{X-})R_X$. Bias current is 50 μA. It is seen that the linearity input range is almost 3 V. Simulated common mode reject ratio (CMRR) of this circuit is illuminated in Fig. 7, it shows that this circuit has a CMRR value of 75.2 dB, and we can see that the circuit can reduce the undesirable common mode signals in a certain extent.

3 CFBCCII BASED SUB–CIRCUIT FOR THE PROPOSED FILTER

3.1 Integrator

Figure 8 shows the integrator based on CFBCCII. Routing analysis yields

$$I_0^+ - I_0^- = I_X^+ - I_X^-\,,$$
$$(I_i^+ - I_i^-)\frac{1}{sC} + (I_X^+ - I_X^-)R_X = 0\,.$$

The transfer function can be written as:

$$H(s) = \frac{I_0^+ - I_0^-}{I_i^+ - I_i^-} = -\frac{1}{sR_XC}\,. \qquad (3)$$

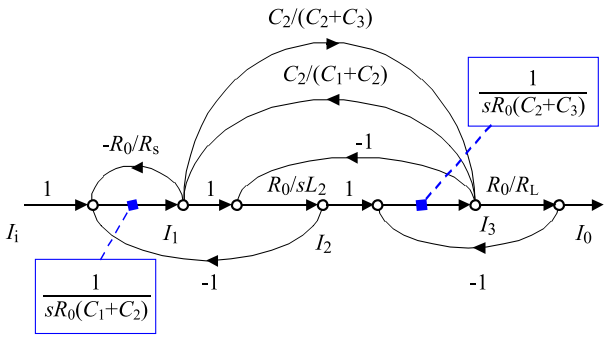

Fig. 11. Signal flow graph of the 3rd-order elliptic low-pass RLC ladder filter

3.2 Scaling Circuit

The CFBCCII based scaling circuit is shown in Fig. 9, whose transfer function is

$$H(s) = \frac{I_0^+ - I_0^-}{I_i^+ - I_i^-} = -\frac{R}{R_x}. \tag{4}$$

4 THE PROPOSED FILTER

4.1 Design of The Filter

Figure 10 shows the low-pass third-order passive LC ladder filter. The proposed elliptic filter can be designed by simulating the transfer functions in the SFG using the integrator and scaling circuits based on CFBCCII. From Fig. 10, one can get the state equation represented as follows

$$V_1 = \left[I_1 - I_2 - (V_1 - V_3)sC_2 - \frac{V_1}{R_s}\right]\frac{1}{sC_1}, \tag{5}$$

$$I_2 = (V_1 - V_3)\frac{1}{sL_2}, \tag{6}$$

$$V_3 = \left[I_2 + (V_1 - V_3)sC_2 - \frac{V_3}{R_L}\right]\frac{1}{sC_3}, \tag{7}$$

$$I_0 = \frac{V_3}{R_L}. \tag{8}$$

Converting the voltage signals into current signals by dividing a virtual resistor R_0, and $V_1 = I_1 R_0$, $V_3 = I_3 R_0$, the state equations can be rewritten as

$$I_1 = \frac{I_i - I_1(R_0/R_S) - I_2}{sR_0(C_1 + C_2)} + \frac{I_3 C_2}{C_1 + C_2}, \tag{9}$$

$$I_2 = (I_1 - I_3)\frac{R_0}{sL_2}, \tag{10}$$

$$I_3 = \frac{I_2 - I_3(R_0/R_L)}{sR_0(C_2 + C_3)} + \frac{I_1 C_2}{C_2 + C_3}, \tag{11}$$

$$I_0 = I_3\frac{R_0}{R_L}. \tag{12}$$

According to the equations (9)–(12), the SFG can be obtained shown in Fig. 11. Substituting the scaler and integrator with CFBCCII based sub-circuits which have been analyzed in Section 3, the proposed filter is obtained as shown in Fig. 12.

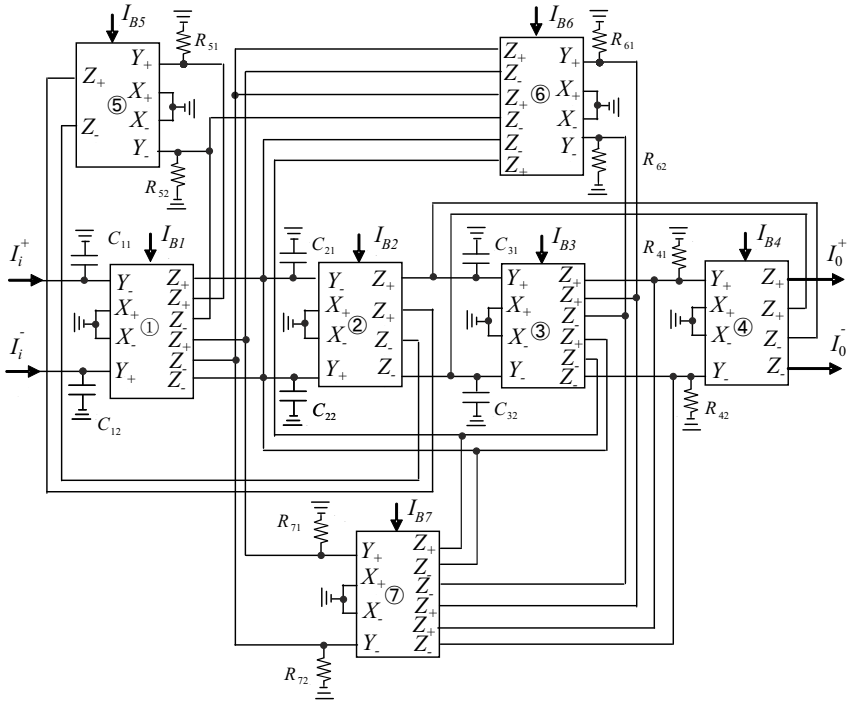

Fig. 12. The CFBCCII based 3rd-order elliptic low-pass ladder filter

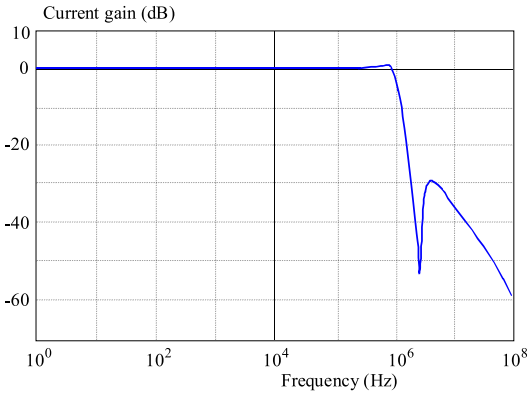

Fig. 13. The frequency response of the current gain

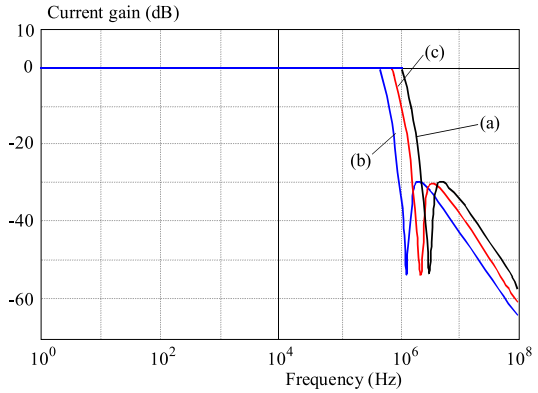

Fig. 14. Simulated frequency response of the current gain with different cut-off frequency

Table 2. Parameter setting for the proposed filter

CFBCCII	Transfer function	R_X	R	C
1	$1/[sR_0(C_1+C_2)]$	$R_{X1}=R_0$	—	$C_{11}=C_{12}=C_1+C_2$
2	R_0/sL_2	$R_{X2}=R_0$	—	$C_{21}=C_{22}=L_2/R_0^2$
3	$1/[sR_0(C_2+C_3)]$	$R_{X3}=R_0$	—	$C_{31}=C_{32}=C_2+C_3$
4	R_0/R_L	$R_{X4}=R_L$	$R_{41}=R_{42}=R_0$	—
5	$-R_0/R_S$	$R_{X5}=R_S$	$R_{51}=R_{52}=R_0$	—
6	$C_2/(C_1+C_2)$	$R_{X6}=C_1+C_2$	$R_{61}=R_{62}=C_2$	—
7	$-C_2/(C_2+C_3)$	$R_{X7}=C_2+C_3$	$R_{71}=R_{72}=C_2$	—

4.2 Parameter Setting

As shown in Fig. 12, the filter consists of 7 CFBCCIIs, and all of them are numbered. The 1st CFBCCII is connected as a integrator, whose transfer function can be obtained as $1/[sR_0(C_1+C_2)]$. According to (3), the intrinsic resistance in X terminal of the first CFBCCII can be written as $R_{X1}=R_0$, and the values of the capacitors would be $C_{11}=C_{12}=C_1+C_2$. The 2nd CFBCCII acts as a integrator whose transfer function is $R_0/(sL_2)$. Setting the value of R_{X2} to be $R_{X2}=R_0$, then the capacitor values are: $C_{21}=C_{22}=L_2/R_0^2$. The 3rd CFBCCII, also acts as an integrator, whose transfer function is $1/[sR_0(C_2+C_3)]$, so $C_{31}=C_{32}=C_2+C_3$, and $R_{X3}=R_0$. The 4th to 7th CFBCCIIs act as scaling elements, and their gains are R_0/R_L, $-R_0/R_S$, $C_2/(C_1+C_2)$ and $C_2/(C_2+C_3)$, respectively. Then one can obtain: $R_{41}=R_{42}=R_0$, $R_{X4}=R_L$, $R_{51}=R_{52}=R_0$, $R_{X5}=R_S$, $R_{61}=R_{62}=C_2$, $R_{X6}=C_1+C_2$, $R_{71}=R_{72}=C_2$, $R_{X7}=C_2+C_3$. All the parameters are shown in Table 2.

5 DESIGN EXAMPLE

A third order elliptic filter can be designed according to the analysis above. The -3 dB cut-off frequency is selected to be $f_c=1$ MHz, the matching impedance is $R_r=1\,\mathrm{K\Omega}$. Considering an elliptic filter with a passband ripple of 0.0109 dB, and a stopband ripple of 28 dB, and consulting the elliptic function normalized parameter C 0305-20 yields the normalized filter parameters as follows [27]: $C_1'=C_3'=0.5728$, $C_2'=0.1043$, $L'=0.8545$, $R_S'=R_L'=1$. According to the normalized equations, $C=C'/(2\pi f_c R_r)$ and $L=L'R_r/(2\pi f_c)$, the parameters in Fig. 10 can be obtained as $C_1=C_3=C_1'/(2\pi f_c R_r)=91.2\,\mathrm{pF}$, $C_2=C_2'/(2\pi f_c R_r)=16.6\,\mathrm{pF}$, $L_2=L'R_r/(2\pi f_c)=1.36\times10^{-4}\,\mathrm{H}$, $R_S=R_L=R_S'R_r=R_L'R_r=1\,\mathrm{K\Omega}$, and the virtual resistor R_0 is set to be $R_0=1\,\mathrm{K\Omega}$.

According to Table 2, the parameters in Fig. 12 can be calculated: $C_{11}=C_{12}=C_1+C_2=107.8\,\mathrm{pF}$, $C_{21}=C_{22}=L_2/R_0^2=136\,\mathrm{pF}$, $C_{31}=C_{32}=C_2+C_3=107.8\,\mathrm{pF}$, $R_{X1}=R_{X2}=R_{X3}=1\,\mathrm{K\Omega}$, $R_{X4}=R_{X5}=1\,\mathrm{K\Omega}$, $R_{X6}=C_1+C_2=107.8\times10^{-12}\Omega$, $R_{X7}=C_2+C_3=107.8\times10^{-12}\Omega$, $R_{41}=R_{42}=R_{51}=R_{52}=R_0=1\,\mathrm{K\Omega}$, $R_{61}=R_{62}=R_{71}=R_{72}=C_2=16.6\times10^{-12}\Omega$. Notice that the value of resistors R_{61}, R_{62}, R_{71}, R_{72}, R_{X6}, and R_{X7} are very small in practice, as the 6th and 7th CFBCCIIs act as scalers. If one multiplies the transfer functions with the same factor, the transfer functions would not change, so they can be rewritten as follows: $H(s)_6=[C_2\times10^{13}]/[(C_1+C_2)\times10^{13}]$, $H(s)_7=[C_2\times10^{13}]/[(C_2+C_3)\times10^{13}]$, then $R_{X6}=(C_1+C_2)\times10^{13}=1.078\,\mathrm{K\Omega}$, $R_{X7}=(C_2+C_3)\times10^{13}=1.078\,\mathrm{K\Omega}$, $R_{61}=R_{62}=R_{71}=R_{72}=C_2\times10^{13}=166\,\Omega$. One can see that the 7 intrinsic resistances R_X are $1\,\mathrm{K\Omega}$. According to (2), the bias current of each CFBCCII can be obtained as $I_{B1}=I_{B2}=I_{B3}=I_{B4}=I_{B5}=I_{B6}=I_{B7}=60\,\mu\mathrm{A}$. Simulation on the power dissipation has also been made, and it is found to be 22 mW.

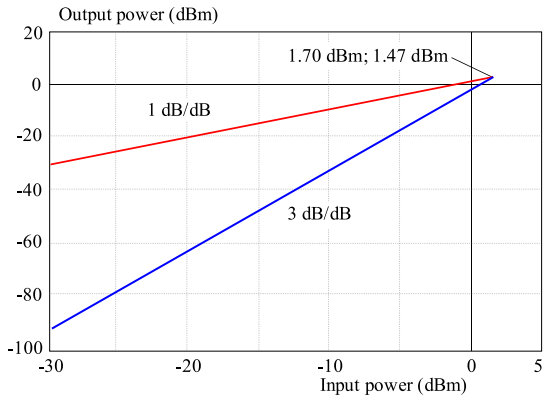

Fig. 15. Simulated frequency response of the current gain with different cut-off frequency

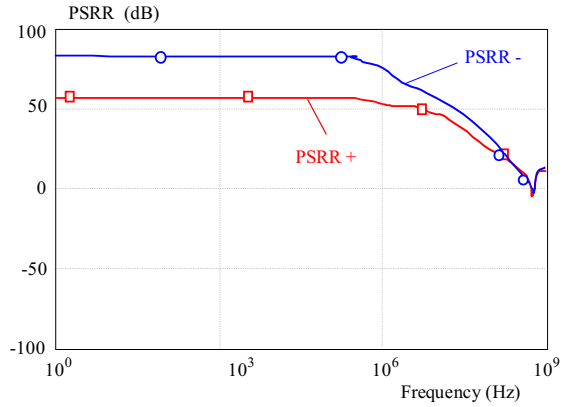

Fig. 16. The power supply rejection ratio of the CFBCCII based 3^{rd}-order elliptic filter

This filter is simulated in Cadence Spectre Using Chartered 0.35 μm CMOS process parameters. The configuration of the building block CFBCCII is shown in Fig. 3, and the dimensions of CMOS transistors are listed in Table 1. Supply voltages of the filter are ± 1.65 V, and bias current of each CFBCCII is 60 μA, the parameters of the passive elements are set as: $C_{11} = C_{12} = C_{31} = C_{32} = 107.8$ pF, $C_{21} = C_{22} = 136$ pF, $R_{41} = R_{42} = R_{51} = R_{52} = 1\,\text{K}\Omega$, $R_{61} = R_{62} = R_{71} = R_{72} = 166\,\Omega$. The frequency response of the transfer function is shown in Fig. 13. The passive filter has a passband ripple of 0.0109 dB and a stopband ripple of 28 dB. The figure shows the elliptic filter has a cut-off frequency of 1.06 MHz, which is 600Hz larger than the designed frequency, a passband ripple of 0.012 dB, which is 0.001 dB larger than the standard value, and a stopband ripple of 29.2 dB, which is in accordance with the standard value.

When we change the bias currents of the 6^{th} CFBCCII, the intrinsic resistance R_{x6} will be varied. Referring to Table 2 and the aforementioned analysis, the equation can be obtained as: $R_{X6} = (C_1 + C_2) \times 10^{13}$. According to the normalized equation $C_1 + C_2 = (C_1' + C_2')/(2\pi f_c R_r)$ and (2), the relationship between the bias current and the cut-off frequency can be obtained as $f_c = [(C_1' + C_2')\sqrt{2K_{eff} I_B}/\pi R_r] \times 10^3$; It is obvious that the cut-off frequency can be adjusted by bias current tuning. Simulations are made to demonstrate the tuning characteristic of this circuit. Figure 14 shows the frequency response of the current gain with different 3 dB frequencies. There are three curves in the figure, curve (a) shows the situation when the bias currents are equal to 60 μA and $f_c = 1$ MHz, Curve (b) shows the second situation: when the bias current of the 6^{th} CFBCCII is set to be 40 μA, then $C_{11} = C_{12} = C_1 + C_2 = 122$ pF, so the cut-off frequency should be 883 KHz. Curve (c) shows the situation when the bias current of the 6^{th} CFBCCII I_{B6} is set to be 50 μA, where $C_{11} = C_{12} = C_1 + C_2 = 112$ pF, and the cut-off frequency is 963 KHz.

Figure 15 shows the linearity of this circuit, and one can see that the input third-order intercept point (IIP3) is 1.7 dBm, indicating that the circuit has good linearity property. Figure 16 shows the simulation results of the power supply rejection ratio (PSRR) of the filter, PSRR from the positive supply to the output (PSRR_+) is 57dB, and PSRR from the negative supply to the output (PSRR_-) is 83dB. It can be seen that $PSRR$ of the filter is high, this is partly because of the fully balanced structure, and then the noise at the output contributed by the ripple on the power supplies can be partly counteracted.

6 CONCLUSIONS

This paper proposes a new element, so called a current controlled fully balanced second-generation current conveyor circuit (CFBCCII) which employs a fully balanced structure to suppress common-mode signals. Then, a current-mode elliptic filter synthesis procedure using CFBCCII is proposed. Although the filter realization is complicated, it has following advantages: (1) The fully balanced circuit structure of the filter can suppress even harmonics and common-mode signals, effectively. (2) The cut-off frequency of the filter can be controlled by adjusting the bias current of CFBCCII. (3) The SFG approach is intuitive and simple. (4) The filter maintains the low-sensitivity properties of its LC prototype. (5) All passive filter components are grounded.

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