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FEEDBACK LOOP CONTROL STRATEGIES OF THE MULTI DC BUS LINK VOLTAGES USING ADAPTIVE FUZZY LOGIC CONTROL

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Voltage source multilevel inverters have become very attractive for power industries in power electronics applications during last years. The main purposes that have led to the development of the studies about multilevel inverters are the generation of output voltage signals with low harmonic distortion; the reduction of switching frequency. A serious constraint in a multilevel inverter is the capacitor voltage-balancing problem. The unbalance of different DC voltage sources of five-level neutral point clamping (NPC) voltage source inverter (VSI) constitutes the major limitation for the use of this new power converter. In order to stabilize these DC voltages, we propose in this paper to study the cascade constituted by three phases five-level PWM rectifier, a clamping bridge and five-level NPC (VSI). In the first part, we present a topology of five-level NPC VSI, and then they propose a model of this converter and an optimal PWM strategy to control it using four bipolar carriers. Then in the second part, we study a five-level PWM rectifier, which is controlled by a multiband hysteresis strategy. In the last part of this paper, the authors study shows particularly the problem of the stability of the multi DC voltages of the inverter and its consequence on the performances of the induction motors (IM). Then, we propose a solution to the problem by employed closed loop regulation using PI regulator type fuzzy logic controller (FLC). The results obtained with this solution confirm the good performances of the proposed solution, and promise to use the inverter in high voltage and great power applications as electrical traction.

K e y w o r d s: NPC inverter, clamping bridge, rectifier multilevel, PWM strategy, enslavement, fuzzy logic control

1 INTRODUCTION

Multilevel are based on the neutral point clamped (NPC) inverters topology and were proposed firstly by Nabae and al [1]. Multilevel inverter structures provide an attractive solution for high power and high voltage applications. While the multilevel topology lets higher voltages using devices of lower ratings, the link multi DC voltage balancing problem is a serious drawback which limits the applicability of multilevel topology for motor drives. One of the major limitations of the multilevel inverters is the instability of the input multi DC voltages [2, 3].

In this work, the authors study a new AC/DC/AC converter five-level NPC PWM rectifier. It synthesis the staircase voltage wave form several levels of multi DC voltages.

In the first part, the knowledge model of this inverter is developed and also the used optimal PWM strategy which requires four bipolar carriers. After that, we clearly show up the stability problem of the four inputs DC voltage sources by studying a five-level PWM current rectifier-clamping bridge-five-level NPC VSI-IM cascade. In the last part of this paper, we study the stability problem of the input multi DC VSI [4]. For this, we propose a solution to this problem by using fuzzy logic controller (FLC) feedback loops to regulate the total DC voltages by using Proportional-Integral regulator [5, 6]. The results obtained with this solution shows that the proposed solution is very efficient to solve the instability problem of this multilevel inverter.

2 FIVE–LEVEL NPC VSI MODELLING

A multilevel voltage source inverter is a converter structure able to proving a line to ground voltage, at each arm, with more than two different levels in the range of 0 to U_c volts. The numbers of levels N corresponds to the different potential levels that each arm is able to deliver at the output. With the emerging concept of multilevel voltage source inverters, some technological limitations of two-level standard inverter can be reduced or avoided making possible the use to low cost semi conductors for high power applications drive. Also, lower harmonics distortion and electromagnetic interferences is expected with this new kind of static converter.

Different circuit topologies have been presented to implement this kind of converter, able of proving an output voltage with the mentioned characteristics. One of the most typical ones is the neutral point Clamped (NPC).

In this topology, a series connection of $N-1$ capacitors is done to create $N-2$ points with different potentials.

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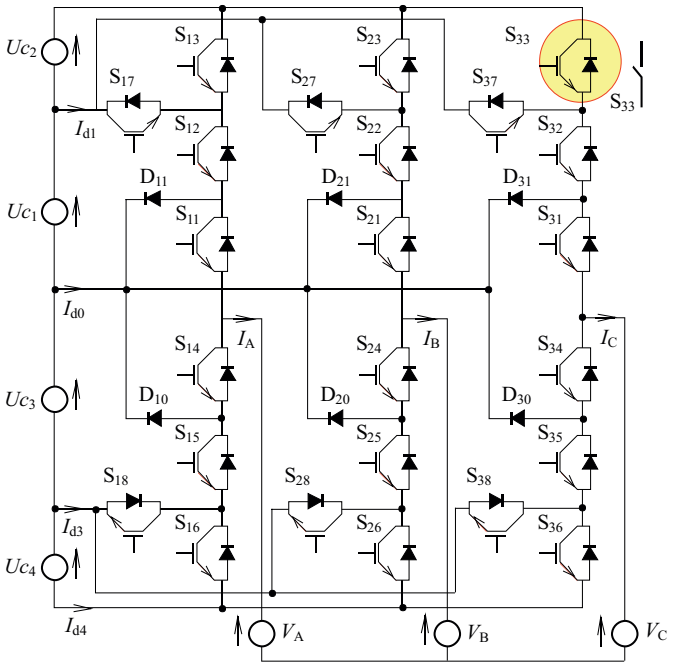

Fig. 1. A Five-level NPC voltage source inverter

Considering in a first approach, that the capacitors from an ideal voltage divider, each point is a DC potential and may be connected to the output by switching on the convenient electronics switches. This characteristic permits the generations of the $N-2$ intermediate voltage at each arm output which U_c and zero voltages always available, constitute the total of N-level voltage generation mechanism. A generic N-level, NPC topology arm presents the following characteristics [7]:

- Each output voltage levels is provided by only one combination of the switches states, so even at steady state operation some switches may have higher switching frequency than others.
- Voltage across each opened electronics switch is intrinsically limited to $U_c/(N-1)$.
- The number of capacitors needed of middle point generation is $N-1$. The number of clamping diodes is $2(N-2)$.

The general structure of the three phase's five-level NPC voltage source inverter is shown in Fig. 1. It is constituted by three arms and four DC voltages sources. Every arm has eight bi-directional switches, six in series and two in parallel and two diodes D_{i0} and D_{i1} ($i \in \{1,2,3\}$) which let to have zero voltage for V_{KM}. V_{KM} is the voltage of the phase K relatively to the middle point M, where $K \in \{A,B,C\}$ [7].

2.1 Knowledge model of the five-level NPC VSI

For this study we will consider that semiconductors are ideal. If semiconductors are assumed in a controllable mode, we can define for each semi-conductor Tis a switching function Sis corresponding switch state (1 =turned on and 0 =turned off) [1, 3]: Several complementary laws are possible for the five-level NPC VSI. The optimal one is given below

$$\begin{aligned} &B_{i1} = \overline{B}_{i5}\,, \quad B_{i2} = \overline{B}_{i4} \quad \text{and} \quad B_{i3} = \overline{B}_{i6}\,. \\ &B_{iS} \text{ is the control signal of the semiconductor } T_{iS}\,. \end{aligned} \tag{1}$$

The output voltage of the inverter, relatively to the middle point M, is given by the following system

$$\begin{aligned} V_{KM} = {} & S_{i1}S_{i2}(1-S_{i3})U_{C1} + S_{i1}S_{i2}S_{i3}(1-S_{i4})(U_{C1}+U_{C2}) \\ & - S_{i4}S_{i5}(1-S_{i6})U_{C3} - S_{i4}S_{i5}(1-S_{i6})(U_{C3}+U_{C4})\,. \end{aligned} \tag{2}$$

In order to get a simple model to design the control, we define equivalent switching functions S^b_{i1} and S^b_{i0} and a global half arm $\left(S^{bT}_{i1}\,,\, S^{bT}_{i0}\right)$ switching function associated respectively to the upper and lower half commutation cells.

$$\begin{aligned} S^b_{i1} &= S_{i1}S_{i2}S_{i3}\,, \\ S^b_{i0} &= S_{i6}S_{i7}S_{i8}\,, \\ S^{bT}_{i1} &= S_{i7} + S^b_{i1}\,, \\ S^{bT}_{i0} &= S_{i8} + S^b_{i0}\,. \end{aligned} \tag{3}$$

We suppose that capacitor voltages are balanced: $U_{c1} = U_{c2} = U_{c3} = U_{c4} = U_c$, the simple voltages of the three phases five-level NPC VSI are given by

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{pmatrix} S_{11}bT - S^{bT}_{10} \\ S_{21}bT - S^{bT}_{20} \\ S_{31}bT - S^{bT}_{30} \end{pmatrix} U_C\,. \tag{4}$$

The input currents of the inverter are

$$\begin{aligned} i_{d1} &= S_{17}i_1 + S_{27}i_2 + S_{37}i_3\,, \\ i_{d2} &= S^b_{11}i_1 + S^b_{21}i_2 + S^b_{31}i_3\,, \\ i_{d3} &= S_{18}i_1 + S_{28}i_2 + S_{38}i_3\,, \\ i_{d4} &= S^b_{10}i_1 + S^b_{20}i_2 + S^b_{30}i_3 \end{aligned} \tag{5}$$

with

$$\begin{aligned} i_{d0} = (i_1+i_2+i_3) - \left(S^{bT}_{11} + S^{bT}_{10}\right)i_1 - \left(S^{bT}_{21} + S^{bT}_{20}\right)i_2 \\ - \left(S^{bT}_{31} + S^{bT}_{30}\right)i_3\,. \end{aligned} \tag{6}$$

2.2 Optimal PWM strategies method

Other authors have extended two-level carrier-based PMWM techniques to multilevel inverters by making the use of several triangular carrier signals and one reference signal per phase. For N-level inverter, $(N-1)$ carriers with the same frequency f_c and same peak to peak amplitude A_c are disposed such that the bands they occupy are contiguous. The reference, or modulation, wave form has peak to peak amplitude A_m and frequency f_m, and it is centred in the middle of the carrier set. The reference

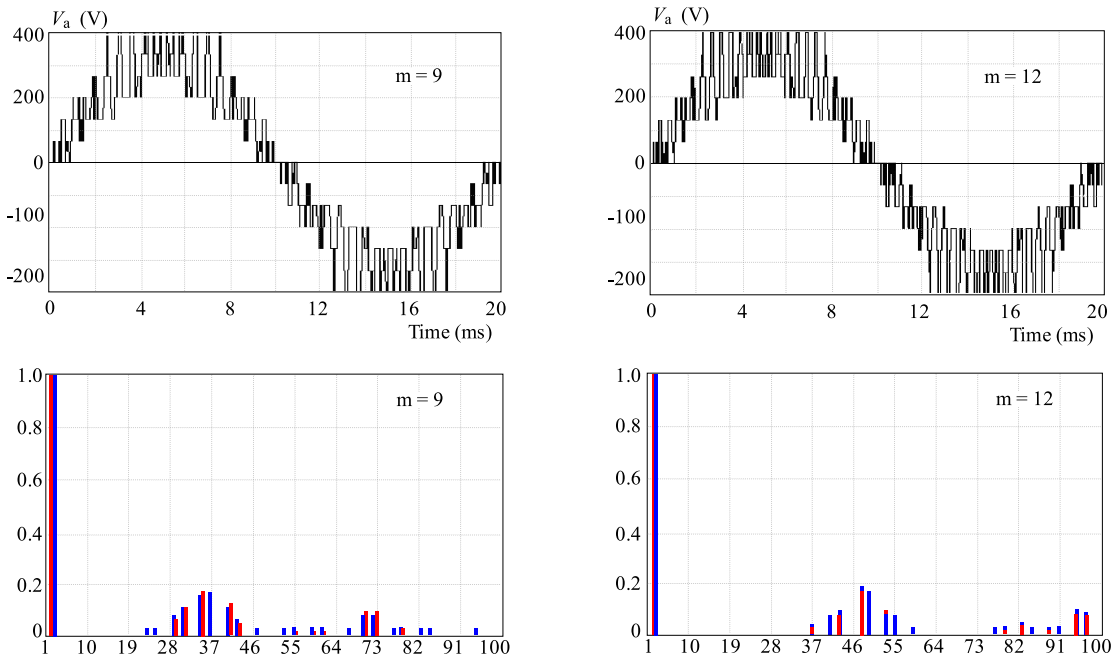

Fig. 2. A Five-level NPC voltage source inverter

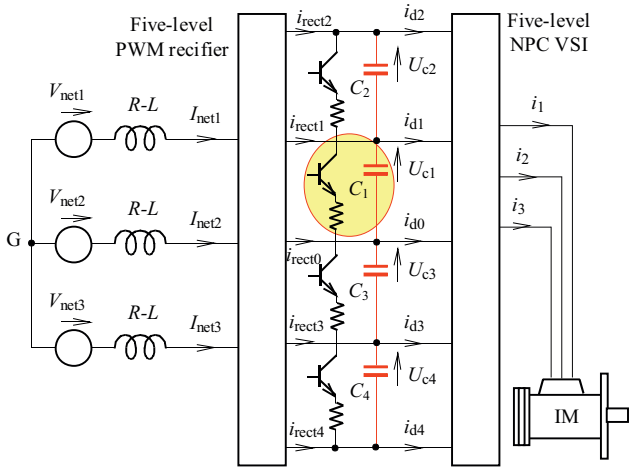

Fig. 3. Five level PWM rectifier-clamping bridge

is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active corresponding to that carrier is switched off [2].

In multilevel inverters, the amplitude modulation index, m_a and the frequency ratio, m_f are defined as $m_a = A_m/A_c = f_c/f_m$.

The principle of this strategy optimal PWM witch is similar to sub harmonic PWM except that a zero sequence (triplen harmonic) voltage is added to each of the carrier waveforms. This method takes the instantaneous average of the maximum and minimum of the three reference voltages $V_{\mathrm{Sref}} = (V_a^*, V_b^*, V_c^*)$ and subtracts this value from each of the individual reference voltages to obtain the modulation waveform [2, 3]. The voltage V_{offset} is given by

$$V_{\mathrm{offset}} = \frac{\max(V_{\mathrm{Sref}}) + \min(V_{\mathrm{Sref}})}{2}. \tag{7}$$

The new reference vectors are defined as follows

$$V^*_{\mathrm{Kref}} = V^*_{\mathrm{K}} - V_{\mathrm{offset}}\,. \tag{8}$$

Figure 2 represents the simple output voltage of the five-level NPC VSI controlled by the proposed optimal PWM strategy with four bipolar carriers for $m = 9, 12$ and $r = 0.9$. We notice that, for even values of m, the simple output voltage has symmetry relatively to the quarter of the period, and we have only odd harmonics. But for odd values of m, we have no symmetry, and then even and odd harmonics exist. The voltage harmonics gather by families centred around frequencies multiple of $4\,mf$.

3 FIVE–LEVEL PWM RECTIFIER–CLAMPING BRIDGE–FILTER–FIVE–LEVEL NPC VSI–CASCADE

Until now, we have supposed the input multi DC voltages of five-level NPC VSI constants. In this part, we study a generation input DC voltages manner. For this, we propose a cascade presented in Fig. 3.

3.1 Modelling and Control of five-level PWM current rectifier

The advantages of five-level PWM rectifier topology are well known and have been applied in medium and

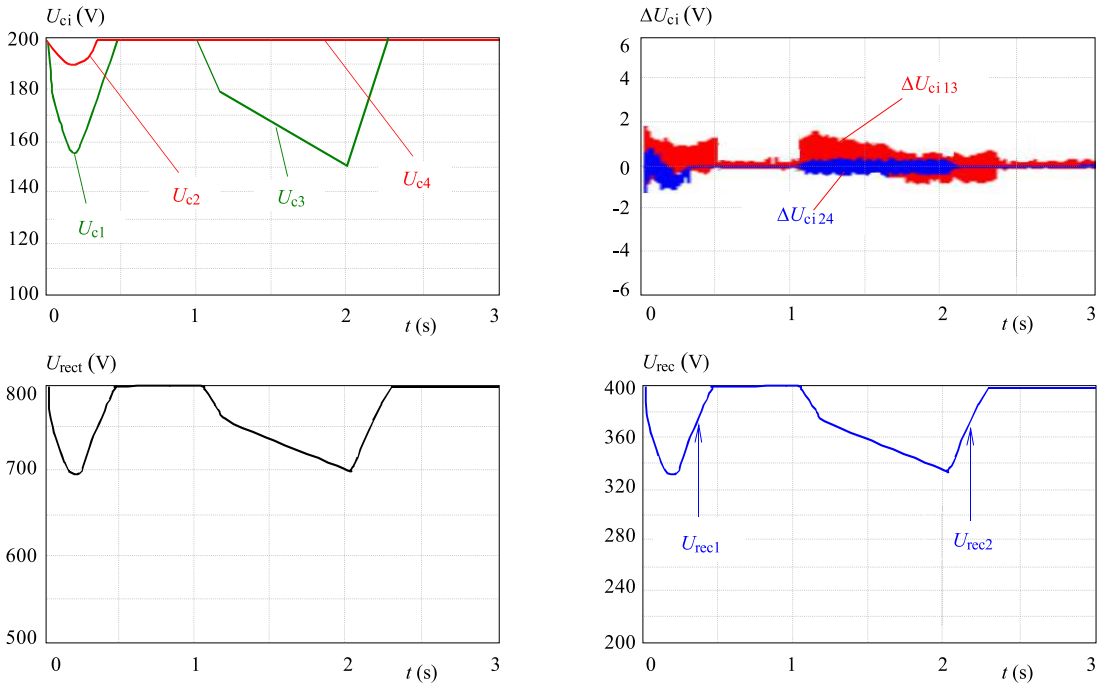

Fig. 4. The multi input and output DC voltages and the difference ΔU_{Ci} of the five-level PWM rectifier

high power applications in the last years [1]. The left side (input) bridge, connected to supply composed of R_{net}, L_{net} representing the AC side resistance and inductance is operated to absorb sinusoidal current, in phase with the line voltages $V_{\text{net}\lambda}$. In order to obtain fast response of the input converter, a multi band hysteresis current control technique can be adopted, with ensures that each line current follows its reference with minimum error.

The input voltages of five-level PWM rectifier are defined as

$$V_{KM} = S_{i1}^{bT} U_{\text{rect1}} + S_{i1}^{bT} U_{\text{rect2}} - S_{i0}^{bT} U_{\text{rect3}} - S_{i0}^{bT} U_{\text{rect4}} \,. \tag{9}$$

3.2 Modelling and Control of clamping bridge

The clamping bridge cell is a simple circuit with a transistor and a resistor in series across the DC capacitor as shown in Fig. 3. The transistors are drived to balance all capacitor voltages. The model of the intermediate filter is defined by the following equation

$$\begin{aligned} C_1 \frac{\mathrm{d}U_{c1}}{\mathrm{d}t} &= i_{\text{rect2}} + i_{\text{rect1}} - i_{r1} - i_{d1} - i_{d2} \,, \\ C_2 \frac{\mathrm{d}U_{c2}}{\mathrm{d}t} &= i_{\text{rect2}} - i_{r2} - i_{d2} \,, \\ C_3 \frac{\mathrm{d}U_{c3}}{\mathrm{d}t} &= -i_{\text{rect3}} - i_{\text{rect4}} - i_{r3} - i_{d4} - i_{d3} \,, \\ C_4 \frac{\mathrm{d}U_{c4}}{\mathrm{d}t} &= -i_{\text{rect4}} - i_{r4} + i_{d4} \end{aligned} \tag{10}$$

$$\text{with } ir_i = T_i \frac{U_{ci}}{R_{pi}} \,. \tag{11}$$

To control the transistor, we propose the following algorithm

$$\begin{gathered} U_{ci} - U_{\text{ref}} = \varepsilon_i \\ \text{if } \varepsilon_i > 0 \text{ then } T_i = 1 \Rightarrow i_{ri} = T \frac{U_{ci}}{R_{Pi}} \\ \text{else } T_i = 0 \Rightarrow i_{ri} = 0 \end{gathered} \tag{12}$$

3.3 Simulation results

Figure 4 shows the simulation results. We note the different input DC voltages of five-level NPC VSI $U_{ci_{(i=1\div4)}}$ are practically not equal, but by pairs they are equal ($U_{c1} = U_{c3}$ and $U_{c2} = U_{c4}$) and become constant after a long transient state. For a load variation, we shows the different input DC $U_{ci_{(i=1\div4)}}$ and output voltage PWM rectifier $U_{\text{rect}_{(i=1\div2)}}$ are sensible to any perturbation and are affected during the variation of the load torque between two instants (Fig. 4). This fact accentuates the problem of unbalance of the different input DC voltages sources of five-level NPC VSI.

4 FUZZY LOGIC FEEDBACK CONTROLS OF MULTI DC BUS LINK VOLTAGES OF FIVE–LEVEL CONVERTER

Recent developments in artificial-intelligence-based control have brought into focus a possibility of replacing a PI controller with a fuzzy logic FL equivalent. Fuzzy logic control (FLC) is sometimes seen as the ultimate solution for high-performance drives of the next generation. To remedy to the problem of the instability of the output DC voltage of the PWM rectifier [8], we propose to enslave it by using a PI type fuzzy logic regulator [5, 6].

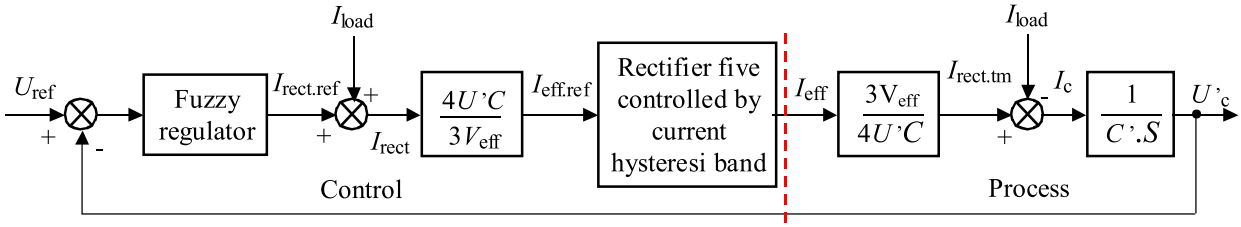

Fig. 5. Synoptic diagram of the five-level PWM rectifier

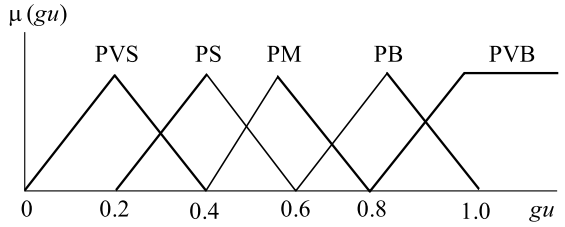

Fig. 6. Membership functions of the output gain

Table 1. A seven-term fuzzy rule table

e / Δe	NB	NM	NS	ZE	PS	PM	PB
NB	PVB	PVB	PB	PM	PS	PVS	PVS
NM	PVB	PB	PM	PS	PVS	PVS	PVS
NS	PB	PM	PS	PVS	PVS	PVS	PS
ZE	PM	PS	PVS	PVS	PVS	PS	PM
PS	PS	PVS	PVS	PVS	PS	PM	PB
PM	PVS	PVS	PVS	PS	PM	PB	PVB
PB	PVB	PVB	PS	PM	PB	PVB	PVB

The synoptic diagram of five-level PWM current rectifier control is given in Fig. 5.

4.1 Multi DC bus link voltage controller

The proposed system configuration is shown in Fig. 3. In order to maintain multi DC bus link voltage U'_c, irrespective of reference U_{ref} and load variations, a closed loop introduced.

The modelling of this loop is based on the instantaneous power conservation principle with no loss. hypothesis. This loop imposes efficient network current [7, 8]. Input power and output power

$$P_{\text{in}} = \sum_{\lambda=1}^{3}\left(V_{\text{net}\lambda} i_{\text{net}\lambda} - R i_{\text{net}\lambda}^2 - \frac{L}{2}\frac{\mathrm{d}i_{\text{net}\lambda}^2}{\mathrm{d}t}\right),$$
$$P_{\text{out}} = \sum_{i=1}^{4}(U_C i_{\text{rect}i}) = 4U_C(i_c + i_{\text{load}})\,. \tag{13}$$

We define the different grandeurs i_c, i_{load} and U'_c as follows

$$i_c = \frac{1}{4}\sum_{i=1}^{4} i_{ci}\,, \quad i_{\text{load}} = \frac{1}{4}\sum_{i=1}^{4} i_{\text{load}i} \quad \text{and} \quad U'_c = \frac{1}{4}\sum_{i=1}^{4} U'_c\,. \tag{14}$$

4.2 Fuzzy voltage control strategy

To remedy to the problem of the instability of the output multi DC voltage of the PWM inverter [5, 9], we pro-

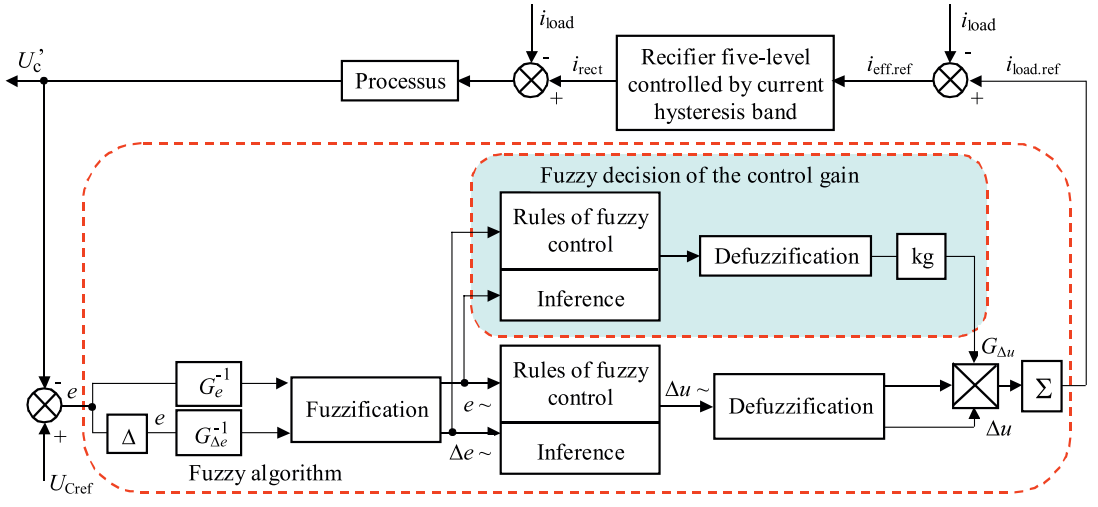

Fig. 7. Enslavement algorithm of output voltage of five-level rectifier using fuzzy logic control

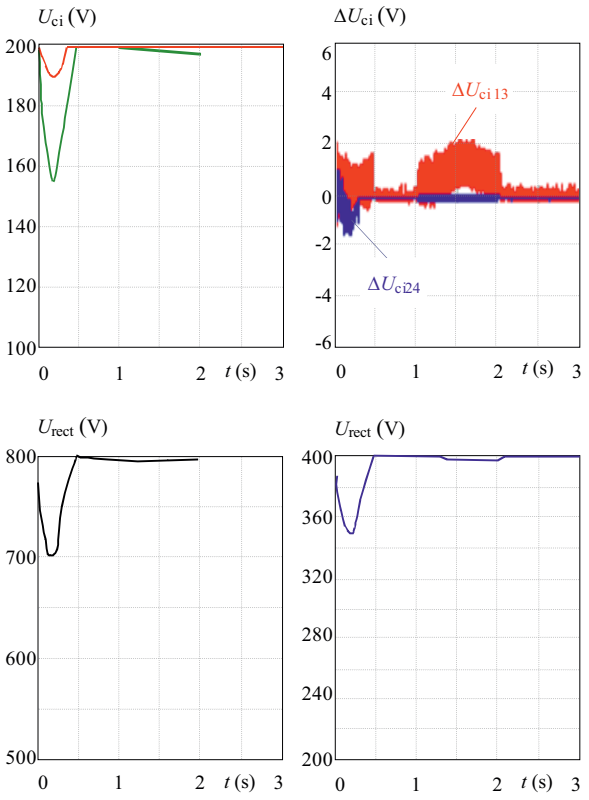

Fig. 8. Output DC voltages of five-level PWM rectifier

pose to enslave it by using a PI type fuzzy logic regulator [2, 10].

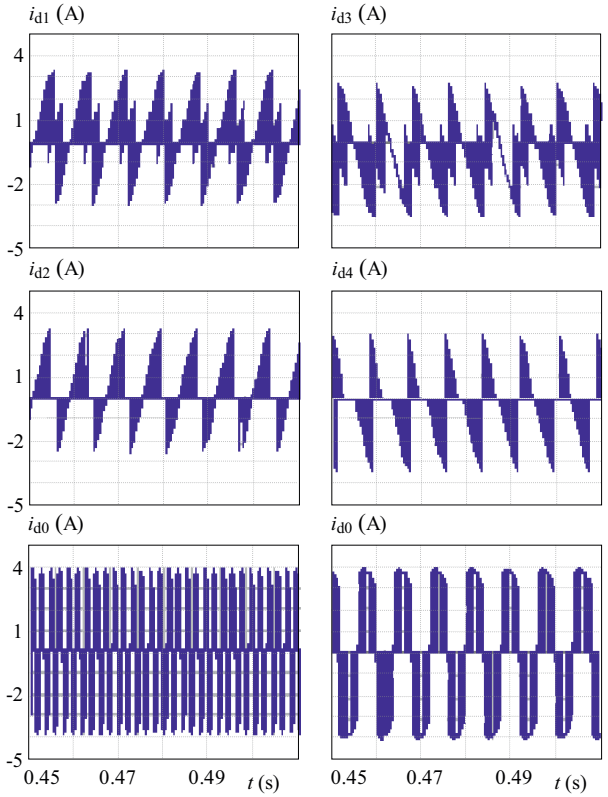

Fig. 9. Input currents of a five-level NPC VSI

In order to maintain multi DC bus link voltage U'_C, respective of reference U_{ref} and load variations. The inputs to the controller are the DC voltage error, $e(k)$ and the change of voltage error, $\Delta?e(k)$. The output of the fuzzy controller is change reference current $\Delta i_{\text{ref}}(k)$ [11].

$$\begin{aligned} E_U(k) &= U'_c(k) - U_{\text{cref}}(k)\,, \\ \Delta e_U(k) &= e_U(k) - e_U(k-1) \end{aligned} \tag{15}$$

where

$$e(k) = ge\, e(k)\,, \quad \Delta e(k) = gce\, \Delta c \tag{16}$$

with ge and gce, constant inputs gain which play an essential role, since they determine the control performances.

For the justification process, seven fuzzy levels are selected with the following fuzzy-set values for $e(k)$ and $\Delta e(k)$: NB (negative big), NM (negative medium), NS (negative small), ZE (zero), PS (positive small), PM (positive medium) and PB (positive big).

In most fuzzy control studies, the gain associated with the control output must be constant and as low possible in order to a void the instability problem. This increases considerably the response time of the system. To solve this problem, we consider the output gain gu as a fuzzy variable [6]. Therefore the gain must be adapted at every situation of the system as a function of the error and its variation. We chose fuzzy sets of variable gain whose corresponding membership functions are represented by Fig. 6.

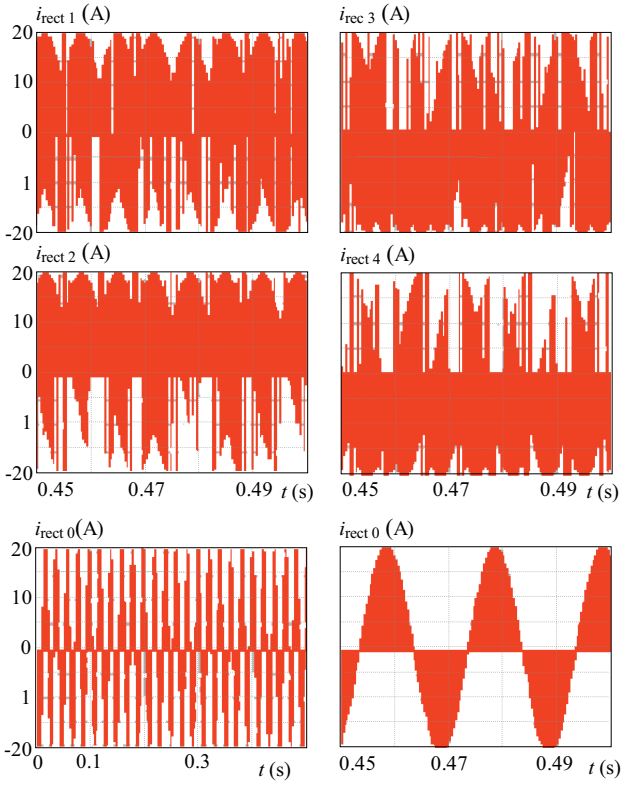

Fig. 10. Output currents of five levels

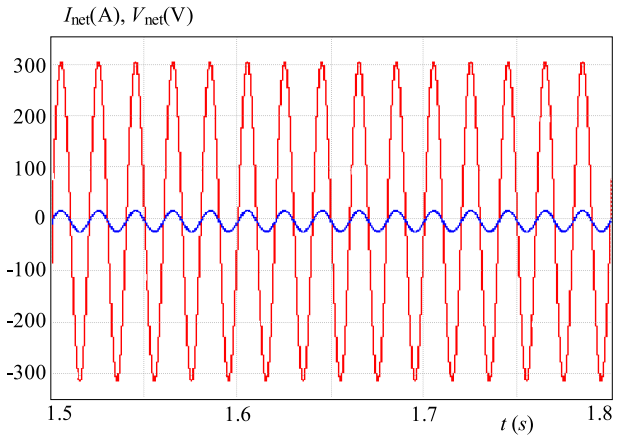

Fig. 11. The network current I_{net} and its voltage V_{net}

The decision matrix on the control gain is given in Table 1.

We use a regulator PI fuzzy logic for enslave multi DC bus link voltage. The general principle enslavement of five-level rectifier is given by Fig. 7. We use the algorithm enslavement elaborate previously (Fig. 5) to control the rectifier of the cascade we apply load variation between two instants $t = 1$ s and $t = 2$ s.

Figures 8–11 show the simulation results when we use a full clamping bridge and feedback control with PI fuzzy logic regulator. We show the performances of the FLC of the output voltage of the five-level PWM rectifier (Fig. 8). We note that, the output voltage of PWM rectifier follows perfectly its reference which is constant and are no effect for the load variation (Fig. 8).

Therefore the different input DC voltages of the five-level NPC VSI are constant and practically equal by pairs too ($U_{c1} = U_{c3}$ and $U_{c2} = U_{c4}$), become constant after a transient state and insensible to any perturbation (fig.8). In consequence the output voltage of the five-level NPC VSI is symmetrical.

The currents i_{d1} and i_{d2} are respectively the opposite of the currents i_{d3} and i_{d4} respectively. The inverter current rectifier i_{d0} has a mean value nearly null (Fig. 9).

The currents rectifier i_{rect1} and i_{rect2} are the opposite of the currents i_{rect3} and i_{rect4}, respectively. The current i_{rect0} has a mean value nearly null (Fig. 10). We remark that the grid currents $i_{\text{net}i}$ feeding rectifier follow their sinusoidal references (Fig. 11). The grid voltages and currents are in phase then the power factor at the grid connection is unit (Fig.11).

5 APPLICATION OF FEEDBACK CONTROLALGORITHM OF RECTIFIER OF THE CASCADE

In this part, we will study the performances of the speed control of the induction motors fed by five-level NPC inverter controlled by the proposed optimal PWM strategies (Fig. 12).

In order to simulate the dynamics of the induction motor, a simplified model has been developed. If all stator and rotor variables are expressed in a rotating reference frame and it is supposed that the 0 component is removed for symmetry reason, the four equations for electrical variables and the two mechanical equations are

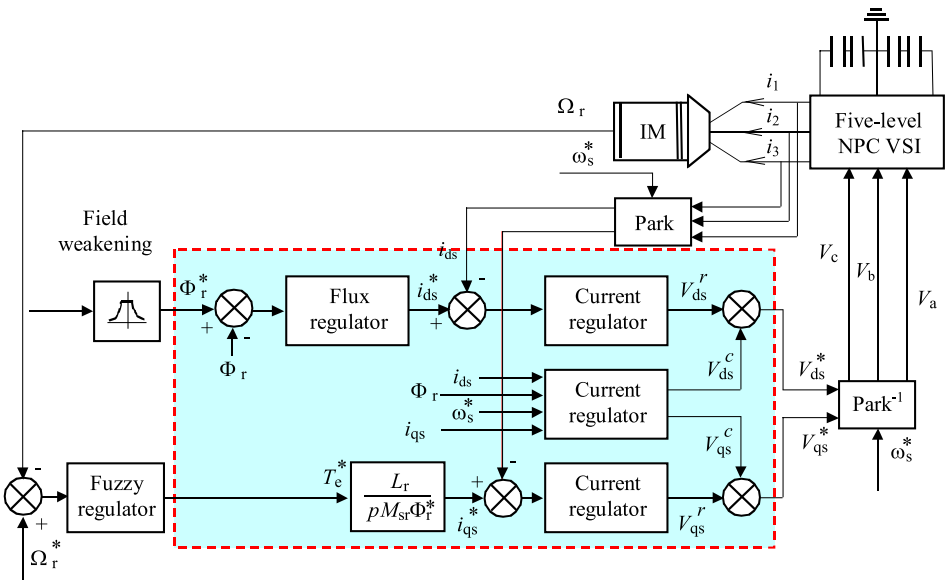

Fig. 12. The speed control using fuzzy logic regulator

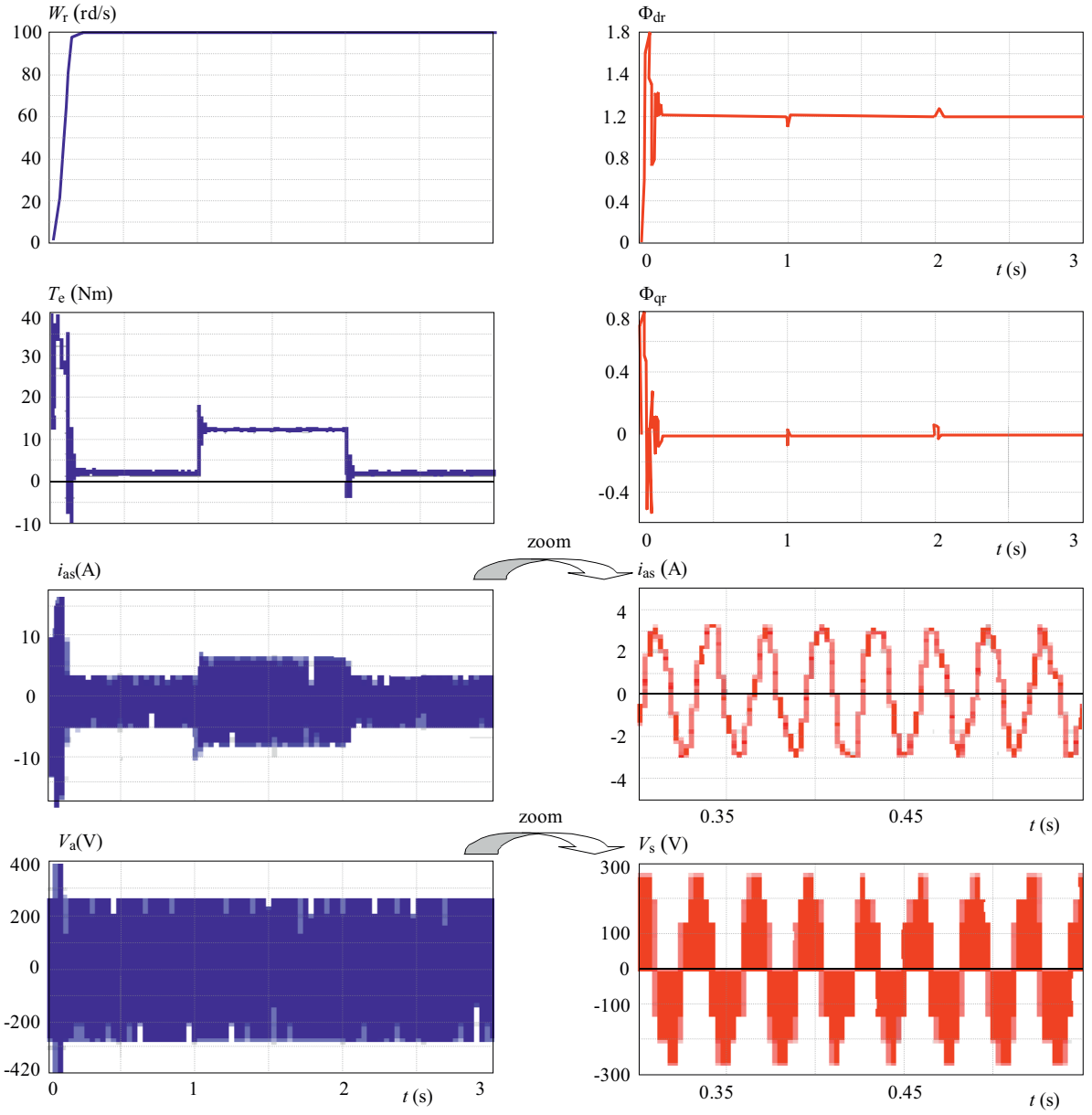

Fig. 13. Performances fed by five-level PWM rectifier-five-level NPC inverter-induction motors cascade

$$
\begin{aligned}
V_{ds} &= R_s i_{ds} + \frac{\mathrm{d}}{\mathrm{d}t}\Phi_{ds} - \omega_s \Phi_{qs}\,,\\
V_{qs} &= R_s i_{qs} + \frac{\mathrm{d}}{\mathrm{d}t}\Phi_{qs} - \omega_s \Phi_{ds}\,,\\
V_{dr} &= R_r i_{dr} + \frac{\mathrm{d}}{\mathrm{d}t}\Phi_{dr}\,,\\
V_{qr} &= R_r i_{qr} + \frac{\mathrm{d}}{\mathrm{d}t}\Phi_{qr}\,,\\
T_e &= \frac{3}{2}P\big(i_{qs}\Phi_{ds} - i_{ds}\Phi_{qs}\big).
\end{aligned}
\tag{17}
$$

Figure 13 shows the electromagnetic torque in study state. The driver of the IM fed quietly its reference. The output voltage of the five-level NPC VSI is sinusoidal and symmetrical. To confirm the effectiveness of the proposed control, a step load torque has been applied between 1 s and 2 s. Figure 13 shows that the line current is approximately sinusoidal. The rapid change of the line current shows that the system has a very good dynamic response to load variation. After starting phase and the variation test of the load torque, the machine stator current save the sinusoidal form.

6 CONCLUSION

In this paper, the fuzzy adaptive controller is used to minimize harmonics of side network introduced by the multilevel converter, including the control of power factor and we have studied the stability problem of the multi DC bus link voltage of the five-level NPC VSI using a cascade constituted by a five-level PWM rectifier-clamping bridge-five-level NPC VSI. We have particularly shown the problem of the middle point of multi DC voltages

source supplied the five- level VSI and its effects the serious problems of the speed control of induction motors and the output voltages source of the five-level inverter is asymmetric. To solve this problem, we propose the fuzzy logic feedback control of the input voltages of the five-level.

The use of the fuzzy logic feedback control has shown a good tracking of AC grid current and the stability of multi DC bus link voltages of the five-level NPC inverter. The results obtained shows that the proposed solution is very efficient to solve the instability problem of the multilevel inverter. Several tests have been performed in order to prove the efficiency of the type of the control. Simulation results confirm the validity of this control technique. So, now is possible to conceiver with frequency charger using in output the five-level inverter, IM variator with feeble rate of harmonics, a power factor of network unity and great charge dynamics performance.

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