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Current mode pulse width modulation/pulse position modulation based on phase lock loop

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In this paper, the fully integrated CMOS current mode PLL with current input injects at the place of input or output of the loop filter without summing amplifier circuit. It functions as PPM and PWM circuit is present. In addition, its frequency response is an analysis which electronic tuning BPF and LPF are obtained. The proposed circuit has been designed with 0.18 μm CMOS technology. The simulation results of this circuit can be operated at 2.5 V supply voltage, at center frequency 100 MHz. The linear range of input current can be adjusted from 43 μA to 109 μA, and the corresponding duty cycle of pulse width output is from 93% to 16% and the normalized pulse position is from 0.93 to 0.16. The power dissipation of this circuit is 4.68 mW with the total chip area is 28 μm $\times$ 60 μm.

K e y w o r d s: pulse width modulation, pulse position modulation, phase lock loop, current mode

1 Introduction

Modulation is a process of varying some property of periodic signal (or carrier signal) such as amplitude, phase or frequency. In general, the carrier signal can be used cosine wave signal for analog communication systems or square wave signal for digital communication systems. For digital modulation, if the carrier wave is a square wave signal, probably called a pulse modulation, which has three properties to generate the modulating signal.

Pulse width modulation (PWM) or pulse duration modulation (PDM) is one of pulse modulation techniques, using amplitude of the analog input signal to control a width of the positive pulse or duty cycle of the pulse period. The PWM technique is frequently utilized in many applications such as switching converters or motor control in control systems or power electronics, modulation/demodulation or power amplifier in communication system etc.

The other property of pulse modulation technique uses modulating an input signal to vary the position of the positive pulse within the pulse period. In general, it can be called Pulse Position Modulation (PPM). In PPM technique, the modulated signal is transmitted with short positive pulses and all pulses have both the same positive pulse width and amplitude. The PPM signal has been utilized to improve efficiency of PWM, it fixes a width of the pulse and decreases to small as possible. The PPM technique has an advantage in power output signal is less than the PWM technique. Finally, pulse amplitude modulation (PPM) which is to be convey information with varying magnitude of positive pulse of square wave carrier proportion directly to information signals.

In general, to generate the PWM signal, we can compare between the modulating signals with a reference signal which is simple to make a circuit. However, it has a problem about the drift of the carrier frequency. Due to this problem, many researches are proposed to improve this problem by using the phase lock loop (PLL) to generate the PWM signal. Because the PLL is a well-known in a negative feedback system and gives a high stability. Thus, it is an important in many areas such as controlling motor speed, modulate/demodulate, frequency synthesizer, phase shifter, carrier recovery and *etc.*

Many years ago, the researchers proposed a pulse width modulation or pulse position modulation based on phase lock loop [1-9]. They classified it into 2 operation types, which consisted of operating in voltage mode [1-4] and current mode [5-7]. The advantage of current mode is better than voltage mode such as larger dynamic range, high signal bandwidth, high linearity and low power etc.

From review the current mode PLL [5] and PWM based on PLL [6-7] which proposed to apply the current mode into certain parts such as a loop filter, while other parts are operated in voltage mode such as VCO or phase detector. Therefore, in this paper proposed a fully current mode PLL with RS F/F phase detector for simultaneous PWM/PPM signals generation by using CMOS Technology. For avoiding some of the limitation or disadvantage of voltage mode such as high voltage supply *etc.*

The proposed model and circuit description are shown at first, next the simulation and the results of this proposed circuit by testing the characteristic of individual parts and then, combined them to full current mode PWM/PPM are presented.

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2 The proposed Current Mode PWM/PPM and Circuit Description

2.1 System Description and Analysis

In this article, pulse width and pulse position modulator by using current mode phase lock loop is proposed. It composts of current phase detector, current loop filter, and current control oscillator, which the reference signal and the output signal of current control oscillator are converted to be mono pulse signals and they are fed to be the input of RS F/F to detect the phase difference between each other. The high frequency component of the output pulse signal of RS F/F is eliminated by using a current loop filter and then its output is used to control the output frequency of the current control oscillator. The block diagram of phase lock loop can be shown as Fig. 1

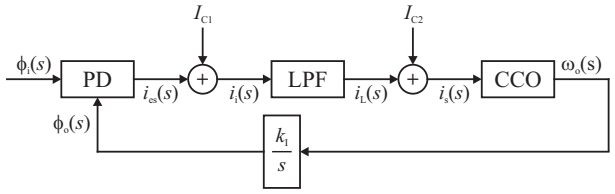

Fig. 1. Block diagram of Current Mode pwm / ppm Based on pll

From Fig. 1, the meaning of the symbolic is described by the following,

$\Phi_i(s)$ is a Laplace transform of an input phase function $\phi i(t))$, $\Phi_0(s)$ is a Laplace transform of an output phase function $\phi_0(t)$, $\Delta\Phi(s)$ is a Laplace transform of a phase differences $\delta\phi(t)$, $i_L(s)$ is a Laplace transform of an output loop filter $i_L(t)$, $\Omega_L(s)$ is a Laplace transform of an output frequency function of CCO, $F(s)$ is a transfer function of a loop filter, $\Omega_r(s)$ is a Laplace transform of an output frequency function of CCO when $i_L(t) = 0$, k_d is a gain of a phase detector, k_L is a gain of a loop filter, and k_I is a gain of an integrator.

From symbolic meaning above, when we find relation all of them, which $\phi_i(s)$ and $\phi_0(s)$ relationship

$$\frac{F(s)k_dk_0k_I\phi_0(s)}{s} + \phi_0(s) = \frac{F(s)k_dk_0k_I\phi_i(s)}{s} + \\ + \frac{F(s)k_0k_II_{C1}(s)}{s} + \frac{k_0k_II_{C2}(s)}{s} + \frac{k_I\omega_r}{s^2} \tag{1}$$

To obtain a second order phase lock loop. Loop filter is assumed to be first order LPF and its transfer function is $F(s) = A/(1 + G_s)$ when it is substituted into (1), we will derive a relation as

$$\frac{Ak_dk_0k_I\phi_0(s)}{s\,(1+Gs)} + \phi_0(s) = \frac{Ak_dk_0k_I\phi_i(s)}{s\,(1+Gs)} + \\ + \frac{Ak_0k_II_{C1}(s)}{s\,(1+Gs)} + \frac{k_0k_II_{C2}(s)}{s} + \frac{k_I\omega_r}{s^2} \tag{2}$$

where it is assumed that $K = Ak_dk_0k_I$ and it is instituted into (2) we will get their relation in s-domain followed by inverse Laplace transform of in order to get their relation in time domain

$$Gs^2\phi_0(s) + s\phi_0(s) + K\phi_0(s) = K\phi_i(s) + \frac{K}{k_d}I_{C1}(s) + \\ + \frac{K}{Ak_d}(1+Gs)I_{C2}(s) + \frac{k_I\omega_r}{s} + k_IG\omega_r(s) \tag{3}$$

$$G\frac{d^2\phi_0(t)}{dt^2} + \frac{d\phi_0(t)}{dt} + K\phi_0(t) = K\phi_i(t) + \\ + \frac{K}{k_d}I_{C1}(t) + \frac{K}{Ak_d}\left(I_{C2}(t) + G\frac{dI_{C2}(t)}{dt}\right) + \\ + k_I\omega_ru(t) + k_IG\omega_r\delta(t) \tag{4}$$

Assuming $\Phi_i(t) = \omega i(t) + \theta_i$ and input signal $I_{C2}(t) = 0$ when $t \geq 0$ $u(t) = 1$; $\delta(t) = 0$, therefore

$$G\frac{d^2\phi_0(t)}{dt^2} + \frac{d\phi_0(t)}{dt} + K\phi_0(t) = K\omega_it + K\phi_i + \\ + \frac{K}{k_d}I_{C1}(t) + k_I\omega_r \tag{5}$$

At steady state

$$\phi_0(t) = \omega_it + \theta_i + \frac{I_{C1}(t)}{k_0} + \frac{\omega_rk_I}{K} - \frac{\omega_ik_I}{K} \tag{6}$$

So, the phase difference between the reference signal and the output of CCO is obtained as follows

$$\phi_D(t) = \phi_i(t) - \phi_0(t) = \frac{\omega_ik_I}{K} - \frac{I_{C1}(t)}{k_0} - \frac{\omega_rk_I}{K} \tag{7}$$

From (7), it shows that, when the phase lock loop is in the lock state, the difference phase is directly proportional to the frequency of reference input signals ω_i. In addition, it is directly varied to current control of the current control oscillator (CCO)

$$i_{es}(t) = \frac{\omega_ik_d}{K} - \frac{\omega_rk_d}{K} - \frac{I_{C1}(t)}{k_0K} \tag{8}$$

In practice, a block diagram of PLL may be written as Fig. 2

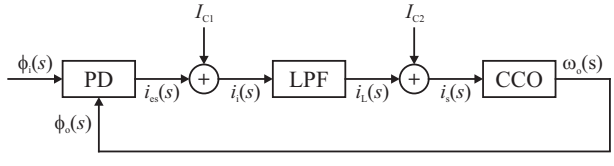

Fig. 2. Block diagram of pll in practical

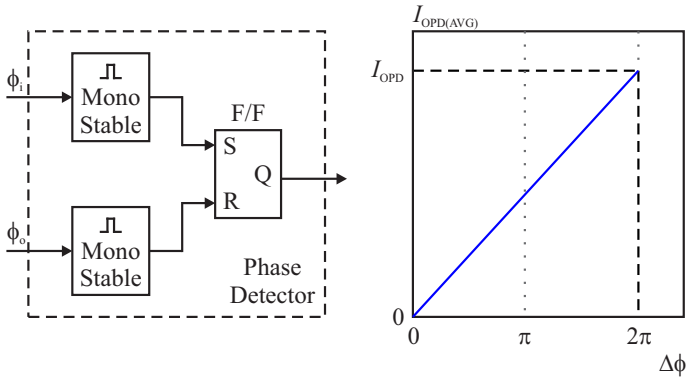

Fig. 3. Block diagram and characteristic of the RS F/F phase detector

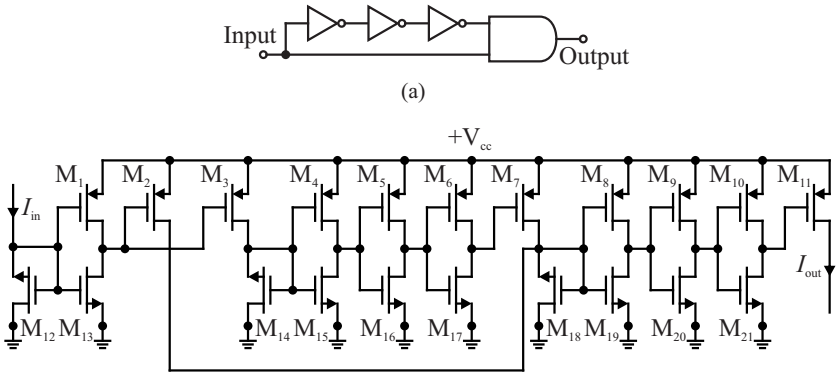

Fig. 4. Monostable Multivibrator

When $P(\phi_D(t))$ is a PWM signal if $P(.)$ is a phase function.

For frequency response from (3) under linearity property if we interested a relation between $I_{C1}(s)$ and $i_L(s)$

$$i_L(s) = F(s)I_i(s) \tag{9}$$

$$i_L(s) = k_d F(s)\phi_i(s) - \frac{k_d k_0 k_I}{s}F(s)(i_L(s)+ + I_{C2}(s)) - \frac{k_d k_I \omega_r F(s)}{s^2} + I_{C1}(s)F(s) \tag{10}$$

$$i_L(s)\left[1 + \frac{F(s)}{s}k_d k_0 k_I\right] = k_d F(s)\phi_i(s) - \frac{k_d k_0 k_I}{s}F(s)I_{C2}(s) - \frac{k_d k_I \omega_r F(s)}{s^2} + I_{C1}(s)F(s) \tag{11}$$

$$i_L(s)\frac{\left[Gs^2 + s + Ak_d k_0 k_I\right]}{s\,(1+Gs)} = \frac{Ak_d\phi_i(s)}{(1+Gs)} - \frac{Ak_d k_0 k_I I_{C2}(s)}{s\,(1+Gs)} - \frac{Ak_d k_I \omega_r}{s^2\,(1+Gs)} + \frac{AI_{C1}(s)}{(1+Gs)} \tag{12}$$

From (12) we have relationship of one output current $(i_L(s))$ and two input current $(I_{C1}(s)$ and $I_{C2}(s))$. Thus, we obtain from two positions to feed current input.

In case 1, we insert input current $(I_{C1}(s))$ between phase detector and low pass filter, and give input current $I_{C2} = 0$. We can find a transfer function between $i_L(s)$ with $I_{C1}(s)$

$$\frac{i_L(s)}{I_{C1}(s)} = \frac{As}{[Gs^2 + s + Ak_d k_0 k_I]} \tag{13}$$

In case 2, we insert input current $(I_{C2}(s))$ between low pass filter and CCO, and set current input $I_{C1} = 0$. The transfer function between $i_L(s)$ with $I_{C2}(s)$ is obtained

$$\frac{i_L(s)}{I_{C2}(s)} = \frac{-Ak_d k_0 k_I}{[Gs^2 + s + Ak_d k_0 k_I]} \tag{14}$$

Which band pass filter and low pass filter is determined from (13) and (14) respectively.

2.2 Phase Detector (PD)

For the phase lock loop, the phase detector is needed to determine the phase difference between the reference signals and the output signals of current control oscillator and feedback to be input for the current control oscillator until feedback loop quiescent and approach to steady state. For phase detector circuit, it can be catalogued to two types such as digital phase detector and analog phase detector. For this here, the digital phase detector is only considered. For XOR gate PD, it achieves 0 - π radian

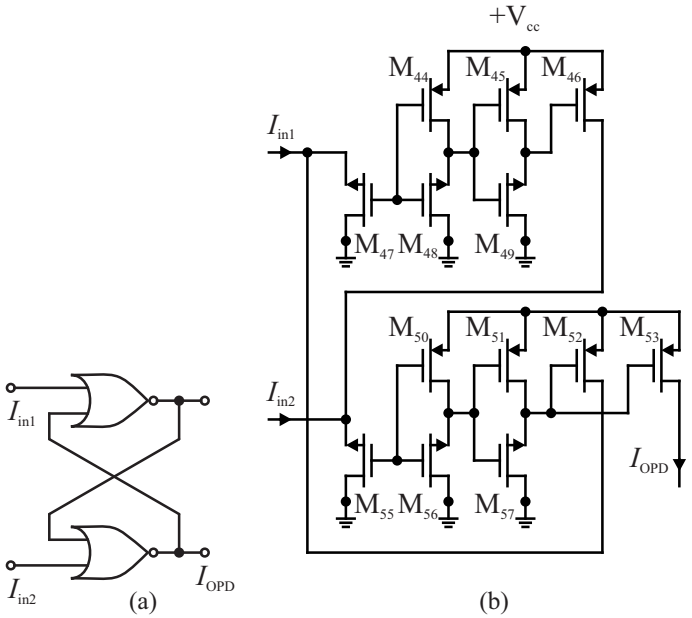

Fig. 5. R-S Flip–Flop Circuit

difference phase and its frequency output is equal a two times of reference signal. While the RS F/F PD gives 0 to 2π radian difference phase and its frequency output is identical to the reference signal and the last one, phase/frequency detector can obtain -2π to 2π radian difference phase.

To detect phase in 0 to 2π radian range, the RS F/F is used. Before the input signal and the reference signal are gotten for finding phase difference, the positive pulse width of both signals are adjusted with monostable multivibrators, then fed as the input of RS F/F which its block diagram is shown in Fig. 3, and this phase detector has a gain k_d

$$k_d = \frac{I_{OPD}}{2\pi} \tag{15}$$

2.2.1 Monostable Multivibrator Circuit

In order to narrow positive pulse width, monostable multivibrators are employed; each individual composes of input current source ($M_1 - M_3, M_{12}$, and M_{13}). The input current is copied to two signals, the first one is delivered from the M_2 and the second one is delivered from M_3, which used the delay of inverter to delay the input signal, then it is fed to cascade three inverters ($M_4 - M_6$ and $M_{15}M_{17}$) and both signals are fed to the input of AND gate ($M_7 - M_{11}$ and $M_{18} - M_{21}$) to generate narrow positive pulse width.

2.2.2 RS Flip–Flop

In this paper, RS flip flop is constructed by using 2 NOR gates to connect as shown in Fig. 5(a) and Fig. 5(b) shown the circuit diagram. The first one of NOR gate is composed of transistor $M_{44} - M_{49}$ and the second one is composed of transistor $M_{50} - M_{57}$ and delivers the output signal at drain of M_{53}.

2.3 Loop filter or Low Pass Filter

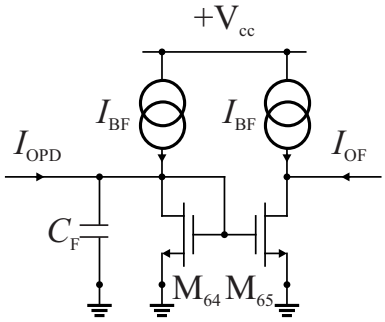

Fig. 6. Current mode first order low pass filter

The loop filter is the one of the important part of phase lock loop. It should filter a high frequency term, and pass the output signals that vary directly with phase difference, which this output signal is used to control the output frequency of the current control oscillator and feedback to the phase detector.

In this paper, the current mode first order low pass filter as shown in Fig. 6, it composes of capacitor C_F and current mirror which its transfer function as follows

$$F(s) = \frac{I_{OF}}{I_{OPD}} = \frac{1}{\frac{C_F S}{gm} + 1} \tag{16}$$

2.4 Current Control Oscillator (CCO)

Generally, the almost PLLs are constructed to operate in voltage mode. So, it uses voltage control oscillator as a one component of PLLs. Nevertheless, in this research, the PLLs operating in current mode is proposed. Therefore, it has to modify VCO to a CCO. Which relaxation CMOS oscillator voltage mode modifies the input signal

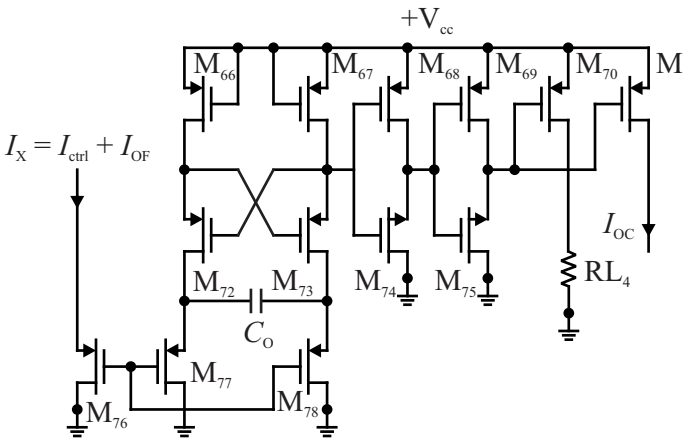

Fig. 7. Source Coupled Current Control Oscillator

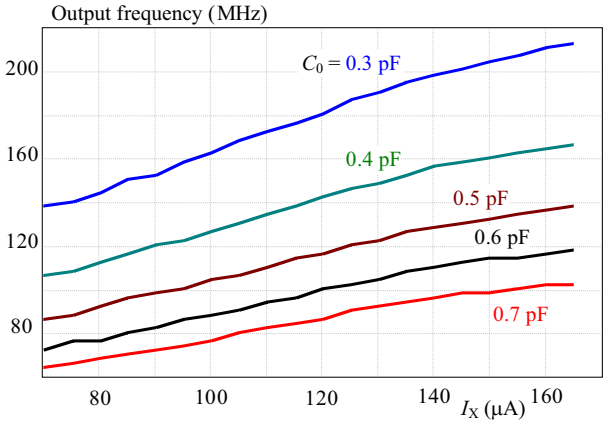

Fig. 8. Characteristic of CCO

as a current with current mirror, for output stage V/I converter by M71 is obtained and its circuit can be shown in Fig.6, which I_X is a summing current between the output current of LPF (I_{OF}) and external current control input (I_{Ctrl}). From Fig. 6, the relationship between frequency output of CCO (f_{OSC}) and I_X is demonstrated as follows

$$f_{OSC} = \frac{1}{2\Delta t} = \frac{I_X/2}{4C_0V_{TH}} \tag{17}$$

$$k_0 = \frac{2\pi}{4C_0V_{TH}} \tag{18}$$

3 Simulation and Results

To obtain current mode PLLs, the phase detector circuit, loop filter or low pass filter, and current control current oscillator are designed and layout chip by the Microwinds program and rule file for CMOS 0.18μm with level-3 process parameter and extract files to simulate by PSPICEs program.

Table 1. Process parameter of CMOS 0.18 μm

Parameter	Typical parameter value		
	NMOS	PMOS	Units
Threshold voltage (VT)	0.35	-0.3	V
Transconductance (K)	345.31	172.65	μA/V2

3.1 Simulation results of the CCO

For CCO simulation, the CMOS circuit as shown in Fig. 7 is simulated with supply voltage VCC = 2.5 V, adjust C_O from 0.3 pF to 0.7 pF with step 0.1 pF and I_X is adjusted from 75 μA to 170 μA, which C_O = 0.3 pF is given 140 MHz to 210 MHz frequency range, C_O = 0.4 pF is given 105 MHz to 165 MHz frequency range, and finally, C_O = 0.7 pF is given a 65 MHz to 100 MHz frequency range as shown in Fig. 8.

3.2 Simulation results of loop filter

Here, the current mode low pass filter is simulated by using the circuit in Fig. 6. Firstly, we use C_F = 10 pF,

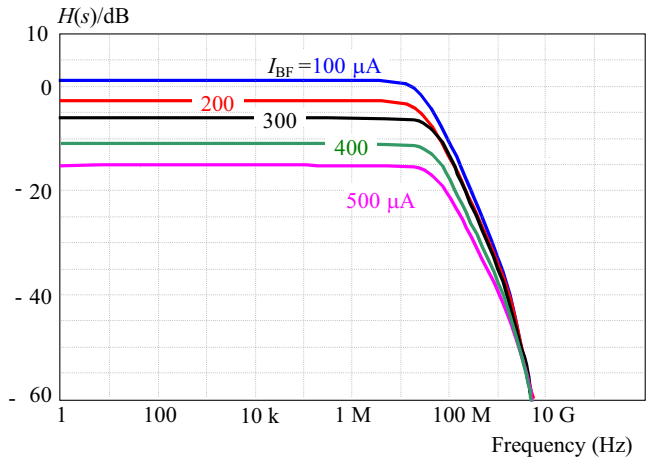

Fig. 9. Frequency response of LPF when varies I_{BF}

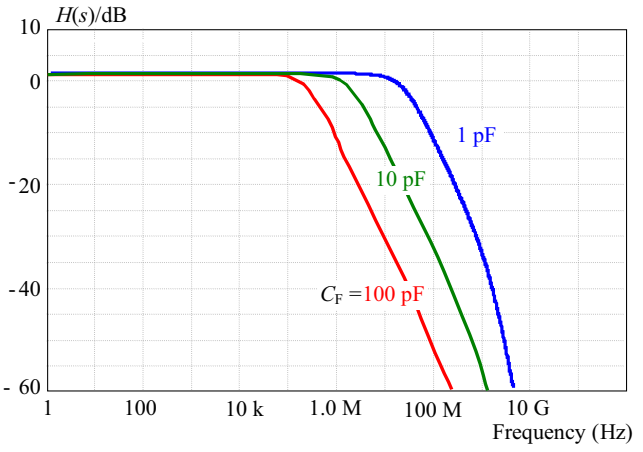

Fig. 10. Frequency response of LPF when varies C_F

Table 2. Transistor aspect ratio

Transistor	W/L (μm)
$M_1, M_5, M_6, M_9 - M_{11}, M_{13}, M_{16}, M_{17}, M_{20} - M_{22}, M_{26}, M_{27}, M_{30} - M_{33}, M_{35}, M_{38}$	
$M_{39}, M_{42} - M_{45}, M_{49} - M_{51}, M_{54}, M_{56}, M_{57}, M_{59} - M_{61}, M_{63} - M_{71}, M_{74}, M_{75}$	0.4/0.2
M_{58}, M_{72}, M_{73}	0.8/0.2
$M_{15}, M_{18}, M_{37}, M_{40}, M_{47}, M_{55}$	1.0/1.0
$M_4, M_{19}, M_{25}, M_{41}$	0.5/1.0
M_{46}, M_{52}, M_{53}	0.4/0.4
$M_2, M_3, M_7, M_{12}, M_{23}, M_{24}, M_{28}, M_{34}$	0.4/1.0
$M_8, M_{29}, M_{77}, M_{78}$	1.0/0.5
M_{76}	2.0/0.5
M_{14}, M_{36}	3.0/3.0
M_{62}	2.0/2.0

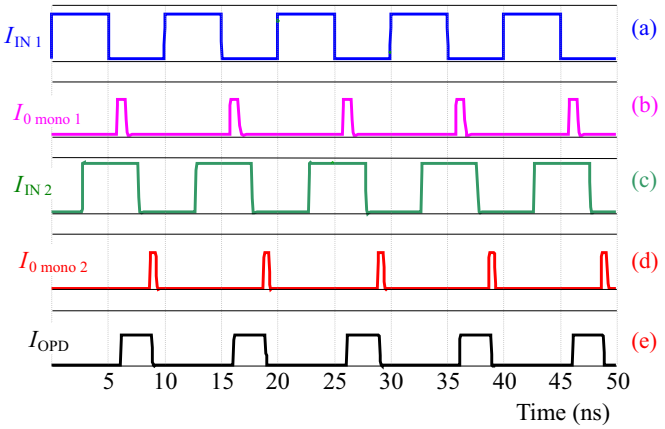

Fig. 11. Results of monostable multivibrator and pd at low phase differences

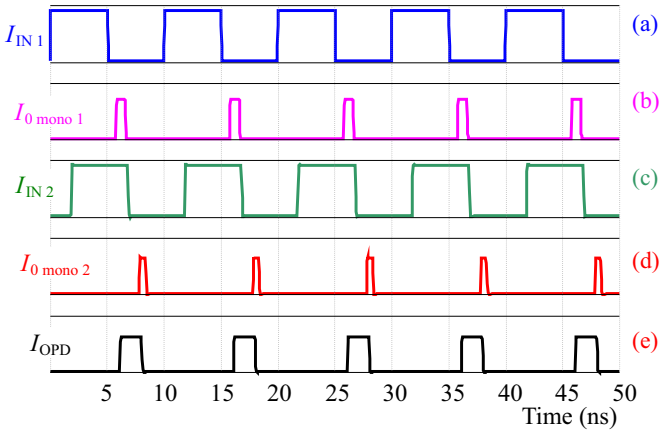

Fig. 12. Results of monostable multivibrator and pd at high phase differences

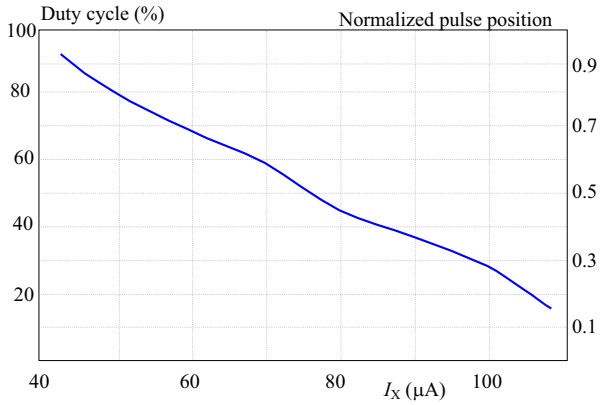

Fig. 13. DC characteristic of PWM/PPM

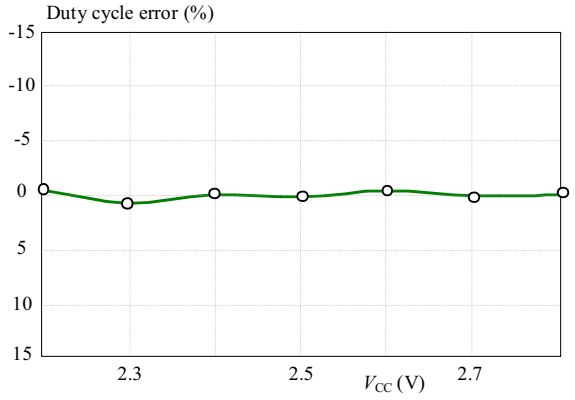

Fig. 14. Effect of power supply to duty cycle of PWM output signal

V_{CC} = 2.5 V and their current control (I_{BF}) are 100 μA to 500 μA with step 100 μA, the result as shown in Fig. 9. The frequency response shown the cutoff frequency is equal to 2.46 MHz, 3.37 MHz, 4.06 MHz, 5.7 MHz, and 7 MHz respectively.

Secondly, the simulation is set by fixing control current (I_{BF}) at 100 μA and step change C_F = 1 pF, 10 pF, 100 pF. The simulation result as illustrated in Fig. 10. In pass band, the current gain of them is equal to 1.24 dB. For the cutoff frequency are 23.89 MHz, 2.42 MHz, and 242.3 kHz respectively.

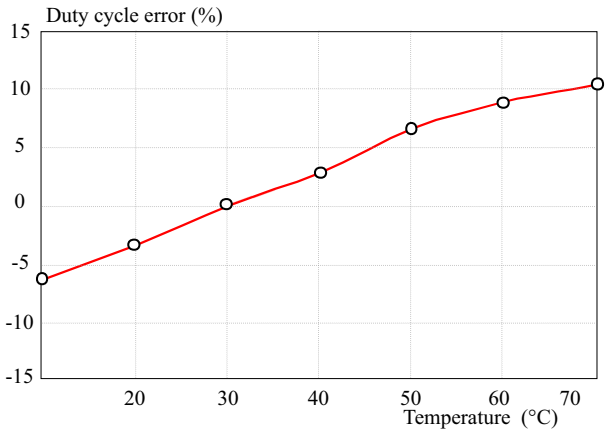

Fig. 15. Effect of temperature to duty cycle of PWM output signal

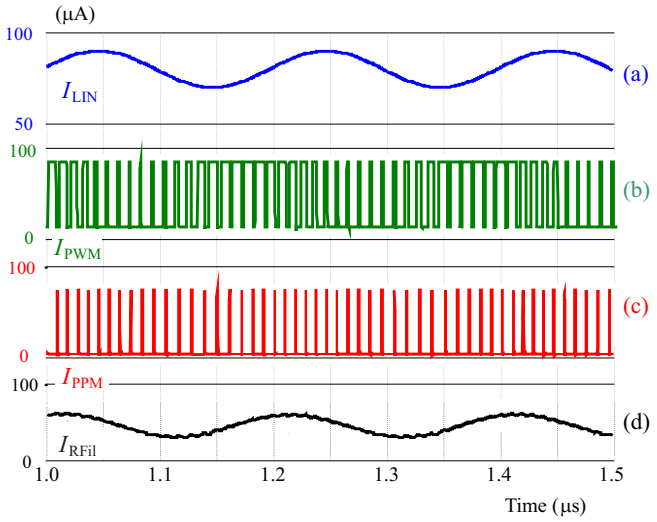

Fig. 16. Simulation results of PWM/PPM signal in time domain

3.3 Simulation result of phase detector

To test characteristic of the phase detector, the circuits from Fig. 4 and Fig. 5 are set up and simulated. The result is shown in Fig. 11 for low phase different and Fig. 12 for high phase different, in signal (a) and (c) are input signals of multivibrator 1 and 2, respectively, signal (b) and (d) are the output of monostable 1 and 2, respectively, It should be noted that, monostable output is triggered with negative rise edge of the input signal and the positive pulse width is 530 ps and signal (e) is an output signal of RS F/F or PD.

3.4 Simulation results of PWM/PPM

In this section, it shows the simulation results of the PWM/PPM based on PLL system by using each part on above (PD, loop filter, CCO) and combined them to PWM/PPM circuit in Fig. 13. Next, it sets all transistors by follow as Tab. 2 with DC supply voltage (V_{cc}) = 2.5 V, running frequency and reference frequency is 100 MHz. From the result of CCO in Fig. 8. It is assigned CO = 0.6 pF for 100 MHz center frequency. In the part of signal input (I_{Ctrl}) is a sine wave at frequency 5 MHz. Thus, the loop filter will be assigned C_F = 10 pF at I_{BF} = 100 μA from the result of loop filter in Fig. 9 and Fig. 10.

Figure 13 shows the DC characteristic of the PWM/PPM circuit between the input signal (I_{Ctrl}) in x-axis with a duty cycle of the pulse or pulse position on the y-axis. The response is a linear negative slope, which can be adjusted the duty cycle from 16% to 93% or shifted the normalized position of narrow pulse from 0.16 to 0.93.

Figure 14 show the effect of power supply variations was also carried out. The supply voltage was varied between 2.2 V and 2.8 V in step 0.1 V. Simulation results shown in Fig. 13 indicate that the duty cycle error of PWM output signal is between ±0.6 %.

Figure 15 shows the Simulation of temperature effects was carried out. The temperature was swept from 10 °C to 70 °C in steps of 10 °C. The simulation result shown in Fig. 14 the error of the duty cycle of PWM output signal is increased from -6% to 10%. It confirms that the propose circuit is sensitive to temperature variations.

Figure 16 has shown the result of PWM/PPM circuit in time domain. The trace of signals from top to bottom. The top trace is a sine wave signal input (I_{Ctrl}) at frequency 5 MHz, current amplitude = 28 μA ppeak-to-peak and offset current = 78 μA. The second trace is a PWM output signal it has a variation of duty cycle between 95% to 1.64%. The third trace is a PPM output signal. The narrow pulse can be shifted between 9.5 to 1.64 ns from the position of a reference signal. The last signal is a demodulate PWM signal or signal from the output of the loop filter.

3.5 Simulation results of frequency response of PWM/PPM system

From the section 2.1, we analyzed a transfer function of the propose system. It is capable to feed into 2 positions. Figure 17 illustrates the comparison results of the frequency response of this system between theory and simulation. In case 1, we feed an external signal between the output of PD and input of the loop filter. Result from (13) and simulation result shows the frequency response is a band pass filter. In case 2, we feed an external signal between the loop filter with CCO. Result from (14) and simulation result shows the frequency response is a low pass filter.

Note that another advantage of this current mode PWM/PPM based on PLL. It doesnt have an offset current input in case 1 and able to use signal input same case 2. The difference in voltage mode, if you feed current input in case 1, you need to decrease the summary of voltage between the voltage output P_D and voltage input signal to less than V_{CC} or logic high.

The analysis frequency response shows that is a BPF or LPF for feeding input at the input and output of the loop filter, respectively, and agree with simulation results.

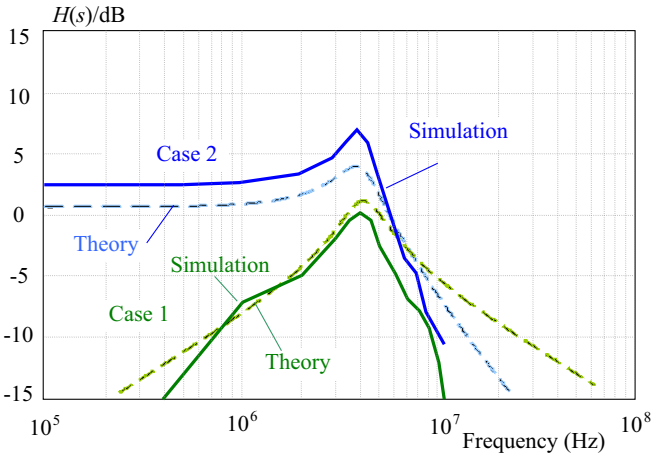

Fig. 17. Frequency response of the PWM/PPM system

4 Conclusions

The fully current mode PWM/PPM based on PLL have been presented in 0.18 μm CMOS technology. The simulation results of current mode PWM/PPM show that it can be operated by using a 2.5 V power supply. The carrier frequency or center frequency can be operated at 100 MHz or more than if change the running frequency of CCO. The responses of the PWM signal in case of DC characteristic, it can be adjusted from 16% to 93% by varying the input control current from 93 μA to 43 μA. In case of AC and DC characteristic, it can be adjusted duty cycle of a PWM signal from 1.64% to 95%. The narrow pulse of PPM signal is equal to 530 ps. The power dissipation of this circuit is 4.68 mW with the total chip area is 28 $\mu \times 60\mu$m. In addition, the PPM and PWM from the propose circuit is not yet depend on the supply voltage.

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