DE GRUYTER OPEN

Journal of ELECTRICAL ENGINEERING, VOL 68 (2017), NO3, 188–193

Novel single-phase five-level inverter utilizing digital counter control scheme

Cajethan M. Nwosu, Anthony I. Umeogamba, Cosmas U. Ogbuka *

A novel single-phase digital control circuit-based five level inverter (FLI) is presented in this paper. Based on the determined switching angle, one switching cycle of the inverter is divided into segments from which the switching sequence of the inverter switches is digitized. A programmed counter built around $J-K$ flip flops with logic gates provided the needed switching signals for the H-bridge inverter. Proposed inverter is verified through simulation in a MATLAB/SIMULINK environment and simulation results are given. Simulation results show notable reduction in total harmonic distortion (THD) in the inverter output voltage and load current. With an RL load (of 200 Ω and 0.250 H), a single digit THD of 8.5 1% for the inverter load current is realized. Comparison of the novel control circuit-dependent FLI with the conventional and contemporary power-circuit-dependent cascaded H-bridge inverter (CHBI) show that the novel FLI is synthesized with lesser number of power circuit and control circuit components.

K e y w o r d s: multi level inverter, switching angle, flip flop, sequential logic circuits, total harmonic distortion

1 Introduction

Cascade multilevel inverter (CMLI) structure has been attracting increasing interests in high power and medium voltage applications owing to its lower harmonics, higher efficiency and lower voltage stress compared to two- or three-level inverters [1], [2], [3], [4]. Diode clamped, flying capacitors, and cascaded H-bridge inverters (CHBI) constitute several multilevel converter topologies presently in use. A cascaded multilevel inverter consists of a series of H-bridge inverters with each H-bridge unit having its own DC source [1] or a single DC source and capacitors-based DC sources [3] for all but the first source.

A cascaded multilevel inverter with k number of DC sources or number of H-bridge cells will provide $(2k+1)$ levels to synthesize the AC output waveform. This means that for a five-level inverter (FLI), two DC sources and two cascaded H-bridge cells are required [5][10]. Where a multicarrier PWM technique is adopted for obtaining the cascade inverter switching signals, $n-1$ carriers with same carrier frequency f_c, and same peak to peak amplitude AC, are also required. For the five-level cascaded inverter in [1] for instance, the additional H-bridge inverter, DC source, and increase in the number of carriers all add to increase in components count and costs that will ultimately lead to increase in switching losses and system size. Several attempts have been made in the recent past by researchers to synthesize the multilevel inverter (MLI) with few number of H-bridge cells, circumventing the $(2k+1)$ levels hypothesis.

Even when high level MLI is to be developed from few number of H-bridge cells, a quite number of auxiliary switches and diodes are usually incorporated in the power circuit resulting in additional control circuit designs for the switches. In [11] for instance, where two H-bridge cells were deployed for an eleven-level cascaded H-bridge MLI, additional four switches and eight diodes were incorporated to realize the design objectives. In the paper, no attempt was made to present the control circuit and its process of design which is predicted to be complex. In all the FLIs developed using a single H-bridge cell [12][24], there are the presence of one or more auxiliary switches and diodes with additional control circuits. For instance, in some schemes two auxiliary switches with two anti-bidirectional diodes, two other diodes through which the capacitors are discharged and two DC voltage sources have been deployed in addition to the single k cell structure [10], [16], [20], [21], [23]. In other schemes, one auxiliary switch, four diodes and either two DC sources or two capacitors across a boost converter have in addition to the single k cell been designed to realize the FLIs output voltages [12], [14], [18], [23]. Due to the complexity of the control circuit structures for the five level inverters, few authors presented the control scheme while many others made little or no attempt to discuss the processes of the control circuit designs.

In all, the realizations of the five level inverters were all power circuit-based. The desired levels of harmonics reduction informed the different choices of the control circuit designs by the authors. It is quite anticipated that if the realization of the FLI is control circuit-based utilizing the single H-bridge cell without auxiliary power components rather than power circuit-based utilizing the single H-bridge cell with additional power circuit components, the resulting inverter will be smaller, lighter, and simpler, implying greater reliability, lower cost and power conservation.

* Department of Electrical Engineering, University of Nigeria, Nsukka, cajethan.nwosu@unn.edu.ng

DOI: 10.1515/jee-2017–0027, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

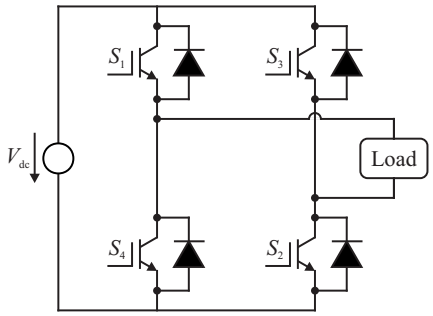

Fig. 1. Single phase h - bridge voltage source inverter, VSI

In this paper, a control circuit-based novel five-level inverter utilizing digital counter built around $J-K$ flip-flops in the generation of the switching signals for a single H-bridge cell without auxiliary power components is proposed.

2 Proposed five level inverter

A control circuit-based novel five-level inverter utilizing digital counter in the generation of switching signals for a single-phase inverter has been proposed to circumvent further addition of power switches to the conventional H-bridge inverter cell when compared to the attempts made by recent researchers to achieve similar results using the H-bridge cell but with additional auxiliary power switches as has been x-rayed above. A single-phase H-bridge five level inverter topology is shown in Fig. 1. The circuit consists of four switching devices S_1, S_2, S_3, and S_4, with two devices each in one leg of the two-leg inverter. The inverter uses a pair of complimentary controlled switches in each inverter leg, *ie* (S_1, S_2) and (S_3, S_4). The two switches in each leg operate in a complimentary pair to avoid short circuiting of the dc source.

The FLI output is a staircase waveform derived from the conventional single phase modified sine-wave inverter having α as angle of zero voltage between the positive and negative half-cycles of the inverter output. Generally, the number of switching angles in a quarter cycle of a staircase voltage waveform is limited to s. The number of harmonics, therefore, that can be eliminated in the waveform is limited to $s-1$. For the FLI output voltage waveform, only two switching angles are there in a quarter of a cycle which translates to the fact that only one harmonics can be eliminated. The two switching angles as denoted by α_1 and α_2 in Fig. 2 can be calculated from [16]

$$\alpha_i = \sin^{-1}\left[\frac{2i-1}{n-1}\right] \tag{1}$$

where $i = 1, 2, 3, \ldots \left(\frac{n-1}{2}\right)$, and n is the number of output voltage level.

3 Design of switching control of the inverter

As stated previously, the novel five-level inverter presented in this paper is derived from control design for quasi-sine wave inverter where one switching cycle of the inverter is divided into $g = \pi/\alpha$ segments with the width of each segment obtained as 2α. The switching signals for the inverter top switches are assigned nomenclatures such that S_1, $S_3 = A\ B =$ "1 1", while switching signals for the inverter down switches are assigned nomenclatures such that S_2, $S_4 = \overline{A}\ \overline{B} =$ "0 0". These switches are fired in the sequence $S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$. Sequencing events like this is a function for which a digital circuit may

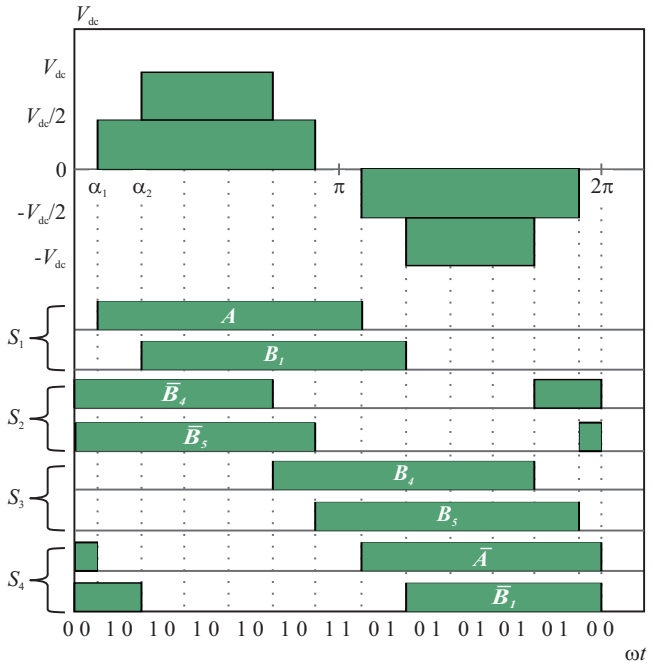

Fig. 2. Inverter switching instants showing segments with repeated states corresponding to output voltage pulses

be designed. Sequencing events can be realized using digital counters. In this paper, a digital programmed counter built around $J-K$ flip flops is deployed to achieve the switching sequence.

Using (1), value α_1 of 14.48 deg was obtained. However, α_1 of 15 deg is selected from which twelve segments of of $\pi/6$ or 30 deg each for one switching cycle is obtained as shown in Fig. 2. As can be observed from Fig. 2, the states "0 0" and "1 1" corresponding to zero level voltages are not repeated while the states "1 0" and "0 1" corresponding to the positive and negative output pulses respectively are each repeated five times. The flow graph and the transition table showing the switching sequence for the single phase inverter are shown in Fig. 3. Employing $J-K$ flip flop in the combinational logic circuit design, the state transition table is generated as shown in Table 1. As can be observed from the state transition table, the J_A and K_A flip flop will require only one block while the J_B and K_B flip flop will need five blocks.

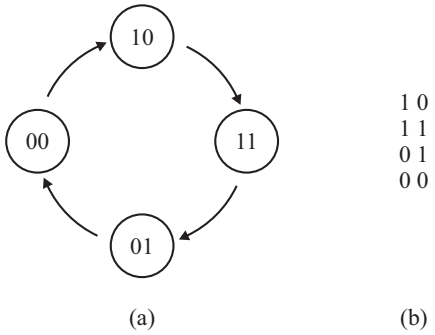

Fig. 3. Switching sequence for the single phase inverter (a) – flow graph (b) – state transition

The characteristic equation from the state transition table is obtained as

$$J_A = \overline{A}\,\overline{B}, \quad K_A = A\,\overline{B}, \qquad J_B = \overline{A}\,B, \quad K_B = \overline{A}\,B \tag{2}$$

Utilizing two variable Karnaugh map for the simplification of the characteristic equation, we obtain

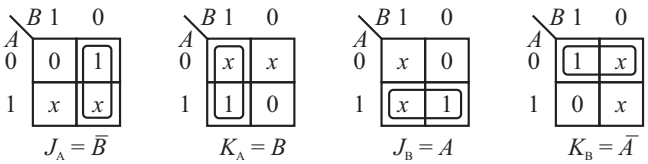

Fig. 4. Karnough maps and the accompanying simplified characteristic equations

The programmed counter control circuit diagram using $J-K$ flip flops is shown in Fig. 5. In setting out the $J-K$ flip flop based switching circuit, the number of repeated states and their location in the required excitation for the next state inside the state transition table, determine the number of blocks of the flip flop and the output terminals to which the inverter switches are connected.

Table 1. State transition table

State				Required excitation for the next state			
Present		Next					
A	B	A*	B*	J_A	K_A	J_B	K_B
0	0	1	0	1	x	0	x
0	1	0	0	0	x	x	1
1	0	1	1	x	0	1	x
1	1	0	1	x	1	x	0

4 Operation principle of the proposed five-level inverter

With the aid of Fig. 2 and Fig. 5, the switching states and the output voltages of the FLI is developed as shown in Table 2. The logic OR-gates as seen in Fig. 5 created the platform for the synthesis of the five-level output voltage of the inverter. Switches S_1 and S_2, for example, must be ON complimentarily in order for the V_{dc} to appear across the load as output voltage. In segment 1, switching signal S_2 is fully supplied with the logic "1 1" while S_1 is semi supplied with the logic "1 0" through the action of the OR-gates hence the output voltage $V_{\mathrm{dc}}/2$. In segment 2, the switching signals S_1 and S_2 receive full

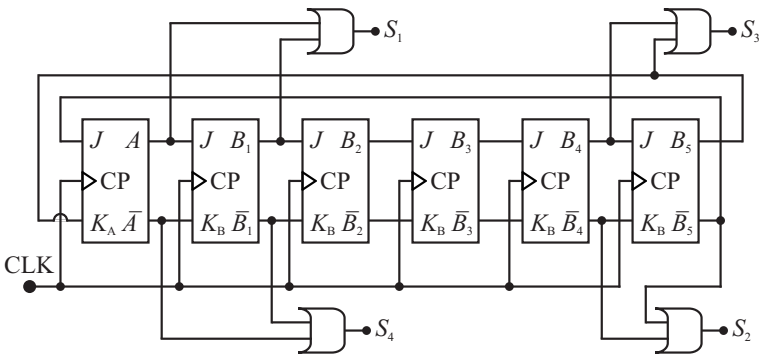

Fig. 5. Programmed counter built around $J-K$ flip flops for the inverter switches

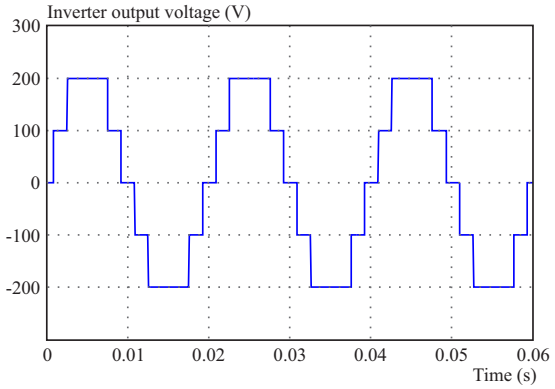

Fig. 6. Inverter output voltage

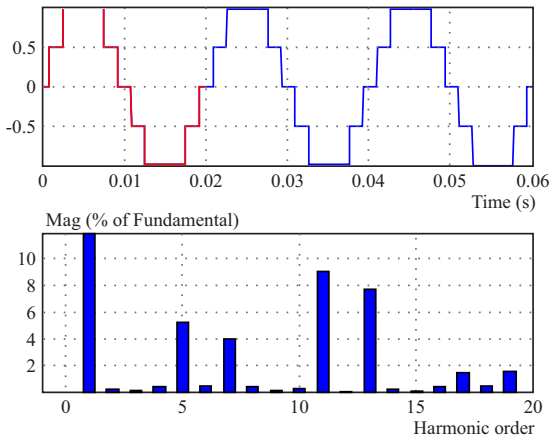

Fig. 8. FFT analysis of inverter load current with R load

Table 2. Switching states and output voltage

Segment									Output
1	1	0	0	0	1	1	0	1	$V_{\mathrm{dc}}/2$
2	0	0	0	0	1	1	1	1	V_{dc}
3	0	0	0	0	1	1	1	1	V_{dc}
4	0	0	0	0	1	1	1	1	V_{dc}
5	0	0	0	1	1	0	1	1	$V_{\mathrm{dc}}/2$
6	0	0	1	1	0	0	1	1	0
7	0	1	1	1	0	0	1	0	$-V_{\mathrm{dc}}/2$
8	1	1	1	1	0	0	0	0	$-V_{\mathrm{dc}}$
9	1	1	1	1	0	0	0	0	$-V_{\mathrm{dc}}$
10	1	1	1	1	0	0	0	0	$-V_{\mathrm{dc}}$
11	1	1	1	0	0	1	0	0	$-V_{\mathrm{dc}}/2$
12	1	1	0	0	1	1	0	0	0

logic supplies of "1 1" each hence the output voltage V_{dc} and because this same switching states are sustained in the next two following segments, the output voltage V_{dc} is maintained across the load. In segment 5, the switching signal S_1 still receives full logic supplies of "1 1" while the switching signal S_2 receives the logic "0 1" hence output voltage drop from V_{dc} to $V_{\mathrm{dc}}/2$. In segment 6, the signals S_1 and S_3 receive full logic supplies to close the corresponding adjacent switches on the two legs of the inverter and the load voltage is zero.

Similar results can be traced for the switches S_3 and S_4 responsible for the negative inverter output voltage between segments 7 and 12.

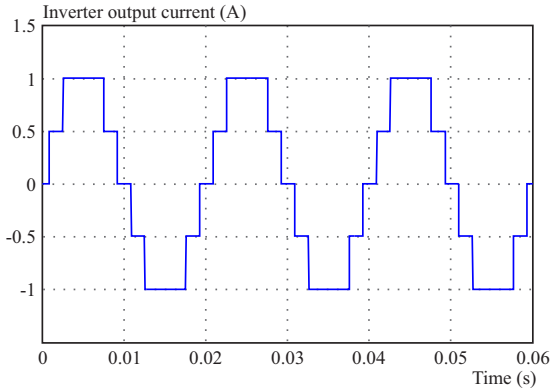

Fig. 7. Inverter load current with R load

5 Simulation and results

In this paper, the simulation model is developed with MATLAB/SIMULINK. The inverter circuit was simulated with R load of 200Ω and RL load of 200 Ω and 0.250 H respectively and with V_{dc} of 200V. The inverter output voltage is shown in Fig. 6 while the load current is shown in Fig. 7 with R load. The corresponding FFT analysis of the inverter load current is shown in Fig 8. The output voltage and load current both have a THD of 16.84% with R load.

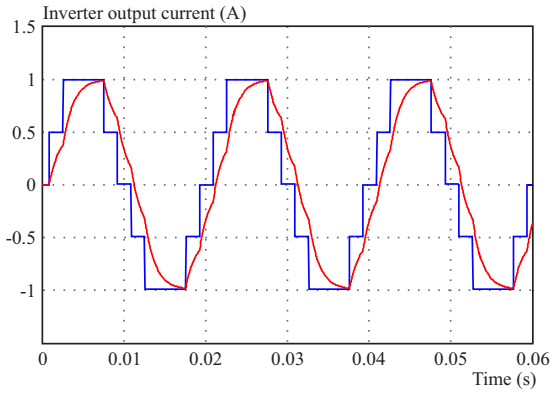

Fig. 9. Inverter load currents with R load and RL load

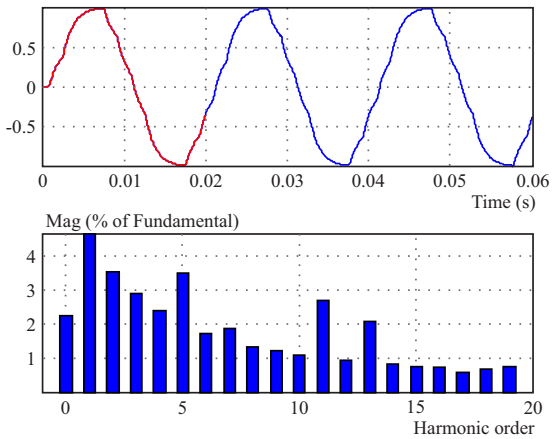

Fig. 10. FFT analysis of inverter load current with RL load

In Fig. 9, the load currents with R load and with RL load are displayed. The FFT analysis of the inverter

load current with RL load is shown in Fig 10. With the RL load, the THD has been reduced from the two digit number to a single digit number of value 8.51%.

Comparisons between switch number n, auxiliary diodes, DC source number and switching frequency for the cascaded H-bridge inverter CHBI, improved cascaded H-bridge inverter ICHBI, and the proposed novel H-bridge inverter NHBI are given in Table 3.

Table 3. Comparison between cascaded H-bridge, improved, cascaded H-bridge and novel H-bridge inverters

	CHBI	ICHBI	NHBI
Switches	$2(n-1)$	$n, n+1, n+2$	$n-1$
Auxiliary diodes	-	2 or 4	-
DC sources	2	2	1
Switching frequency	?kHz	?kHz	600 Hz

6 Conclusions

In this paper, a novel single-phase digital control-circuit-based five level inverter has been presented. One cycle of the inverter output voltage is divided into 12 segments of $\pi/6$ from which the switching sequence of the inverter switches is established. Employing a programmed counter built around $J-K$ flip flops the switching sequence is digitized, and the logic combinations of the digital flip-flop outputs using OR-gates provided the platform for the synthesis of the five-level output voltage of the inverter. The simulation model of the proposed FLI is developed and verified through simulation in MATLAB/SIMULINK environment. From the harmonic analysis of the inverter output voltage and load current it is observed that the choice of 15 deg switching angle led to significant reduction in the triple harmonics hence improved THD. For an R load of $200\,\Omega$, the simulation results show a total harmonic distortion of 16.84% in the inverter output voltage and load current. With an RL load (of $200\,\Omega$ and 0.250 H), a single digit THD of 8.51% is realized for the inverter load current. Comparison of the novel control-circuit-based FLI with the conventional as well as contemporary power-circuit-based cascaded H-bridge inverters show that the novel FLI is synthesized with lesser number of power circuit and control circuit components. With one DC source, one H-bridge structure, simple control logic and low switching frequency, the novel FLI has comparative advantage with better efficiency, reduced weight and reduced losses.

References

[1] P. V. Kumar, Ch. S. Kumar and K. R. Reddy, "Single Phase Cascaded Multilevel Inverter using Multicarrier PWM Technique", *Journal of Engineering and Applied Sciences*, vol. 8, pp. 796 - 799, 2013.

[2] K. S. Reddy and Ch. V. Kumar, "Implementation of a single-phase Multilevel Inverter with Battery balancing", *International Journal of Electrical and Electronic Engineering*, vol. 1, pp. 35 - 39, 2014.

[3] E. Beser, B. Arifoglu, S. Camur and E. K. Beser, "Design and Application of a Single Phase Multilevel Inverter Suitable for using as a Voltage Harmonic Source", *Journal of Power Electronics*, vol. 10, pp. 138 - 45, 2010.

[4] W. S. Oh, S. K. Han, S. W. Choi and G. W. Moon, "Three phase three-level PWM switched voltage source inverter with zero neutral point potential", *IEEE Trans. on Power Electronics*, vol. 21 pp. 1320 - 1327, 2006.

[5] B. M. Veena and M. T. Triveni, "H", *dware Implementation of 5 Level Inverter Using Microcontroller*, International Journal of Advanced Research Electrical, Electronics and Instrumentation Engineering, vol. 5, no. 1, pp. 175 - 182, 2016.

[6] P. V. V. R. Rao, P. D. Kiran and A. P. Kumar, "Hybrid 5-level inverter fed induction motor drive, ", *World Journal of Modelling and Simulation*, vol. 10, no. 3, pp. 224 - 230, 2014.

[7] B. Ismail, S. I. S. Hassan, R. C. Ismail, A. R. Haron and A. Azmi, "Selective Harmonic Elimination of Five-level Cascaded Inverter Using Particle Swarm Optimization, ", *International Journal of Engineering and Technology (IJET)*, vol. 5, no. 6, pp. 5220 - 5232, 2014.

[8] P. Iraianbu and M. Sivakumar, "A Single Dc Source Based Cascaded H-Bridge 5- Level Inverter, ", *International Journal of Innovative Research Science*, Engineering and Technology, vol. 3, Special no. 1, pp. 995 - 1000, 2014.

[9] B. C. Vinayaka and S. N. Prasad, "Modeling and Design of Five Level Cascaded H-Bridge Multilevel Inverter with DC/DC Boost Converter, ", *Int. Journal of Engineering Research and Applications vol. 4*, no. 6, pp. 50 - 55, 2014.

[10] M. S. Sivagamasundari and P. M. Mary, "Sinusoidal PWM Based Cascaded H-Bridge Five Level Inverter Using Fuzzy Logic Controller, ", *Journal of Applied Sciences*, vol. 14, pp. 3486 - 3492, 2014.

[11] M. V. Kumar and B. Naresh, "A Novel Single Phase Eleven-Level Grid-Connected Transformerless Converter Topology for PV Systems, ", *International Journal of Science and Research (IJSR)*, vol. 4, no. 9, pp. 375 - 380, 2015.

[12] R. An,, A. N. Ali, "A Single phase Five level Inverter for Grid Connected Photovoltaic System by employing PID Controller, ", *African Journal of Scientific Research*, vol. 6, no. 1, pp. 306 - 315, 2011.

[13] S. Yogesh, K. G. Prasad, S. Ramesh and R. Ramesh, "Five-Level Full-Bridge Single-Phase Grid Connected Converter for Renewable Distributed Systems, ", *International Journal of Advanced Research Electrical*, Electronics and Instrumentation Engineering, vol. 3, no. 8, pp. 11327 - 11333, 2014.

[14] M. P. Kumar and A. S. H. Babu, "A Five Level Inverter for Grid Connected PV System Employing Fuzzy Controller, ", *International Journal of Modern Engineering Research (IJMER)*, vol. 2, no. 5, pp. 3730-3735, 2012.

[15] G. Balasundaram and S. Arumugam, "Implementation of Five Level Inverter Considering PV System Using MPPT Technique, ", *ARPN Journal of Engineering and Applied Sciences*, vol. 10, no. 4, pp. 1552 - 1557, 2015.

[16] S. Camur, B. Arifoglu, E. Beser and E. K. Beser, "A Novel Topology For Single-Phase Five-Level Inverter, ", *Proc. of the 5th WSEAS/IASME Int. Conf. on Electric Power Systems*, High Voltages, Electric Machines, Tenerife, Spain, December 16-18, pp. 314 - 319, 2005.

[17] P. R. Ch,ran, T. Jothi, "A Multisource Five Level Inverter using an Improved PWM Scheme, ", *International Journal of Science and Research (IJSR)*, vol. 2, no. 6, pp. 279 - 282, 2013.

[18] J. M. Shen, H-L, Jou, J-C, Wu, K-D and Wu, "Five-Level Inverter for Renewable Power Generation System, ", *IEEE Trans. on Energy Conversion*, vol. 28, no. 2, pp. 257 - 266, 2013.

[19] S. Boilla and P. Varunkrishna, "Modelling of Five-Level Inverter for Renewable Power Source, ", *International Journal of Electrical and Electronics Engineering (SSRG-IJEEE)*, vol. 1, no. 7, pp. 17 - 21, 2014.

[20] S. N,ini, R. S. Zachariah, "Performance Analysis and Simulation of a Five Level Inverter with Coupled Inductors, ", *International Journal of Computer Applications*, vol. 92, no. 15, pp. 22 - 26, 2014.

[21] L. Jose and S. N. Raj, "A Novel Single Phase Five Level Inverter With Coupled Inductors And Closed Loop System, ", *International Journal of Scientific & Technology Research*, vol. 3, no. 6, pp. 293 - 298, 2014.

[22] M. S. Sivagamasundari and P. M. Mary, "Analysis of Cascaded Five Level Multilevel Inverter Using Hybrid Pulse Width Modulation, ", *International Journal of Emerging Technology and Advanced Engineering*, vol. 3, no. 4, pp. 55 - 58, 2013.

[23] D. Subramanian and R. Rasheed, "F", *e Level Cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique*, International Journal of Engineering and Innovative Technology (IJEIT), vol. 3, no. 1, pp. 438 - 441, 2013.

[24] N. Kashappa and R. K. Ramesh, "Implementation of a Low Cost 5 Level PWM Inverter, ", *Global Journal of Researches Engineering Electrical and Electronics Engineering*, vol. 13, no. 9, pp. 45 - 48, 2013.

Received 7 March 2016

Cajethan Nwosu (Engr, Dr) was born in 1967. He obtained the BEng, MEng and PhD Degrees in Electrical Engineering from the University of Nigeria, Nsukka in 1994, 2004 and 2015 respectively. From 1995 to 1996, he worked as a Project Engineer with I. O. International Power Line Construction Company Nig. Ltd. From 1997 to 2000, he was the Director of Cee Jay Engineering Services. From 2002 to 2003 he was a Resource Teacher, In-House Training Programme University of Nigeria. In 2007, he undertook a three months pre-doctoral research on Wind/Solar Hybrid Power System and Renewable Energy Resources at the University of Technology, Delft (TU-Delft), the Netherlands. Since 2005, he has been with the Department of Electrical Engineering, University of Nigeria, Nsukka, where he is currently a Senior Lecturer. He had written two books and had published over thirty articles both in local and international journals. He is the executive vice-chairman of Nigerian Institution of Electrical and Electronic Engineers (NIEEE), Nsukka chapter. He is a member of Power Electronics Society of Institution of Electrical and Electronic Engineering (PES IEEE). He is an editorial board member World Science Journal of Engineering Applications. His areas of research interest include power electronic converters, electrical drives and renewable energy technologies.

Anthony I. Umeogamba was born in Anambra State, Nigeria. He received the Bachelor of Engineering and Master in Engineering Degrees in Electrical Engineering from University of Nigeria, Nsukka in 2010 and 2016 respectively. He is currently involved in research programme on electric motor drives, power inverters, STATCOM and renewable energy.

Cosmas Ogbuka (Engr, Dr) was born in Umuna Nigeria on 1st April, 1981. He received his BEng (First Class Honors), MEng (Distinction) and Doctor of Philosopy PhD in 2004, 2009 and 2014 respectively in the Department of Electrical Engineering University of Nigeria, Nsukka. He is the General Secretary, the Nigerian Institution of Electrical and Electronic Engineers (NIEEE) Nsukka Branch. Member, Electrical and Power Systems on IEEE Journal (Editorial Advisory Board) in Nigeria, January 2011 till Date. Member, Nigerian Society of Engineers (NSE), Registered Engineer, Council for the Regulation of Engineering in Nigeria (COREN), member, International Research and Development Institute (IRDI), member, International Association of Engineers (IAENG), member, World Association of Young Scientists (WAYS). His research interests are in Adjustable Speed Drives of Electrical Machines: (DC and AC Electric Machine Torque/Speed Control with Converters and Inverters), Electric Machines and Power Electronics.