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PAPERS

A design methodology for programmable-gain low-noise TIA in CMOS

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The work reports on the design of an area-efficient inductor-less low-noise CMOS transimpedance amplifier suitable for entry-level optical time-domain reflectometers. The work suggests a novel approach for implementing a programmable-gain in capacitive feedback TIA with an independent adjustment of the low- and high-frequency behavior using the input stage biasing impedance and one of the feedback capacitors. The approach addresses a typical noise problem of fast feed-forward or resistive feedback topologies while alleviating the trade-off of the key TIA performance indicators. A more accurate amplifier model is proposed which takes into account the effects due to capacitive isolation and both biasing circuits. Further modifications to the reference design are suggested including the PMOS-based implementation of the biasing circuit to address the voltage headroom issue. The circuit was implemented using a standard 180 nm CMOS process and operates from 1.8 V supply with the drawn current of 11.7 mA.

K e y w o r d s: analog integrated circuits, broadband amplifiers, CMOS integrated circuits, optical time-domain reflectometry, transimpedance amplifier (TIA)

1 Introduction

The tremendous growth of the Internet traffic in recent years had led to a rapid development of broadband optical communication systems. The data transmission in optical domain provides a number of advantages such as security, an excellent trade-off of achievable data rates and the transceiver complexity, power efficiency, cross-talk and unregulated bandwidths [1-3]. Nevertheless, the communication systems based on optical fibers may still suffer from mechanical, environmental and natural deterioration. Some of these problems can be prevented by monitoring the optical fiber in real-time and identifying the locations of the faults as quick and accurately as possible, so that an immediate recovery can be achieved or corresponding technical measures can be taken [4]. One of the typically used instruments is the optical Time-domain reflectometer (OTDR) [5,6]. The instrument is used for characterization and fault detection in optical fibers and it operates by injecting a series of optical pulses into the fiber under test. As the pulses are reflected due to inherent scattering mechanisms or faults in the fiber, those are recorded by the instrument at the very same end of the fiber and the accurate location of the fault in the fiber as well as the nature of the fault can be obtained from the analysis of the reflected signals in time domain.

Similar to optical receivers designed for high-speed data transmission, the front-end structure of a classical OTDR device includes the front-end Transimpedance Amplifier (TIA) and its sensitivity, if insufficient, can limit the overall performance of the instrument. Although numerous TIA designs in CMOS have been proposed in last decades (see [7,8] for an overview of recent designs), most of them have been designed with respect to the requirements of classical optical data transmission. Here, the fiber characterization with OTDR puts a slightly different context on the specification of the circuit with additional performance constraints to be considered. Among those one may mention phase response, low noise and the linearity of the output as well as the flatness of the passband.

The most typical TIA is a so-called resistive shunt-feedback TIA [7] which got extremely popular due to its beneficial feedback structure, simplicity, flexibility and relatively good balance between the most important performance measures such as noise levels, gain and bandwidth [9]. Although a large number of modifications have been proposed to this reference architecture, not all inherent limitations of the TIA can be addressed with these adjustments. An issue while using this TIA comes from the requirement to operate with the off-chip photodetectors (PD) of large capacitance C_{IN} which affects the dominant TIA pole. Although high-speed common-gate (CG) [10] or regulated cascode (RGC) [11,12] TIA configurations are able to address this issue, they introduce the problems on their own such as typically higher noise levels when compared to the baseline TIA [13], even though the noise performance of the basic resistive shunt-feedback TIA itself is often insufficient due to noise component from the feedback resistor. An inductive peaking is an-

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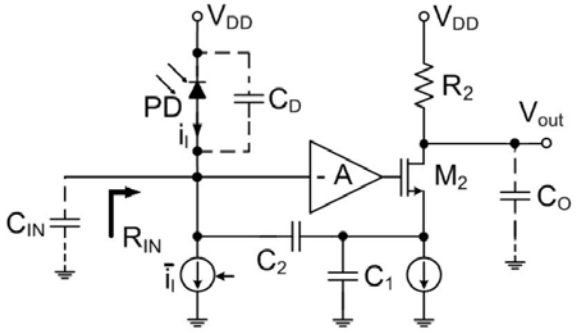

Fig. 1. Basic configuration of capacitive feedback TIA

other approach to increase the bandwidth without sacrificing noise and which has been widely adopted for low-voltage low-power broadband amplifiers. Unfortunately, a practical need to have an area-efficient solution with flat frequency response (with OTDR requirement opting for < 0.5 dB) may also limit application of extensive bandwidth enhancement techniques [14,15]. Furthermore, inductors may also lead to design challenges as it may be hard to keep their inductive characteristics over the complete bandwidth and higher cross-talks may appear due to substrate coupling. For the envisioned TIA bandwidth of 1 GHz the bandwidth extension techniques using inductor peaking may also render themselves redundant as the achievable speed of available general-purpose CMOS is already sufficient for inductor-less implementation.

Although a number of works have reported design of programmable- or variable-gain CMOS TIA, those have been typically implemented either using classical shunt-feedback TIA [16,13] or feed-forward approaches [17,18]. In the former case the adjustable feedback resistance is typically used to control the gain. However, a single adjustable parameter often tends to result in suboptimal amplifier configurations as it may be insufficient to adjust both the high- and low-frequency behavior of the circuit. Typically, the reported approaches will posseses the very same drawbacks as their constant-gain versions such as gain-bandwidth and noise-power trade-offs as well as increased noise levels in fast feed-forward designs.

Only several works tried to address a problem of designing a CMOS TIA specifically for OTDR instruments. As the market volume for OTDR instruments is relatively small, especially when compared to optical communication systems, the OTDR amplifiers were often implemented from discrete components with lower bandwidth (typically below 100 MHz) with the performance limited by the parasitic capacitances [6]. A clear advantage of a completely integrated CMOS TIA is not only due to reduction in all the parasitic capacitances and increased bandwidth when compared to discrete implementations, but also an ability to design a TIA which exactly matches the specification as the latter is unlikely to happen with commercially available CMOS TIAs. As we show below, a single integrated CMOS TIA also nicely scales for programmable-gain application where it is extremely unlikely to find a fully matching TIA chip for all the required gain configurations.

The work [6] proposed a programmable-gain fully differential TIA using a classical resistive feedback topology. The programmable gain was implemented with switchable feedback resistors connected in series using single-pole double-throw switches to reduce input parasitic capacitance with five resistor pairs needed to achieve the target range of feedback resistances. The reported bandwidth was from 6 MHz at the gain of 118 dBΩ to 125 MHz at the gain of 87.25 dBΩ with more than 30% of the topology area occupied by the feedback resistors. Several recent works also reported integration of TIA into a complete lower performance OTDR ASICs [4], SoC solution [2] and even on integration of the OTDR functionality directly in the optical transceiver modules [19]. However, in all the cases the authors employed classical TIA topologies such as resistive shunt-feedback TIA with a priority set for higher integration rather than on the performance of the front-end TIA itself.

Due to tight inherent relationship between the achievable dynamic range, gain of the instrument and the responsivity of the PD, the OTDR instrument requires an implemention of the front-end TIA with different gain-bandwidth configurations supporting detection of extremely weak optical signals. The work presents a design methodology for a programmable-gain capacitive feedback TIA and applies it for design of CMOS TIA with 10 kΩ base level gain at the bandwidth of 1 GHz and input-referred noise density below $5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ while consuming less than 50 mW from 1.8 V power supply. The programmable-gain configuration supports additional gains of 25, 100, 200 and 500 kΩ with no specific requirements on achievable bandwidth and noise. The rest of the paper is organized as follows. The design methodology and concepts along with a detailed discussion on the model for capacitive feedback programmable-gain TIA are presented in Section 2. The results of analytical modeling and simulation are described in Section 3 for both fixed- and programmable-gain configurations. Section 4 concludes this work.

2 Design methodology

Classical resistive-feedback TIA has an inherent problem with the noise performance of the feedback resistor RF as it is directly added to the input-referred noise current and, therefore, drastically degrades the noise performance. Furthermore, the design clearly tradeoffs among the key TIA parameters such as noise, gain and bandwidth. On the other hand, the feedback approach itself has important structural benefits as it ensures almost constant transimpedance gain in the bandwidth of interest while decreasing the sensitivity to process and temperature variations [20]. Thus, it may be beneficial to keep the general feedback structure of the amplifier, while substituting the noisy feedback resistor with a less noisy or

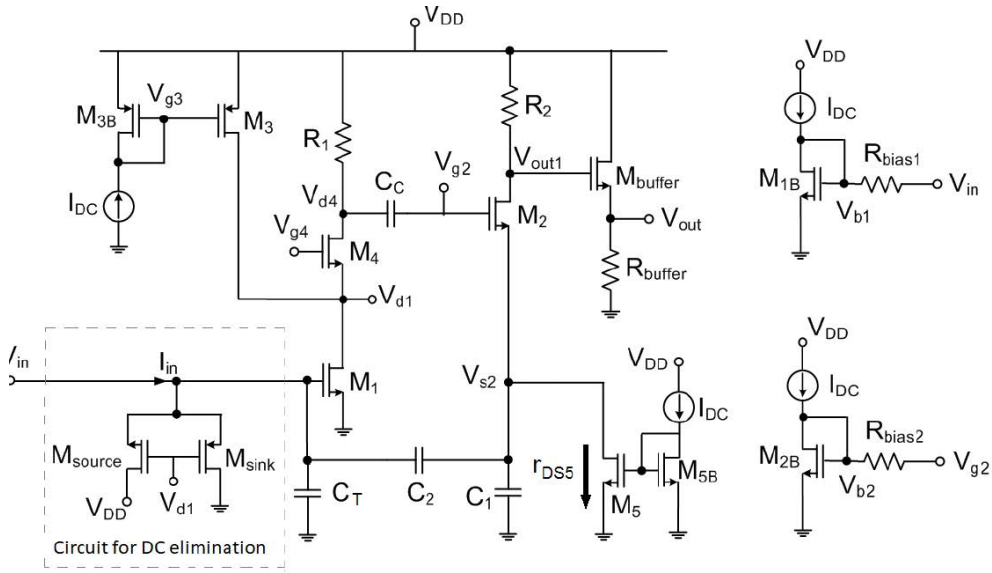

Fig. 2. An implementation of a fixed-gain capacitive feedback TIA and resistive biasing circuits. For simplicity, the PDs capacitance and the input capacitance are replaced with a single capacitance C_{T}

completely noise-free element. An intuitive candidate for such a noise-free element is a capacitor. However, a direct replacement of feedback resistor with a capacitor will result in a phase shift which requires a subsequent stage for phase correction [21]. In this work we follow an alternative approach from [22] and shown in Fig. 1. This generic solution employs the voltage amplifier, the second stage with M_2 and a capacitive feedback network formed by C_1 and C_2.

In this topology, the amplifier maintains a virtual ground at the input node and hence the signal current flows through C_2. The capacitor C_2 senses the voltage across the first feedback capacitor C_1 and the current proportional to the sensed voltage is returned to the input of the amplifier. Under the assumption $A \gg 1$, the resultant current gain can be approximated as

$$\frac{I_{\mathrm{out}}}{I_{\mathrm{in}}} \approx 1 + \frac{C_1}{C_2}. \tag{1}$$

This forms a current amplifier and, with the resistor R_2 connected to the drain of the output transistor M_2, the transimpedance gain for low frequencies becomes

$$R_{\mathrm{T}} = \left(1 + \frac{C_1}{C_2}\right) R_2. \tag{2}$$

Here the capacitive term augments the gain of the resistor and allows for a larger combined on-chip gain. Important is that the capacitive gain does not contribute noise, while the noise current of the R_2 is divided by the current gain factor as we will see later. A more detailed analysis also confirms that, at least in general, the bandwidth can be increased via the increase of the gain of the core voltage amplifier without reducing R_2 and, therefore, without a negative impact on the transimpedance gain [23].

The simplified expressions from above assume an infinite forward gain A with the overall gain determined by the feedback circuit only. In practice, this simplified expression suggests somehow higher gain when compared to the one obtainable in realistic circuit with CMOS voltage headroom constraints. Although the expression can be used for an approximate analysis of the design, it is not extremely helpful if one wants to predict accurately the performance of a real circuit and, therefore, models with improved predictive power are needed.

In order to develop a practical TIA circuit for OTDR application, one shall start with a careful analysis of the corresponding fixed-gain configuration. While preserving the general structure of the capacitive feedback, one still has some flexibility in selecting the structure of the core operational amplifier. Here we follow a classical approach of using a modification of the common-source (CS) amplifier as shown in Fig. 2, although promising alternative approaches have been also reported [24, 23]. The configuration resembles the original work of Razavi [22], which had been later elaborated in a series of works of Shahdoost [25, 26]. The circuit employs a single-stage CS as a core amplifier as one is opted for a simpler voltage amplifier due to stringent requirements for noise performance and, hence, less number of active components. Obviously, one shall ensure that sufficient gain is achieved with the provided CS configuration. Note that for low-noise applications the CS stage can be considered as a viable option when compared to alternative implementations [25].

The overall voltage gain transfer function G_Σ of the circuit can be derived from the combined forward gain $G_1G_2G_3$, the feedback gain component F_1 and the output feed-out gain G_{out}

$$G_\Sigma = \frac{V_{\mathrm{out1}}}{V_{\mathrm{in}}} = \frac{G_1G_2G_3}{1 + G_1G_2G_3F_1} G_{\mathrm{out}}\,, \tag{3}$$

where using the complex variable $s = j\omega$ one defines the gain for the input CS stage with M_1 and R_1 as

$$G_1 = \frac{V_{\mathrm{d4}}}{V_{\mathrm{in}}} = g_{\mathrm{m1}} R_1 \,. \tag{4}$$

The expression above ignores the impact of the cascode transistor M_4. The second gain component considers the influence of the biasing resistor of the second stage $R_{\mathrm{bias,2}}$ and capacitive isolation C_{C} and results in

$$G_2 = \frac{V_{\mathrm{g2}}}{V_{\mathrm{d4}}} = \frac{sR_{\mathrm{bias,2}}C_{\mathrm{C}}}{1 + sR_{\mathrm{bias,2}}C_{\mathrm{C}}} \,, \tag{5}$$

with the resistive biasing circuits shown in the right of Fig. 2. The term controls the high-pass behavior, where an introduction of the capacitor in the connecting path between M_1 and M_2 shall also help for reducing the voltage headroom constraints on R_1 and hence the value of R_1 can be also increased to minimize the thermal noise component. The capacitor may also result in lowering the bandwidth and degrading the stability by introducing another dominant pole and it becomes important to consider this capacitor in the detailed model of the amplifier. The last gain component is caused by the source-follower M_2 and can be written

$$\begin{aligned} G_3 = \frac{V_{\mathrm{s2}}}{V_{\mathrm{g2}}} = \frac{g_{\mathrm{m,2}} r_{\mathrm{DS5}}}{1 + g_{\mathrm{m,2}} r_{\mathrm{DS5}}} \frac{1}{1 + s\dfrac{r_{\mathrm{DS5}} C_1}{1 + g_{\mathrm{m,2}} r_{\mathrm{DS5}}}} \approx \\ \approx \frac{1}{1 + s\frac{C_1}{g_{\mathrm{m,2}}}} \,, \end{aligned} \tag{6}$$

and simplifications possible due to $g_{\mathrm{m,2}} r_{\mathrm{DS5}} \gg 1$. The capacitive feedback is implemented from the source follower to isolate R_1 from the leading effect of both the feedback circuit and the input capacitance of the subsequent stage. Thus, the parameters of the capacitive feedback circuit can be adjusted without an explicit impact on headroom constraints. Note that this design idea is often used in shunt-feedback TIA as discussed in [27].

The feedback component becomes approximately

$$F_1 = \frac{V_{\mathrm{in}}}{V_{\mathrm{s2}}} = \frac{sR_{\mathrm{bias,1}}C_2}{1 + sR_{\mathrm{bias,1}}(C_{\mathrm{T}} + C_2)}, \tag{7}$$

and includes the influence of the total input parasitic capacitance $C_{\mathrm{T}} = C_{\mathrm{D}} + C_{\mathrm{IN}}$ with an additional path neglected due to $C_2 \ll C_1$. Finally, the last factor becomes

$$G_{\mathrm{out}} = \frac{V_{\mathrm{out1}}}{V_{\mathrm{s2}}} = R_2 \frac{1 + sr_{\mathrm{DS5}}C_1}{r_{\mathrm{DS5}}}, \tag{8}$$

with a zero formed by C_1 and r_{DS5}. The pole due to the load capacitance would appear also outside the loop and as long as R_2 is less than the drain-source resistance of M_1, the stability of this TIA is not determined by the value of R_2. According to [21], this property allows for a different set of trade-offs between gain, noise and bandwidth when compared to the classical resistive feedback TIA. The work [21] also suggests the R_2 to be implemented as an active PMOS load in order to maximize the gain of the TIA. The very same work implements the DC bias at the input of the amplifier with a stack of diode-connected PMOS transistors through long channel devices operating in the sub-threshold region.

For the transimpedance gain R_{T} the current-voltage transformation at input impedance shall be considered.

For $C_{\mathrm{T}} \gg C_2$ this results in

$$\begin{aligned} R_{\mathrm{T}} = \frac{V_{\mathrm{out1}}}{V_{\mathrm{in}}} \frac{V_{\mathrm{in}}}{I_{\mathrm{in}}} = G_\Sigma \frac{X_{C_{\mathrm{T}}} R_{\mathrm{bias,1}}}{X_{C_{\mathrm{T}}} + R_{\mathrm{bias,1}}} = \\ = G_\Sigma \frac{R_{\mathrm{bias,1}}}{1 + sR_{\mathrm{bias,1}}C_{\mathrm{T}}}. \end{aligned} \tag{9}$$

Assuming small C_2, high forward gain g_{m1}, large bias resistances and r_{DS5}, an approximate expression for the transimpedance gain becomes

$$R_{\mathrm{T}} \approx R_2 \frac{C_1}{C_2} \,, \tag{10}$$

and this is close to the original approximate gain as derived by [22] with $C_1 \gg C_2$. However, the major improvement is in the detailed model, where differently from the original works Razavi [22] and Shahdoost [26], the gain includes the impact of both biasing resistors $R_{\mathrm{bias,1}}$ and $R_{\mathrm{bias,2}}$ along with that of the C_{C}. The newly derived expressions provide the foundation for a more accurate design methodology including some of the important issues ignored by previous works. The expressions above hold only when the operation point of the input stage transistor M_1 is established. The operation point can be controlled by the current source in parallel with R_1. Note that if we are targeting programmable-gain conguration, the current source formed by M_3 shall consistently fit and be aligned for all the required configurations.

The presented design is believed to have several major advantages over other well-established TIA designs [22]. First of all, the gain is still mainly defined by C_1 and C_2 and, therefore, shall contribute far less noise when compared to resistive feedback. Furthermore, the total noise current contributed by the rest of the stage shall be significantly lower compared to that of shunt-feedback TIA for the given bandwidth. Finally, the capacitance as seen at the input node shall not degrade the stability of the design and shall only lower the DC loop gain. The presented design differs from the reference implementation shown in [22] in the way that the core amplifier is not followed by another gain stage. Note that as the output driver is a large device, a 15 nH on-chip inductor was also added to the second stage in [22] to extend the bandwidth, while here we reach the bandwidth requirements without any inductive enhancement.

The classical CS structure of the voltage amplifier can be improved using the cascode implementation with an additional NMOS (M_4) stacked on the top of M_1. Because of its high output resistance, the voltage gain of

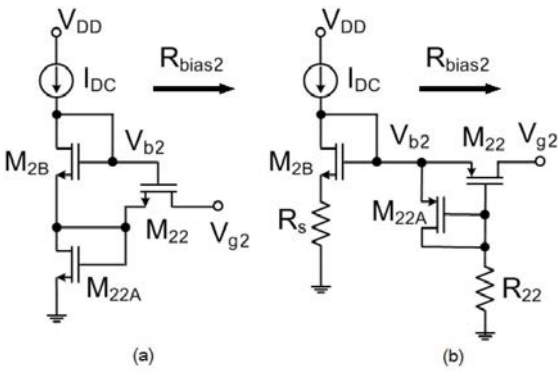

Fig. 3. Implementation of the biasing circuit: (a) - original NMOS-basedinal, and (b) –modified PMOS-based implementation. Corresponding parasitic capacitances which make the circuit to perform as a low-pass filter are not shown

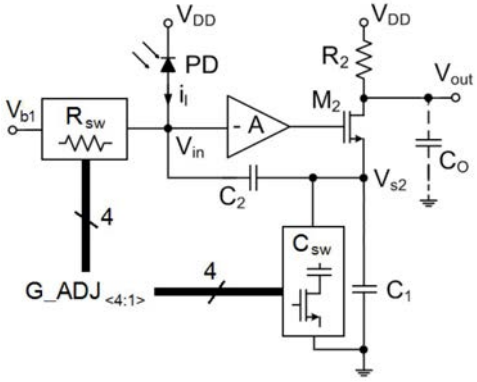

Fig. 4. Concept for a programmable-gain capacitive feedback TIA. For simplicity neither of the input capacitances C_{IN}, C_{D} (or equivalently total capacitance C_{T}) nor input resistance R_{IN} are shown

the cascode structure is higher than that of the regular one [1]. A naive approach to increase the value of R_1 is likely to fail due to issues related to the voltage headroom problems for our 1.8 V power supply. A remedy can be found by implementing a so-called gain boosting, where an alternative path to the drain current is provided with a PMOS transistor M_3 added to operate in parallel with R_1 and to handle the current fed to M_1. One may increase the value of R_1 while keeping the current density in M_1 suficiently high. The proposed circuit is configured with 80% of the current fed via M_3 and the rest passing through original R_1. The approach not only reduces the noise contribution of the load, but also a relatively high gain of this simple core amplifier may be reached.

A special handling of the DC dark current is also necessary for the TIA of the given topology. If not addressed properly, it may lead to saturation issues and instability as explained in [22] and [26]. Here we follow the general strategy suggested in previous works of Razavi and Shahdoost with a pair of transistors placed at the gate of M_1. In order to match the output of the TIA to $50\,\Omega$ loads, as a requirement for most of the voltage-output amplifiers, a dedicated buffer stage is added to the output with the transistor M_{buffer} biased to have a transconductance $g_{\mathrm{buffer}}^{-1} = 50\,\Omega$.

A special challenge in terms of an area-efficient design comes due to the requirement to have a low cut-off frequency of 100 kHz. An implementation as shown above requires to place large $R_{\mathrm{bias},1}$ and $R_{\mathrm{bias},2}$ at the corresponding gates of M_1 and M_2 while minimizing the parasitic capacitance. Even though a straightforward implementation with bias resistor can be applied for M_1 as, *eg* for the configuration with a gain of $R_{\mathrm{T}} = 10\,\mathrm{k}\Omega$ the $R_{\mathrm{bias},1}$ is only $16\,\mathrm{k}\Omega$ and has a negligible impact on the total area of the circuit, the method can be hardly used when applied to V_{g2} as the value of the resistance becomes in MΩ range even for a default TIA configuration with $R_{\mathrm{T}} = 10\,\mathrm{k}\Omega$ and, therefore, may prohibit a practical area-effcient design.

An attempt to address this problem had been already demonstrated before, (*eg* see the works of Shahdoost [26, 28]) and is shown in Fig. 3(a), where a biasing circuit formed by three NMOS transistors was suggested for design running from 2.2 V supply (parasitic capacitances, which make the circuit to perform as a low-pass filter, are not shown). This three-transistor topology plays the role of a very large resistor while occupying considerably less silicon area compared to using a regular resistance on the chip with the same resistance value [26, 29]. In such bias network the biased transistor (*eg* M_1 or M_2 in our design) and $M_{22\mathrm{A}}$ constitute a current mirror, while I_{DC} and $M_{2\mathrm{B}}$ define the on-resistance of M_{22}, which provides large resistance for isolation of the signal path from the low impedance introduced by $M_{22\mathrm{A}}$ [29]. Unfortunately, the proposed approach, while running from 2.2 V supply, is hardly applicable in the present design with 1.8 V supply due to voltage headroom problem.

In order to mitigate the problem of an area-efficient design with $R_{\mathrm{bias},2}$, we suggest an alternative approach for V_{g2} using two PMOS devices M_{22} and $M_{22\mathrm{A}}$ as shown in Fig. 3(b). The proposed approach addresses the NMOS problem with the voltage headroom as while $V_{\mathrm{DD}} - V_{\mathrm{g2}}$ is not sufficient for proper operation of NMOS devices, the voltage difference $V_{\mathrm{g2}} - V_{\mathrm{GND}}$ provides enough voltage for PMOS-based implementation.

The concept for the programmable-gain configuration capacitive feedback TIA is shown in Fig. 4 and employs a simultaneous adjustment of M_1 biasing network and one of the feedback capacitors C_1. The modifications necessary for programmable-gain functionality are elaborated for $R_{bias,1}$ and C_1 in Fig. 5. The proposed approach also allows an independent tuning for low- and high-frequency ranges and significantly simplifies the design process when compared to one parameter approach such as when using R_2 only. A parallel connection of the capacitance increments as required for each gain configuration forms the overall capacitance C_1. However, practically only the upper part of the amplifier pass-band is addressed with the adjustment of C_1 via its coupling to the gain of the second stage. Here the tuning of $R_{\mathrm{bias},1}$ implements the missing additional control knob for the lower part of the pass-band and allows an independent adjustment of the gain

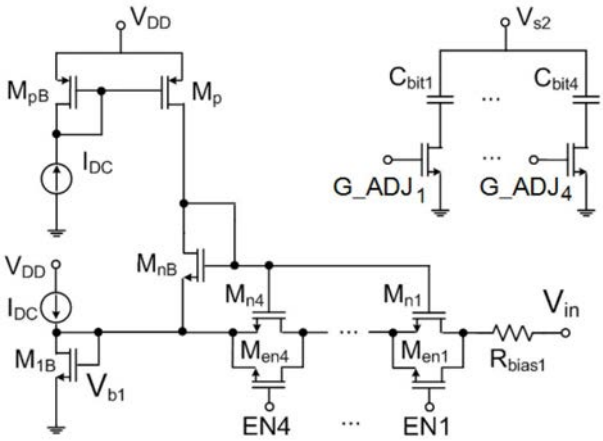

Fig. 5. Implementation of $R_{\text{bias},1}$ and C_1 switches for programmable-gain capacitive feedback TIA

to that implemented with C_1. From the general gain expression as elaborated before one recalls that the overall gain depends on both C_2 and C_1. In order to avoid redundant adjustments we suggest C_2 to be kept constant and it shall be selected very small.

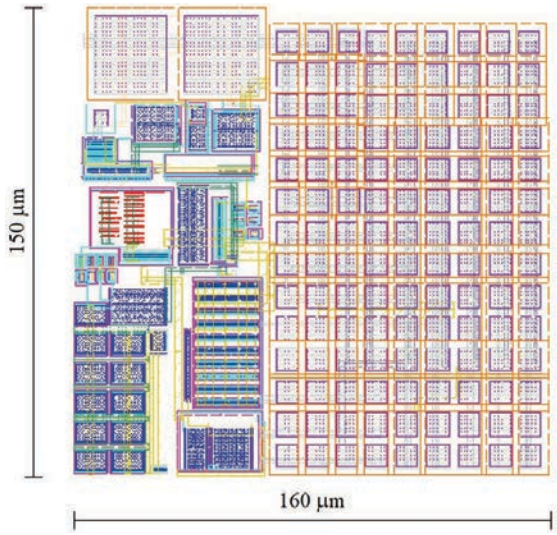

Fig. 6. Layout of the implemented programmable-gain TIA using TSMC 0.18 pm CMOS process

The input-referred noise current $i_{n,\text{TIA}}$ is an important parameter when characterizing the TIA design as it determines the overall sensitivity of the circuit. It can be shown [27, 24] that the noise for the topology has the following general form

$$\overline{i_{n,\text{TIA}}^2} \approx \frac{4k_\text{B}T}{R_2\left(1+\dfrac{C_1}{C_2}\right)^2} + s^2\left(C_\text{T}+C_2\right)^2\overline{v_{n,\text{OpAmp}}^2}, \quad (11)$$

where T is the absolute temperature and k_B is the Boltzmann constant and $v_{n,\text{OpAmp}}$ is the input-referred voltage noise of the core operational amplifier. Clearly, the input-referred current noise due to the load R_2 is reduced with the approximate circuit gain. Comparing to the classical resistive feedback TIA, the topology alleviates the trade-off between noise and gain. Note also that the noise of the amplifier is still affected by the parasitic capacitance of the photodiode via its coupling with the voltage noise of the operational amplifier [23].

Since the channel length modulation has been neglected for the expression above, there will be partial drain current noise contribution from M_1 as well in a real circuit. Also, non-ideal biasing will result in an additional noise component (drain current noise because of biasing transistor). Before we have demonstrated that the proposed configuration augments the gain of the resistor by an additional current gain factor thereby allowing for larger on-chip gain. The expression from above also shows that the noise from R_2 is attenuated by the very same factor when referred to the input, unlike the resistive feedback where the noise due to R_F is referred directly.

3 Results

The proposed amplifier was designed and optimized using TSMC 0.18 μm CMOS process. Figure 6 shows the layout of the programmable-gain version with five gain configurations (10, 25, 100, 200 and 500 kΩ). While the original 10 kΩ configuration with a pure resistive biasing for both M_1 and M_2 occupied 150 μm $\times$ 200 μm (excluding contact pads) due to MΩ resistance in the second bias circuit, the transistor-based solution for M_2 biasing circuit reduces the 10 kΩ TIA configuration size down to 130 $\mu m \times 70$ μm (excluding contact pads) with the area reduction of around 70%. The proposed configuration with programmable-gain occupies 150 $\mu m \times 160$ μm which with a factor 2.6 $\times$ increase in the area when compared to a fixed-gain solution with PMOS-based biasing for M_2 but is still less than a single-gain configuration with pure resistive biasing. Here the implementation of C_1 for larger gains consumes around 50% of the design area and is, therefore, mainly responsible for the area increase. The design area is comparable to a previously

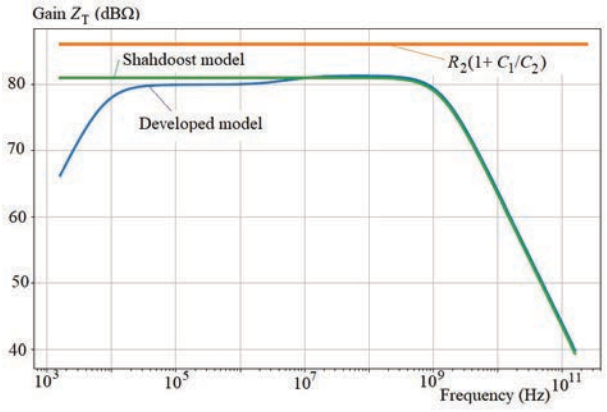

Fig. 7. Transimpedance gain of the developed and several alternative models

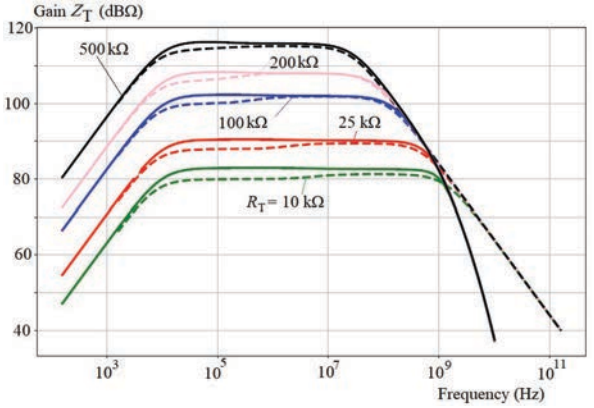

Fig. 8. Transimpedance of programmable-gain TIA configuration

reported [6] programmable-gain amplifier for OTDR applications based on resistive feedback in 0.35 μm CMOS. However, in the proposed design we have achieved significantly better performance (gain, bandwidth and noise) for all TIA configurations with almost no penalty in the die area.

Table 1 shows the values of the adjustable parameters C_1 and $R_{\text{bias},1}$ for selected gain-bandwidth configurations. Both the values for $R_{\text{bias},1}$ and C_1 scale up linearly with the required gain and this results in an extremely simple methodology for designing a programmable-gain capacitive feedback TIA in CMOS. As was explained before, the values of $R_{\text{bias},1}$ and C_1 shall be interpreted as cumulative ones for both the resistance and capacitance. The configurations with the largest gains ($R_{\text{T}} = 200\,\text{k}\Omega$ and $500\,\text{k}\Omega$) are the most demanding in terms of the consumed area with the cumulative capacitance reaching 120 pF for C_1. The adjustable $R_{\text{bias},1}$ is implemented as a resistor only for the configuration with the smallest gain $R_{\text{T}} = 10\,\text{k}\Omega$, while for the rest a transistor-based implementations with equivalent resistivity is adopted to save the chip area. The power dissipation of all configurations is nearly the same and is around 21 mW while running from 1.8V power supply. First, let us note that the proposed transfer function $Z_{\text{T}}(s)$ is different from the one suggested by Shahdoost where the author ended up with

Table 1. Parameters for programmable-gain TIA

R_{T} (kΩ)	C_1 (pF)	$R_{\text{bias},1}$ (kΩ)
10	2.4	16
25	6	40
100	24	160
200	48	320
500	120	800

$$\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{\dfrac{A\,(C_1+C_2)+C_2}{C_T+C_2+AC_2}}{1+\dfrac{s\,(C_1C_T+C_1C_2+C_2C_T)}{g_{\text{m},2}\,(C_T+C_2+AC_2)}}, \qquad (12)$$

which for the CS voltage amplifier results in

$$Z_{\text{T}}(s) = \frac{V_{\text{out}}}{I_{\text{in}}} = \frac{R_2\dfrac{g_{\text{m},1}R_1\,(C_1+C_2)+C_2}{C_T+C_2+g_{\text{m},1}R_1C_2}}{1+\dfrac{s\,(C_1C_T+C_1C_2+C_2C_T)}{g_{\text{m},2}\,(C_T+C_2+g_{\text{m},1}R_1C_2)}}. \qquad (13)$$

The latter expression can be approximated by classical (2) for low-frequency range. Note that the detailed model from above does not contain C_{C} nor includes the impact of the bias resistors $R_{\text{bias},1}$ and $R_{\text{bias},2}$. Figure 7 compares the simplified constant gain model against the model of Shahdoost [20] and the model suggested in this work.

Clearly, the approximation (2) strongly overestimates the gain even in low- and mid-frequency ranges for practically realizable circuits. Both our suggested model and the model from Shahdoost are equivalent for mid-and high-frequencies, whereas the low-frequency behavior is correctly covered only by the model presented in this work.

Importance of properly covering the low-frequency behavior can be seen in Fig. 8, where the simulation results are compared to the analytical model for all five gain-bandwidth configurations of the programmable-gain circuit. The circuit demonstrates a pass-band behavior which is not covered by the model of Shahdoost. What relates the simulation results and the analytical model derived in previous section, even though the low- and mid-frequency behavior is covered reasonably well, one can still see some discrepancy for high-frequency range. A comparison of Fig. 7 and Fig. 8 shows that this mismatch of common for both our and Shahdoost model as those demonstrate almost perfect match above 1 GHz.

Although the analytical expression for the transimpedance gain explicitly considers the value for C_{T}, this value is only partially under the control of the designer and, in practice, the total input capacitance can be slightly different from the one assumed for the reference design. The sensitivity of the transimpedance gain with respect to the value of C_{T} can be seen in Fig. 9, where the circuit was designed assuming a reference value C_{T}

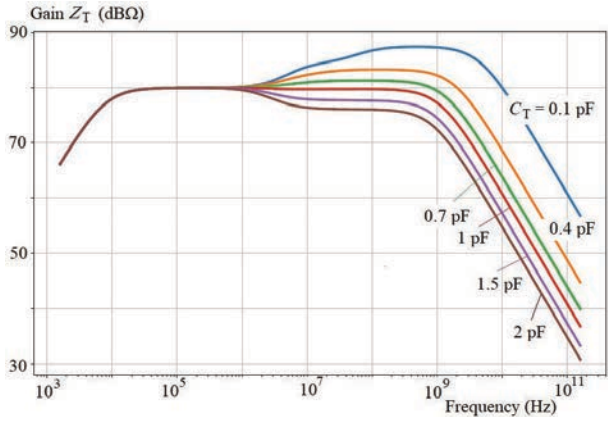

Fig. 9. Sensitivity of the gain with modeled transimpedance gain (proposed model) to the total input capacitance for configuration with $R_T = 10\,k\Omega$

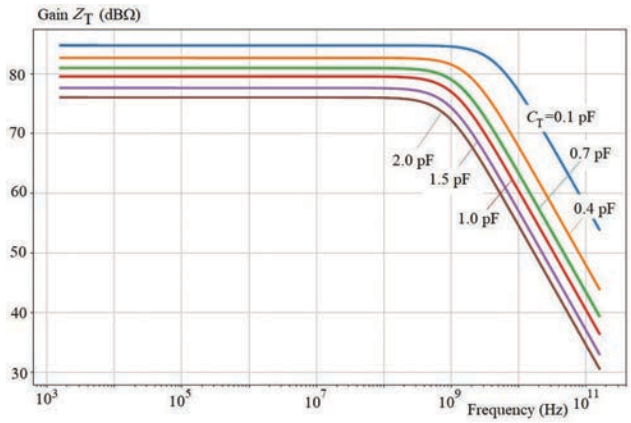

Fig. 10. Sensitivity of the transimpedance gain (Shahdoost model) to the total input capacitance for configuration with $R_T = 10\,k\Omega$

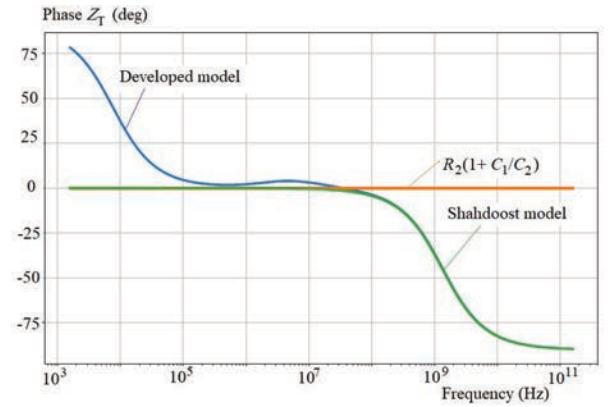

Fig. 11. Transimpedance phase of the developed and several alternative models

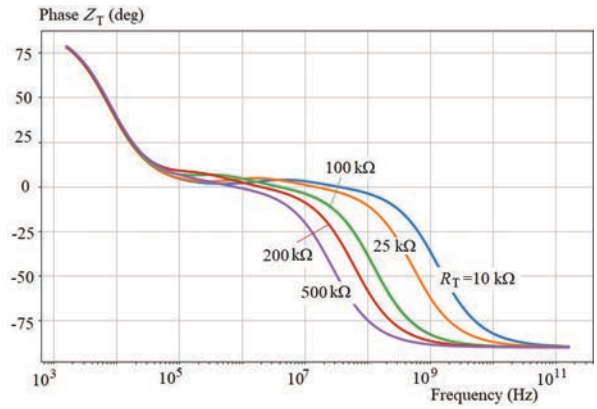

Fig. 12. Analytically calculated transimpedance phase for programmable-gain TIA configuration

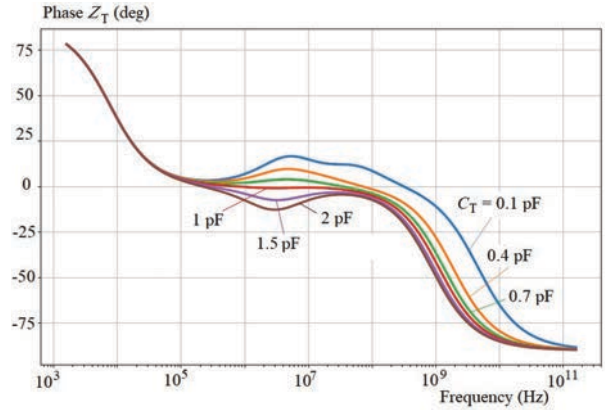

Fig. 13. Sensitivity of the developed model phase to the total input capacitance for configuration with $R_T = 10\,k\Omega$

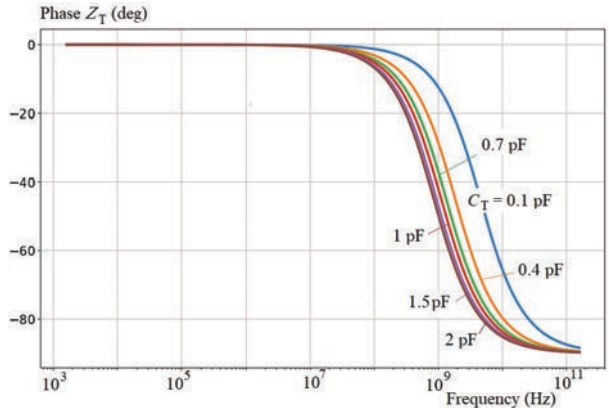

Fig. 14. Sensitivity of the Shahdoost model phase to the total input capacitance for configuration with $R_T = 10\,k\Omega$

of 0.7 pF. Note that the lower frequency range is not affected by C_T variation with a strong impact visible for mid- and high-frequency ranges. As expected, the actual value of C_T plays an important role in determining the bandwidth of the circuit with smaller C_T resulting in increased bandwidth. For comparison, the same sensitivity plot of the transimpedance gain is shown in Fig. 10 for the model of Shahdoost. The results are consistent with our observation from above that this model does not accurately describe the low-frequency behavior where variation in C_T also does not affect the gain. Still, both models consistently demonstrate a strong dependency of the bandwidth on the actual value of C_T. This is different from the results reported in [29], where the authors claimed the capacitive feedback TIA to perform better over conventional resistive feedback structure, of which

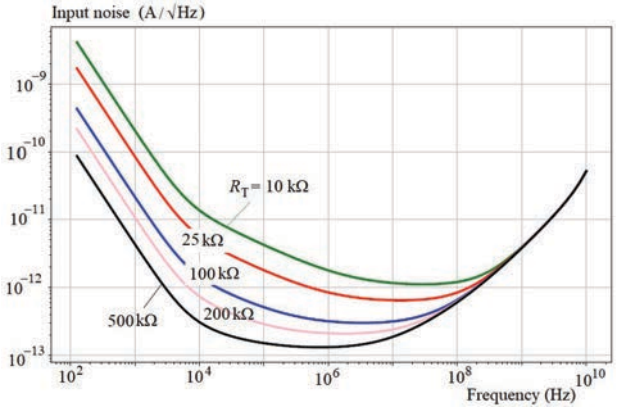

Fig. 15. Simulated input-referred noise performance for programmable-gain configuration

-3dB bandwidth shall decrease proportional to increase of the PD capacitance. Unfortunately, this feature of the capacitive feedback TIA cannot be directly deduced from our model, although the results reported in [29] may be still influenced by particular TIA parametrization and the dependency on C_T may be still better than that of classical resistive shunt-feedback TIA.

Figure 11 shows the phase performance of the developed model and the one proposed by Shahdoost. Similarly to the gain performance, both models differ in lower frequency range as the simpler model of Shahdoost ignores the pass-band behavior of a real amplifier. The results of the analytical model for a set of different gain-bandwidth configurations are shown in Fig. 12.

It may be also educative to see the sensitivity of the modeled phase performance with respect to the total input capacitance C_T. Figure 13 shows the phase performance of the developed model depending on the actual value of C_T , where the circuit was designed assuming the value of C_T equal to 0.7 pF. Similarly, Fig. 14 shows the sensitivity of Shahdoost's model for the very same set of mismatched C_T values. Similarly to the case of the gain, both models significantly differ in low-frequency range, where a simplified model ignores the bandpass behavior of a real circuit.

The simulated noise performance for programmable-gain configuration is shown in Fig. 15. The 10 kΩ design reaches the noise level below 1.8 pA/$\sqrt{Hz}$ and provides sufficient noise margin with respect to the OTDR requirement of being below 5 pA/$\sqrt{Hz}$ for 10 kΩ gain configuration. As expected, TIA configurations with higher gain result in smaller noise at the price of reduced bandwidth as we did not target constand bandwidth design.

The results of simulation confirmed that the proposed inductor-less design is able to achieve the required gain and bandwidth without any additional stage of post-amplifier. A closed-form expression for -3dB bandwidth can be approximated as [21]

$$BW_{-3dB} \approx \frac{1}{\sqrt{2}} \frac{g_{\mathrm{m},2} C_2 g_{\mathrm{m},1} R_1}{\pi C_1 \left(C_2 + C_T\right)} \,. \tag{14}$$

The results for the bandwidth calculation are shown in Tab. 2 with the Tab. 3 demonstrating the dependency of the bandwidth on the total parasitic input capacitance.

The performance of the developed amplifier can be compared to the performance of some selected works using the data in Tab. 4. Note that not all works provide exact values of the input capacitance (*eg* see [20, 28]) and, therefore, a single performance measure in terms of figure-of-merit can be hardly computed. However, the proposed design in terms of the combined gain, bandwidth, power dissipation and the noise is better than most of the reported works. The only known to us attempt to implement some variable gain using capacitive feedback TIA was reported in [29] with the most important parameters of the reported circuit such as achievable baseline gain, bandwidth and noise being inferior to those of the approach proposed in this work. The applicability of the simplistic model developed in [29] for larger range of circuit parameters is unclear as it ignores not only the value of C_1, but also the impact of the biasing circuits as explained above. Finally, our approach implements a double control strategy with an independent adjustment of the low- and high-frequency performance, where in [29] only a single tuning parameter R_2 is becomes available for the designer.

Table 2. Results of analytical bandwidth calculations for programmable-gain TIA

R_T (kΩ)	Open-loop bandwidth ≈ (MHz)	Closed-loop bandwidth ≈ (MHz)
10	1524	1078
25	591	418
100	141	100
200	69	49
500	30	21

Table 3. Analytical bandwidth dependency on C_T for 10 kΩ gain configuration

C_T (pF)	Open-loop bandwidth ≈ (MHz)	Closed-loop bandwidth ≈ (MHz)
0.1	8059	5698
0.4	2564	1813
0.7	1524	1078
1.0	1084	767
1.5	732	518
2.0	553	391

Table 4. Performance of some reported TIA

Work/Year	CMOS (μm)	C_T (pF)	R_T (dB · Ω)	BW_{-3dB} (GHz)	Power/V_{DD} (mW / V)	Avg. noise (pA/$\sqrt{Hz}$)
Razavi, 2000 [22]	0.60		78.8	0.55	30 / 3.0	4.5
Oh, 2004 [30]	0.35	0.6	68	1.73	50.0 / 3.3	3.3
Wu, 2005 [31]	0.18	0.25	61	7.2	70.2 / 1.8	8.2
Jin, 2006 [15]	0.18	0.05	51	30.5	60.1 / 1.8	55.7
Wang, 2007 [32]	0.18	0.15	59	8.6	18.0 / 1.8	25
Momeni, 2010 [33]	0.13	0.25	62	6.0	98 / 2.0	20
Liu, 2012 [11]	0.50		57.6	1.04	73.4 / 3.3	18.33
Yu, 2012 [34]	0.13	0.25	82.3	1.8	118 / 0.8	0.8
Atef, 2014 [35]	0.13	2.0	76.8	1.6	47.3 / 1.8	26.5
Shahdoost, 2014 [20]	0.18		75.5	1.62	26.3 / 2.2	3.18
AbdElrahman, 2015 [36]	0.13	2.0	61.6	2.0	3.0 / 1.5	>12.4
Liu, 2015 [37]	0.18		87.8	1.4	8.1 / 1.8	2.75
Shahdoost, 2016 [28]	0.13		76	1.76	13.7 / 1.5	2.67
AbdElrahman, 2016 [1]	0.13	0.2	56.65	7.0	1.95 / 1.5	7.5
Zohoori, 2018 [38]	0.09	0.2	53.5	3.5	1.28 / 1.0	16.8
Hosseinisharif, 2020 [39]	0.09	0.25	40	6.4	1.6 / 1.2	25
This work	0.18	0.7	83/80	1.0	21.0 / 1.8	2.0

4 Conclusions

The paper demonstrates a low-noise capacitive feedback TIA and applies the developed design methodology for a programmable-gain amplifier configuration suitable for entry-level OTDR instruments. The presented approach possesses an advantage of an inductor-less design while addressing the challenges of classical TIA designs such as simultaneously high performance in terms of noise, bandwidth and gain. The work reports a more accurate design procedure which also accounts for the in influence of both biasing circuits and decoupling capacitance. The suggested approach for amplifier gain-bandwidth adjustment is based on varying C_1 capacitor in parallel with the biasing resistor of the input MOSFET. The scheme enables an independent tuning of the amplifier performance in both lower and higher frequency ranges and all required gain-bandwidth configurations for OTDR instruments can be easily obtained. The feasibility of the design was demonstrated using a standard commercially-available TSMC 0.18 μm 1.8 V CMOS process. The schematic simulation confirms the circuit to dissipate 21 mW for the basic configuration with 83/80 dBΩ transimpedance gain and bandwidth around 1.0 GHz. For this basic configuration the input-referred current noise density is kept below 2.0 pA/$\sqrt{Hz}$ and even smaller noise values are reached for higher gain configurations. The developed model and the supporting simulation were compared to previously developed models and advantages of a newly developed model were indicated. Additional analysis is provided for the sensitivity of the developed with respect to variation of the input parasitic capacitance.

References

[1] D. Abd-elrahman, M. Atef, and G. Wang, "10 Gb/s 1.95 mW active cascode transimpedance amplifier for high speed optical receivers, in", *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2016, pp. 1-4.

[2] J. Shi, N. Qi, Q. Yang, H. Guo, G. Yan, and J. Du, "A low-cost system-on-chip for optical time domain reflectometer (OTDR), in", *2016 IEEE MTT-S International Wireless Symposium (IWS)*, Shanghai, 2016, pp. 1-4.

[3] M. Atef and H. Zimmermann, "Low-power 10 Gb/s inductorless inverter based common-drain active feedback transimpedance amplifier in 40 nm CMOS,", *Analog Integr Circ Sig Process*, 2013.

[4] J. H. Yeom, K. Park, J. Choi, M. Song, and S. Y. Kim, "Low-cost and high-integration optical time domain reflectometer using CMOS technology, in", *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, July 2019, pp. 145-148.

[5] M. Tateda and T. Horiguchi, "Advances in optical time-domain reflectometry,", *Journal of Lightwave Tech- nology*, vol. 7, no. 8, pp. 1217-1224, 1989.

[6] J. Charlamov and R. Navickas, "Design of CMOS Differential Transimpedance Ampli- fier,", *Elektronika ir Elektrotechnika*, vol. 21, no. 1, pp. 38-41, 2015. [Online]. http://eejournal.ktu.lt/index.php/elt/article/view/4548.

[7] E. Sackinger, *Analysis and Design of Transimpedance Amplifiers for Optical Receivers*, Wiley, 2017.

[8] A. Romanova and V. Barzdenas, "A Review of Modern CMOS Transimpedance Amplifiers for OTDR Applications,", *Electronics*, vol. 8, no. 10, p. 1073, Sep 2019. [Online]. http://dx.doi.org/10.3390/electronics8101073.

[9] H. Escid, S. Salhi, and A. Slimane, "Bandwidth enhancement for 0.18 um CMOS transimpedance amplifier circuit, in", *2013 25th International Conference on Microelectronics (ICM)*, Dec 2013, pp. 1-4.

[10] M. Kossel, C. Menolfi, T. Morf, M. Schmatz, and T. Toifl, "Wideband CMOS transimpedance amplifier", *Electronics Letters*, vol. 39, no. 7, 2003.

[11] R. q. Liu, Z. p. Wang, J. Tian, and Z. Meng, "A 57dBOmega 1GHz CMOS Front-End Preamplifier for Optical Receivers, in", *2012 8th International Conference on Wireless Communications, Networking and Mobile Computing*, Sept 2012, pp. 1-4.

[12] L. Han, M. Yu, and L. Zong, "Bandwidth ehancement for transimpedance ampilfier in CMOS process",*2010 3rd International Conference on Biomedical Engineering and Informatics*, vol. 7, 2010, pp. 2839-2842.

[13] G. Royo, C. Sanchez-Azqueta, C. Aldea, S. Celma, and C. Gimeno, "CMOS transimpedance amplifier with controllable gain for RF overlay", *2016 12th Conference on Ph.D. Research in Microelectronics and Elec- tronics (PRIME)*, 2016, pp. 1-4.

[14] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors,", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 346-355, March 2000.

[15] J. D. Jin and S. S. H. Hsu, "40-Gb/s Transimpedance Amplifier in 0.18-um CMOS Technology, in", *2006 Proceedings of the 32nd European Solid-State Circuits Conference*, Sept 2006, pp. 520-523.

[16] R. Y. Chen, T-S. Hung, and C.-Y. Hung, "A CMOS variable-gain transimpedance amplifier for infrared wireless data communications", *2005 Digest of Technical Papers. International Conference on Consumer Electronics, 2005, ICCE.*, 2005, pp. 357-358.

[17] R. Ma, M. Liu, H. Zheng, and Z. Zhu, "A 77-db dynamic range low-power variable-gain transimpedance amplifier for linear ladar,", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 2, pp. 171-175, Feb 2018.

[18] P. Monsurro, A. Trifiletti, and T. Ytterdal, "A novel transimpedance amplifier with variable gain", *NORCHIP*, 2010, pp. 1-4.

[19] C. Kuznia, J. Ahadian, D. Pommer, R. Hagan, P. Bachta, M. Wong, K. Kusumoto, S. Skendzic, C. Tabbert, and M. W. Beranek, "Novel high-resolution OTDR technology for multi-Gbps transceivers", *OFC 2014*, March 2014, pp. 1-3.

[20] S. Shahdoost, A. Medi, B. Bozorgzadeh, and N. Saniei, "A novel design methodology for low-noise and high- gain transimpedance amplifiers, in", *2014 Argentine Conference on Micro-Nanoelectronics, Technology and Applications (EAMTA)*, July 2014, pp. 77-82.

[21] J. Salvia, P. Lajevardi, M. Hekmat, and B. Murmann, "A 56M? CMOS TIA for MEMS applications", *2009 IEEE Custom Integrated Circuits Conference*, Sep. 2009, pp. 199-202.

[22] B. Razavi, "A 622 Mb/s 4.5 pA/ (Hz) CMOS transimpedance amplifier [for optical receiver front-end]", *Hz2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056)*, in 2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056), Feb 2000, pp. 162-163.

[23] J. Hu, Y. Kim, and J. Ayers, "A low power 100MOmega CMOS front-end transimpedance amplifier for biosensing applications", *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, 2010, pp. 541-544.

[24] "A 65 nm CMOS ultra low power and low noise 131M front-end transimpedance amplifier", *23rd IEEE International SOC Conference*, 2010, pp. 281-284.

[25] S. Shahdoost, A. Medi, and N. Saniei, "A 1.93 pA/$\sqrt{\text{Hz}}$ transimpedance amplifier for 2.5 Gb/s optical communications", *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, May 2011, pp. 2889-2892.

[26] S. Shahdoost, B. Bozorgzadeh, A. Medi, and N. Saniei, "Low -noise transimpedance amplifier design procedure for optical communications", *22 nd Austrian Workshop on Microelectronics (Austrochip)*, Oct 2014, pp. 1-5.

[27] P. Keshri, "Comparative study of transimpedance amplifier design for MEMS resonators for GSM commu- nication systems", Leland Stanford Junior University, Tech. Rep., 2010.

[28] S. Shahdoost, A. Medi, and N. Saniei, "Design of low-noise transimpedance amplifiers with capacitive feed- back,", *Analog Integrated Circuits and Signal Processing*, vol. 86, no. 2, pp. 233-240, 2016.

[29] Y. Zhang, V. Joyner, R. Yun, and S. Sonkusale, "A 700Mbit/s CMOS capacitive feedback front-end amplifier with automatic gain control for broadband optical wireless links, in", *2008 IEEE International Symposium on Circuits and Systems*, May 2008, pp. 185-188.

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