Journal of Electrical Engineering, Vol. 74, No. 3, 2023, pp. 177-183

sciendo

PAPER

Mutually coupled CG-CS current reuse low noise amplifier architecture for 4 – 14 GHz frequency

Dheeraj Kalra[1,2], Vishal Goyal[2], Manish Kumar[2], Mayank Srivastava[1]

The current research paper presents a design of a mutually coupled cascode Common Gate Common Source (CG-CS) Low Noise Amplifier (LNA) using current reuse technique. The proposed design provides a significant improvement in the gain and noise performance of the LNA, while also reducing power consumption. Mutually coupled inductors help in reducing the size of the circuit while transformer connected at the output provide output impedance matching. Proposed LNA simulated for the 4–14 GHz RF frequency. Mathematical analysis of proposed LNA has been analyzed using the small signal model henceforth input impedance; gain and Noise Figure (NF) have been derived from it. The design and simulation results show that the proposed LNA design with current reuse technique achieved a maximum gain of 17.87 dB, minimum NF of 5.45 dB, and input reflection coefficient less than –10 dB for the 10 GHz bandwidth. These results indicate a significant improvement in the overall performance of the LNA compared to conventional designs as Figure of Merit (FoM) is 17.34.

Keywords: CMOS, current reuse, mutual coupling, LNA, NF, CG–CS stage

1. Introduction

LNA is a critical component in modern communication systems. It is used to amplify the weak incoming signal received by the antenna and to maintain the signal-to-noise ratio (SNR) of the system. For high frequency applications, such as millimeter-wave communication systems, the design of an LNA becomes more challenging due to the increased losses and NF of the components at higher frequencies. In recent years, there has been significant research focused on developing LNAs for high frequency applications. One approach is the use of advanced semiconductor technologies such as indium phosphide (InP) or gallium nitride (GaN) to achieve high performance at high frequencies. Another approach is the use of innovative circuit topologies, such as cascode and common gate, to achieve better noise and gain performance. Several research works have reported the design of LNAs for high frequency applications using InP technology. For instance, a 24 GHz InP HEMT LNA was designed and fabricated by [1]. The LNA exhibited a minimum NF of 2.2 dB, a maximum gain of 16.6 dB, and an input return loss of –14 dB. Similarly, [2] presented the design of a 60 GHz InP HEMT LNA with a NF of 2.7 dB and a gain of 14 dB. Other research works have proposed innovative circuit topologies for LNAs at high frequencies. For example, [3] proposed a cascode LNA with improved linearity and gain performance for millimeter-wave applications. The LNA designed using a 90 nm CMOS process and exhibited a NF of 3.3 dB, a gain of 16.5 dB, and a 1-dB compression point of –11 dBm at 60 GHz. [4] proposed a 60 GHz CMOS LNA using a common gate topology with an inductor-peaking technique. The LNA exhibited a NF of 5.2 dB, a gain of 10.7 dB, and an input return loss of –12 dB. Similarly, [5] presented a 24 GHz CMOS LNA with a CS topology that used a modified T-match network to improve the input matching. The LNA exhibited a NF of 3.8 dB, a gain of 19 dB, and an input return loss of –19 dB. Another approach for designing CMOS LNAs for high frequency applications is the use of advanced CMOS process technologies, such as silicon germanium (SiGe) or RF CMOS, to achieve better performance at high frequencies. For example, [6] presented a 60 GHz RF CMOS LNA that exhibited a NF of 3.1 dB, a gain of 10 dB, and an input return loss of –14 dB. Similarly, [7] designed a 77 GHz SiGe LNA with a NF of 3.6 dB, a gain of 16 dB, and an input return loss of –10 dB. In conclusion, the use of CMOS technology for designing LNAs for high frequency applications is a challenging task. Innovative circuit topologies and advanced CMOS process technologies have been proposed to achieve high performance at high frequencies. The performance of the LNA is highly dependent on the circuit topology, semiconductor technology, and fabrication process used. Section 2 describe the CG and CS amplifier stages with mutually coupling between the inductors and its design considerations. The impedance matching, gain analysis and NF analysis have been discussed with the mathematical derivations. Section 3 describes simulation results and analysis of performance metrics along with comparison to other LNA designs in the literature.

[1]Department of ECE, National Institute of Technology, Jamshedpur, India
[2]Department of ECE, GLA University, Mathura, India
dheeraj_kalra7@yahoo.co.in, vishal.goyal@gla.ac.in, manish.kumar@gla.ac.in, mayank.ece@nitjsr.ac.in

https://doi.org/10.2478/jee-2023-0023, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

2. Mutually coupled CG-CS LNA design

The circuit diagram is shown in Fig. 1.

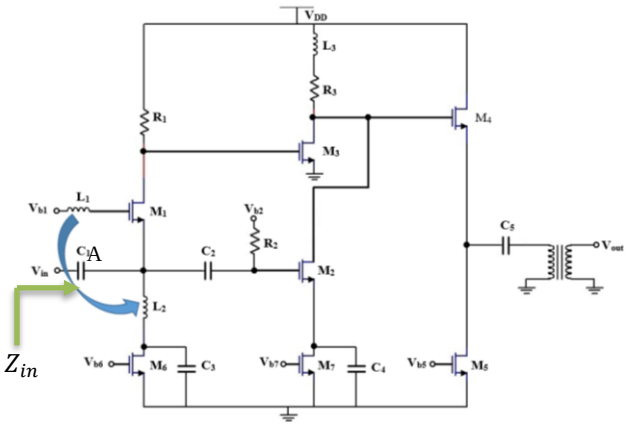

Fig. 1. Proposed Mutually Coupled CG-CS LNA

Table 1. Circuit Parameters for Proposed LNA

$\left(\frac{37.5\ \mu m}{45\ nm}\right)_{M1}$	$\left(\frac{42.5\ \mu m}{45\ nm}\right)_{M2}$	$\left(\frac{6.2\ \mu m}{45\ nm}\right)_{M3}$
$\left(\frac{10\mu m}{45\ nm}\right)_{M4}$	$\left(\frac{10\mu m}{45\ nm}\right)_{M5}$	$\left(\frac{23.7\ \mu m}{45\ nm}\right)_{M6}$
$\left(\frac{26.3\ \mu m}{45\ nm}\right)_{M7}$	$(1\ \text{nH})_{L1}$	$(3.5\ \text{nH})_{L2}$
$(20\ \text{nH})_{L3}$	$(1.1\ \text{k}\Omega)_{R1}$	$(100\ \Omega)_{R3}$
$(1.3\ \text{k}\Omega)_{R2}$	$(6\ \text{pF})_{C2}$	Coupling Coefficient $k = 0.835$
$C_1 = C_3 = C_4 = C_5 = 1\ \text{pF}$		

The analog circuit operating in subthreshold region consume very low power but required a trade-off with bandwidth and linearity. The biasing of proposed circuit provides high transition efficiency g_m/I_D as compared with strong inversion (SI). The proposed LNA consists of a two-stage common gate (CG) cascaded with a CS-CG stage. The first stage provides proper input impedance matching $R_S=1/g_m$ minimizing the reflection and increase the gain [14]. While second stage provide the high gain with noise cancellation at output terminal. Since inductor consume large chip area, Therefore, inductors L_1 and L_2 are mutually coupled to reduce the area and provide extra variable (coupling coefficient) to optimize the impedance matching. For output matching a buffer and transformer is added. Table 1 showing the parameters of components connected in the proposed circuit.

2.1 Input matching

Wideband input matching is gained by setting $g_m=1/R_S$, where $R_S=75\ \Omega$. Working in subthreshold region it become challenging to achieve this transconductance due to requirement of a large device, henceforth large input gate to source capacitance C_{gs} which reduced the bandwidth. However, to reduce the dependence of input impedance on C_{gs} an inductor L_1 which is mutually coupled with L_2 is used. The input impedance of proposed circuit is given by equation [13]

$$Z_{in} = Z_3 \left\| \frac{1}{g_{m1}(1-\alpha)} \right\| \frac{1}{sC_{gs1}(1-\alpha)}, \quad (1)$$

where Z_3 is the impedance without considering the effect of Inductor L_1 and α is the complex coefficient defined by equation

$$\alpha = \frac{sC_{gs1}\left(\frac{1}{Z_1}+sC_{gd1}\right)+sC_{gd1}g_{m1}}{\left(\frac{1}{Z_1}+sC_{gd1}\right)\cdot\left(\frac{1}{Z_2}+sC_{gs1}+sC_{gd1}\right)+sC_{gd1}(g_{m1}-sC_{gd1})}. \quad (2)$$

Z_1, Z_2 and Z_3 are given by equation (3) (4) and (5) respectively.

$$Z_1 = R_1 \left\| [s(C_{db1} + C_{g3})]^{-1} \right. \quad (3)$$

$$Z_2 = (s(L_1 + M) + R_{L1}) \left\| \left(\frac{1}{sC_{gb1}}\right) \right. \quad (4)$$

$$Z_3 = (s(L_2 + M) + R_{L1}) \left\| \left(\frac{1}{sC_{gs2}}\right) \right. \quad (5)$$

The proposed LNA is designed to achieve the objective of $S_{11} < -10\ dB$.

2.2 Gain analysis

Figure 2 displays the small signal model of the proposed mutually coupled LNA. Let A_1 be the gain of MOS M_1, A_2 is the gain of MOS M_2 i.e. from its input to the output and A_3 is the gain provided by the MOS M_3. Hence, the overall gain will be given by $A_V = A_1 \cdot A_3 + A_2$. As shown in Fig. 3, the signal at the input of CG stage is further amplified with the CS stage1 while signal travels through second path, i.e., CS stage 2. It can be observed that the signals at the output of stage 1 and 2 are having the same phase and henceforth the overall gain of the circuit is high. The derived values of A_1, A_2 and A_3 are given in equation (6), (7) and (8).

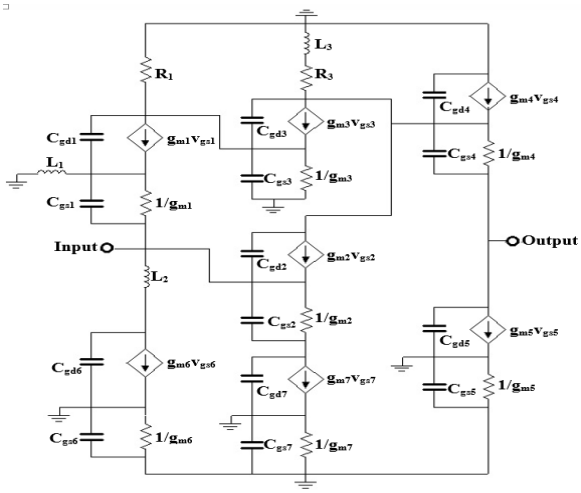

Fig. 2. Small signal model of the proposed mutually coupled LNA

$$A_1 = g_{m1}(1-\alpha)R_1 \left\| \left[s\left(C_{db1}+C_{g3}\right)\right]^{-1} \right. \quad (6)$$

$$A_2 = \left(\frac{g_{m2}+sC_{gd2}}{{}^{1}/_{(R_3+sL_3)}+sC_{ds2}+sC_{gd2}+{}^{1}/_{r_{02}}}\right) \quad (7)$$

$$A_3 = \frac{g_{m3}\left((R_3+sL_3)\left\|{}^{1}/_{sC_{db3}}\right.\right)}{1+{}^{g_{m3}}/_{sC_{sb3}}} \quad (8)$$

$$A_V = A_1 \cdot A_3 + A_2 \quad (9)$$

2.3 Noise calculation

Thermal noise in MOS devices is caused by the random movement of charge carriers. This movement of charge carriers can create fluctuations in the electrical signal, which can affect the performance of MOS devices. The amount of thermal noise in MOS devices is determined by several factors, including the temperature of the device, the size of the device, and the type of material used in the device. Generally, as the temperature of the device increases, the amount of thermal noise also increases. One way to reduce thermal noise in MOS devices is to reduce the size of the device, as this can reduce the number of charge carriers that are present in the device. Additionally, using materials with a lower level of noise can also help to reduce the amount of thermal noise in MOS devices. Thermal noise is an important consideration in the design and operation of MOS devices, as it can affect the performance and reliability of these devices. Engineers and designers must take into account the effects of thermal noise when designing and optimizing MOS devices for various applications.

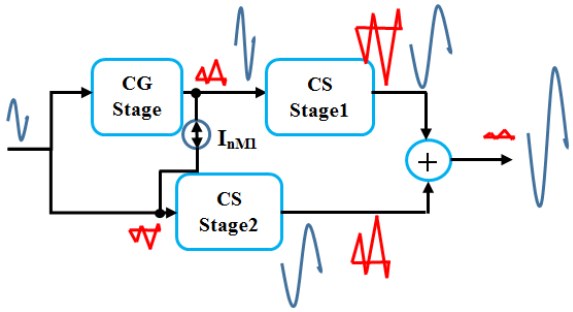

Fig. 3. Noise analysis of the proposed mutually coupled LNA

Figure 3 shows the propagation of noise through the various stages of LNA. The thermal noise present at the drain and source of MOS M_1 (CG Stage) are opposite in phase as depicted in Fig. 3. Further the noise gets amplified by CS stage 1 as well as another path CS stage 2. It can be noticed that the two noises are having the opposite phase at the output so therefore the resulting noise is less henceforth the NF get improved. The total noise is the noise contributed by the various components connected in the circuit. The noise current due to M_1, M_2, M_3, R_1 and R_2 are given in equations (10) – (14).

$$\overline{I_{nout,M1}^2} = 4kT\frac{\gamma}{\alpha}g_{m1}\left(\frac{Z_1A_3}{Z_4}\right)^2, \quad (10)$$

where

$$Z_1 = R_1 \left\| \left[s\left(C_{db1}+C_{g3}\right)\right]^{-1}, \right.$$

$$Z_4 = (R_3+sL_3)\|[sC_{db3}]^{-1}$$

Here, α is the ratio of MOS transconductance and drain conductance at zero bias, and γ is thermal noise parameter having a value of 2/3 for long channel devices and greater than 1 for short channel devices.

$$\overline{I_{nout,M2}^2} = 4kT\frac{\gamma}{\alpha}\frac{1}{g_{m2}}(G_{m2})^2 \quad (11)$$

$$\overline{I_{nout,M3}^2} = 4kT\frac{\gamma}{\alpha}\frac{1}{g_{m3}}(G_{m3})^2 \quad (12)$$

$$\overline{I_{nout,R1}^2} = \frac{4kT}{R_1}(Z_1G_{m3})^2 \quad (13)$$

$$\overline{I_{nout,R3}^2} = \frac{4kT(R_3+R_{L3})}{(sL_3+R_3+R_{L3})} \quad (14)$$

Here, $G_{m2}$is transconductance gain from M_2 gate to output and G_{m3} is transconductance gain from M_3 gate to output. The overall noise factor is given in equation (15).

$$F=1+\frac{\overline{I_{nout,M1}^2}+\overline{I_{nout,M2}^2}+\overline{I_{nout,M3}^2}+\overline{I_{nout,R1}^2}+\overline{I_{nout,R3}^2}}{\overline{I_{nout,Rs}^2}} \quad (15)$$

2.4 IIP3 analysis

The input third-order intercept point (IIP3) is a measure of the linearity and distortion characteristics of the amplifier. It represents the input power level at which the third-order intermodulation distortion (IMD) products reach the same level as the input signal. In other words, when the input power is increased to a level corresponding to the IIP3, the third-order distortion products will be as strong as the original signal [16]. At this point, the amplifier is said to be in compression, and the distortion products can interfere with nearby signals, causing intermodulation interference. In practical terms, a higher IIP3 indicates a more linear and distortion-free amplifier. In low noise amplifiers, a high IIP3 is desirable because it ensures that the amplifier can handle high input signal levels without introducing distortion or degrading the signal-to-noise ratio. To improve the IIP3 of an LNA, design techniques such as adjusting the bias current and impedance matching can be employed. However, it is important to note that increasing the IIP3 typically comes at the cost of increased power consumption and reduced gain, so a trade-off must be made between linearity and other performance metrics. To measure IIP3 in MOS amplifiers, a two-tone test is typically used. Two signals with frequencies f_1 and f_2 are applied to the amplifier and the third-order distortion products at frequencies $2f_1 - f_2$ and $2f_2 - f_1$ are measured. The IIP3 result for the proposed mutually coupled LNA is given in the results and discussion section.

3. Results and discussion

3.1 S-parameters

In LNA design, the S-parameters are used to optimize the performance of the amplifier, by adjusting the input and output matching networks, biasing conditions, and other design parameters. In this case, the S_{11} parameter has a bandwidth of 10 GHz and is less than –10 dB throughout the band as shown in Fig. 4. Having an S_{11} less than –10 dB throughout the entire bandwidth means that the LNA has good input matching and low reflection losses, which are important factors for achieving high performance and low NF.

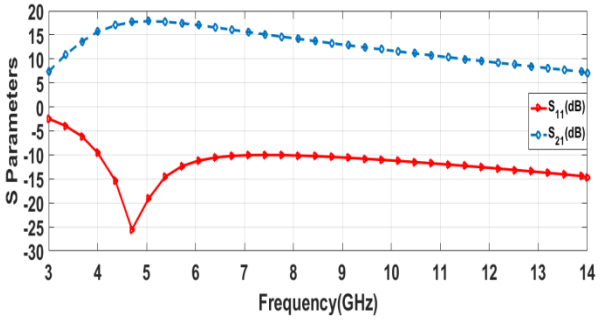

Fig. 4. S-parameters for proposed mutually coupled LNA

A well-matched LNA ensures that the maximum power is transferred from the input signal to the amplifier, resulting in optimal signal-to-noise ratio and minimal distortion. This makes the LNA suitable for use in a wide range of microwave applications where good matching and low noise are critical, such as in wireless communications, radar systems, and test and measurement equipment. S_{21} parameter has a bandwidth of 10 GHz and the simulation result as shown in Fig. 4 indicate that the highest value of S_{21} throughout the band is 17.87 dB. A high value of S_{21} also indicates that the LNA has good performance in terms of linearity, stability, and NF. Overall, a simulation result showing an S_{21} is a positive indicator of the performance of the LNA. The transformer at the output provides the good output matching in term of S_{22}. Simulation result for S_{22} is shown in Fig. 5.

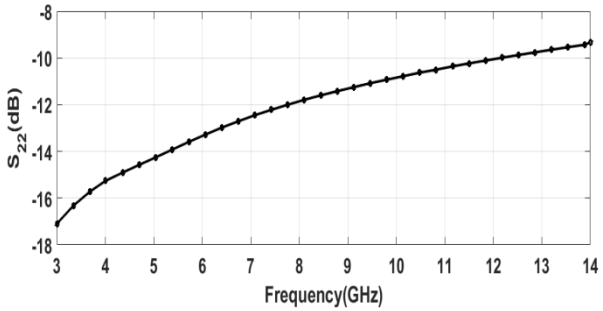

Fig. 5. S_{22} parameter for proposed mutually coupled LNA

3.2 Noise figure

The simulation result for the NF of the LNA depicts a minimum value of 5.45 dB as shown in Fig. 6. A NF of 5.45 dB means that the output noise power of the amplifier is only 1.43 times higher than the input noise power. A low NF helps to improve the sensitivity and range of the system, allowing signals to be transmitted and received over longer distances with greater accuracy.

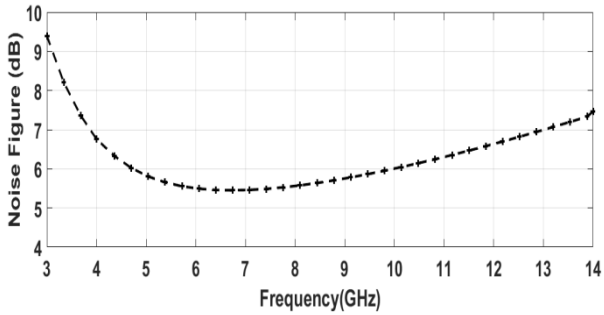

Fig. 6. Noise figure for proposed mutually coupled LNA

3.3 Process corner simulation

Process corner simulation is a type of simulation performed in the design and testing of integrated circuits (ICs) to ensure their functionality and reliability under different operating conditions. A process corner refers to a specific combination of process, voltage, and temperature (PVT) that can affect the performance of an IC. During the manufacturing process of an IC, there can be variations in the physical and electrical properties of the semiconductor material, as well as in the various processing steps involved. These variations can result in differences in the performance and behavior of the IC under different operating conditions. For example, variations in the supply voltage or temperature can affect the speed, power consumption, and reliability of the IC. The different types of process corners used in simulation can include typical, slow, fast, and worst-case scenarios, which represent different combinations of PVT parameters. For example, the slow corner represents the worst-case scenario for speed, with the lowest supply voltage and highest temperature, while the fast corner represents the best-case scenario for speed, with the highest supply voltage and lowest temperature. By performing process corner simulations, designers can identify any potential performance or reliability issues in the IC and make design modifications as needed to ensure that the IC meets its design specifications under a wide range of operating conditions. This helps to ensure that the IC will be able to function reliably and meet its intended performance goals in a variety of real-world applications. Fig. 7 shows the process corner simulation result for the proposed Mutually Coupled LNA. As depicted in Fig. 7, the maximum value of S_{21} achieved for FF corner is 10.04 dB while maximum value for SS corner is 17.87 dB. Similarly, S_{11} simulation under the four-process corner shows good results.

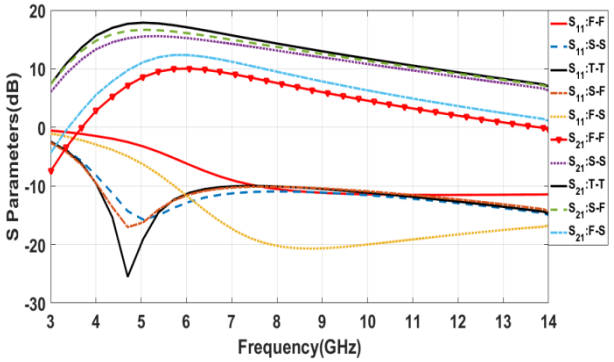

Fig. 7. Process corner for proposed mutually coupled LNA

The overall evaluation of LNA is calculated using FoM [8]. As given in equation (16), FoM comprises the gain (max.), NF (min.), bandwidth (max.) and power dissipation.

$$FoM = \frac{S_{21av.[lin]} \times BW_{[GHz]}}{P_{dc[mW]} \times (F_{av.[lin]} - 1)} \quad (16)$$

The proposed LNA FoM is 17.34, indicating that it is optimal for the required band. Table 2 compares the proposed LNA's success to those of other papers.

4. Conclusion

A mutually coupled CG-CS stage LNA has been designed using 45 nm CMOS technology. The proposed LNA simulated for the 4 – 14 GHz bandwidth has a maximum gain of 17.87 dB while having the NF of 5.45 dB. The input reflection coefficient has a value less than –10 dB throughout the entire band. A mutually coupled inductor has been proposed which will reduce the circuit size. The proposed LNA has the FoM value of 17.34.

References

[1] W. J. Lee, J. J. Liou, and W. R. Chen, "24 GHz low-noise amplifier using 0.1 μm InP HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 3, pp. 1059-1065, 2005.
[2] C. K. Lim, K. B. Kim, and K. J. Kim, "A 60 GHz low-noise amplifier using InP HEMT technology," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 9, pp. 597-599, 2005.
[3] X. Guan, H. Wang, Y. Liu, and X. Guo, "A 60 GHz cascode LNA with improved linearity and gain performance," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 9, pp. 727-729, 2016.
[4] C. Xu, J. Lin, H. Wang, Y. Liu, and X. Guo, "A 60 GHz CMOS LNA with inductor-peaking technique," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 10, pp. 838-840, 2016.
[5] Y. Jeon, K. Kim, and H. Yoon, "A 24 GHz low-noise amplifier in 0.18-μm CMOS with modified T-match network," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 10, pp. 560-562, 2006.
[6] W. Lee, J. Lee, J. Lee, and B. Kim, "A 60-GHz low-noise amplifier in 90-nm RF CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2891-2897, 2007.
[7] W. Lee, J. Lee, J. Lee, and B. Kim, "A 77 GHz SiGe low-noise amplifier with input matching," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 10, pp. 705-707, 2007.
[8] B.-Z. Lu et al., "A Submilliwatt K-Band Low-Noise Amplifier for Next Generation Radio Astronomical Receivers in 65-nm CMOS Process," *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 7, pp. 669-672, 2020.
[9] M.-Y. Huang, R.-Y. Huang, and R.-M. Weng, "A 0.3 V low cost low power 24 GHz low noise amplifier with body bias technology," *IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), Jul. 2017, pp. 519-522.
[10] C. Li, O. El-Aassar, A. Kumar, M. Boenke, and G. M. Rebeiz, "LNA design with CMOS SOI process-l.4dB NF K/Ka

band LNA," *IEEE MTT-S International Microwave Symposium Digest (IMS)*, pp. 1484-1486, 2018.
[11] M. Keshavarz Hedayati, A. Abdipour, R. Sarraf Shirazi, C. Cetintepe, and R. B. Staszewski, "A 33-GHz LNA for 5G wireless systems in 28-nm bulk CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1460-1464, 2018.
[12] S. Kong, H.-D. Lee, S. Jang, J. Park, K.-S. Kim, and K.-C. Lee, "A 28-GHz CMOS LNA with stability-enhanced Gm-boosting technique using transformers," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 7-10, 2019.
[13] A. A. Kumar, B. D. Sahoo, and A. Dutta, "A wideband 2-5 GHz noise canceling subthreshold low noise amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 7, pp. 834-838, 2017.
[14] B. Cui, J. R. Long, and D. L. Harame, "A 1.7-dB minimum NF, 22-32 GHz low-noise feedback amplifier with multistage noise matching in 22-nm SOI-CMOS," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2019, pp. 211-214, 2019.
[15] L. Gao and G. M. Rebeiz, "A 24-43 GHz LNA with 3.1-3.7 dB noise figure and embedded 3-pole elliptic high-pass response for 5G applications in 22 nm FDSOI," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 239-242, 2019.
[16] P.B. Huynh, J.H. Kim, and T.Y. Yun, "Dual-Resistive Feedback Wideband LNA for Noise Cancellation and Robust Linearization", *IEEE Transaction on Microwave Theory Techniques*, vol. 70, no. 4, pp. 2224-2235, 2022.

Table 2. Comparison of the Proposed Work with Other Papers

References	Process	Freq (GHz)	B.W.	Gain	NF (dB)	P_{DC} (mW)	FoM
[9]	0.18 µm	24	24	10.76	4.18	1.09	6.42
[10]	45 nm	24 – 28	4	12.8	1.4	7	16.4
[11]	28 nm	33	33	18.6	4	9.7	2.55
[12]	65 nm	24.9 – 32.5	7.6	18.3	3.25	20.5	2.76
[15]	22 nm	20 – 44	24	23	3.1	20.5	14.5
This work	45 nm	4 – 14	10	17.87	5.45	1.8	17.34

Dheeraj Kalra obtained his master degree in information and communication technology from GLA University, Mathura, India. He is currently pursuing Ph.D. from NIT Jamshedpur, India. His areas of interest include radio frequency integrated circuit design and other latest trends in technology. He has more than 11 years of experience in teaching and research in the area of integrated circuits.

Vishal Goyal is a senior member IEEE, received his B. E. degree in electronics engineering from Nagpur University, India in year 2001 and M. Tech degree in digital communication from Uttar Pradesh Technical University, Lucknow in year 2006. He received his PhD degree from GLA University, Mathura in year 2016. His research interests include nonlinear control, adaptive control and sliding mode control, process control, evolutionary algorithms, RF integrated circuits and intelligent systems.

Manish Kumar obtained his Ph.D. degree in RFIC master degree in VLSI. He is currently working in high frequency analogy circuit such as LNA, Mixer, Power Amplifier and oscillator. He is also used optimization technique such as PSO, FA, GA etc. in circuit design and other latest trends in technology. He has more than 19 years of experience in teaching.

Mayank Srivastava obtained Ph.D. in analog integrated circuits and signal processing from Jamia Millia Islamia, New Delhi, India, in 2015. Presently he works as an Assistant Professor with Department of Electronics and Communication Engineering, National Institute of Technology, Jamshedpur, India. His research interest is in the areas of analog circuits. Dr. Srivastava has authored or co-authored 50 research papers in SCI/Scopus indexed International Journals and Conferences. He acted as reviewer of various SCI Indexed international journals and worked as a member of technical program committee/ reviewer/ session chair in several international conferences in India and abroad.

Received 2 April 2023