

# Design and prototype of a 60 GHz variable gain RF amplifier with 90 nm CMOS for multi-gigabit-rate close proximity point-to-point communications

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This paper presents the implementation of a low-power and variable-gain 60 GHz millimeter-wave CMOS Amplifier designed for short-range multi-gigabit close proximity point-to-point communications. The design uses coplanar wave transmission lines to achieve 50  $\Omega$  input and output matching. Realized in a 90 nm CMOS process, the variable-gain VGA exhibits power consumption ranging from 4.7 mW to 39.1 mW, with gains spanning from 5.5 dB to 12.4 dB at 60 GHz and a 3 dB bandwidth exceeding 14.4 GHz. Input and output return losses remain below  $-10$  dB across the gain spectrum. Successful demonstration of gain controllability further validates the circuit's performance. The compact VGA die, inclusive of pads, has dimensions of 740  $\mu\text{m}$  by 920  $\mu\text{m}$ , thereby occupying a core area of 0.2  $\text{mm}^2$ . This design demonstrates the potential of low-power, high-performance VGAs in enhancing millimeter-wave communication systems.

Keywords: 60 GHz, CMOS, high-frequency amplifiers, low-power design, millimeter-wave, transmission lines, RFIC, variable gain amplifier (VGA)

## 1 Introduction

The 60 GHz millimeter wave band presents a promising opportunity for short-range multi-gigabit wireless communication applications due to the limited propagation of electromagnetic waves over longer distances at this frequency [1]. The unlicensed frequency band of approximately 7 GHz centered around 60 GHz has garnered increasing attention for millimeter-wave applications in settings like offices and households [2]. In these scenarios, the design of 60 GHz transmitter and receiver architectures has become a matter of concern [3-7]. Conversely, with the complementary metal-oxide-semiconductor (CMOS) microelectronic technology scaling down to dimensions below 100 nm in integrated memory and chip applications, CMOS circuits are capable of operating at millimeter-wave speeds. This attribute makes 60 GHz CMOS VGAs an enticing choice for transmitter and receiver circuits [8].

With high spectral efficiency, OFDM or high-order QAM wireless communication systems can effectively transmit multi-gigabit data from transmitter to receiver in the 60 GHz frequency band [9, 10]. Nonetheless, these systems exhibit significantly high power consumption at such elevated speeds, particularly during modulation and demodulation processes in the baseband. Furthermore, ensuring linearity in the millimeter wave transceiver chain contributes to additional power consumption. Moreover, despite its lower spectral efficiency compared to the methods mentioned earlier, impulse radio in Fig. 1 utilizing on-off-keying (OOK) modulation can transform electromagnetic pulses into

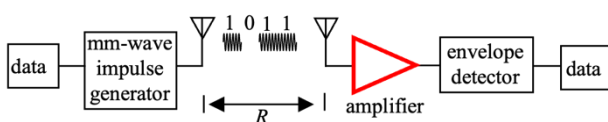
digital bits at multiple GBPS rates within the 60 GHz frequency band. The availability of an 8.864 GHz bandwidth, ranging from 57 GHz to 66 GHz, enables multi-Gbps communication [1]. This operation is achieved through a low-power millimeter-wave pulse generator [11, 12] and an extremely low-power envelope detector [13-15]. In multi-GBPS communication systems, the transmitter can remain off when there is no data, reducing power consumption. On the other hand, since the receiver is always on because it does not know when the data will arrive, it has a negative effect on the high power consumption of the receiving system in multi-Gbps communication systems when viewed in a long time window. The first active circuit element of the receiver system is the VGA. Therefore, it is essential to reduce the power consumption of the VGA.

This paper presents the design of a low-power, three-stage 60 GHz variable gain amplifier (VGA) utilized especially for 60 GHz band Multi-Gbps data rate close proximity point-to-point communication applications implemented using a standard 90 nm CMOS process. The VGA is specifically tailored for low-power short-range multi-gigabit OOK applications. Therefore, the VGA is optimized for low power and wide bandwidth by sacrificing linearity. S-parameter measurements reveal the VGA's capability to achieve variable power gain ranging from 5.5 dB to 12.4 dB at 60 GHz when operated under a 1.2 V supply voltage and the gain of the VGA is a linear function of the power consumption. Therefore the power consumption of the whole receiver system can be reduced when the millimeter-wave signal power is

strong for extremely low-power operations. Moreover, it exhibits an impressive 3 dB bandwidth of 14.4 GHz, while demonstrating input and output return losses of  $-19$  dB and  $-20$  dB, respectively. The VGA maintains input and output return losses better than  $-10$  dB across the operational frequency range, accompanied by a commendable minimum power consumption of 4.7 mW. Noise simulations indicate a noise figure of 5.1 dB at the center frequency of 60 GHz. Furthermore, it is noteworthy that the chip boasts a compact footprint, occupying a mere  $0.680$  mm<sup>2</sup>, which includes the area allocated for testing pads. The core area of the 60 GHz VGA is only  $0.2$  mm<sup>2</sup>.

## 2 Circuit design

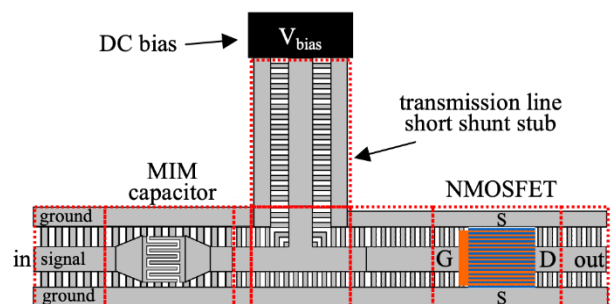
CMOS manufacturing technologies, widely employed for standard digital circuit production, offer numerous advantages in high-volume manufacturing. Additionally, it has been demonstrated that utilizing technology at 100 nm and below allows for the production of radio frequency circuits within the 60 GHz frequency range. However, challenges exist in the design of millimeter-wave communication circuits. Among these challenges, the absence of models in the millimeter-wave band and the rapid attenuation of electrical signals within the chip during transmission are the most significant. Consequently, the primary focus lies in acquiring specialized models for active metal-oxide-semiconductor field-effect transistors (MOSFET) and passive transmission lines operating in the targeted millimeter-wave band, as well as for metal-insulator-metal capacitors and transmission lines. The MOSFETs are the core component of the millimeter wave variable gain amplifier. We have conducted a comprehensive analysis of the MOSFET by incorporating the extrinsic high-frequency parasitic elements identified through on-wafer S-parameter measurements extending into the millimeter-wave spectrum. This approach involves augmenting the standard MOSFET models from the process design kit (PDK), which are primarily based on low-frequency parameters, with these identified high-frequency parasitic [16]. In this study, specialized models were initially developed for the millimeter-wave band, followed by the circuit design process.



**Fig. 1.** The block diagram of 60 GHz millimeter-wave impulse radio

There are several traditional techniques in millimeter-wave CMOS design, some of which include the usage of monolithic spiral inductors (MSI), microstrip lines (MSL), or coplanar transmission waveguides (CPW). Among all, using coplanar transmission lines brings about a couple of advantages, such as the ability to control the characteristic impedance by arranging the distance from ground planes and the control of the quality factor, which diminishes seriously at millimeter frequencies for other types of transmission lines [17]. On the other hand, in contrast to small sizes of chips with lumped spiral inductors, employing coplanar transmission lines causes the chip size to increase. Nevertheless, the behavior and flexibility of the coplanar transmission lines at millimeter frequencies provide an excellent solution for designing VGAs.

In the current study, we have incorporated a slow-wave transmission line (SWTL), as described in [16], for constructing the matching networks that connect the pads to the inputs and output of the Variable Gain Amplifier (VGA). Detailed analyses of this methodology are available in [18, 19], and the SWTL's architecture is depicted in Fig. 2.



**Fig. 2.** Illustration of the millimeter-wave circuit layout employed in this study

The unique feature of the SWTL lies in its design, where ground shields with slots are placed beneath the signal line and aligned perpendicular to the current's flow direction. This innovative configuration effectively slows down the wave's phase velocity, leading to a reduction in the wavelength at any given frequency. Such a reduction is advantageous in matching circuit designs that require specific wavelength lengths, allowing for shorter physical lengths in the layout. The phase constant ( $\beta$ ) of the SWTL exceeds that found in a standard microstrip line (MSL), enabling the achievement of a more condensed wavelength,  $\lambda$ .

Determining the effect of parasitic connections in the millimeter band is challenging. Therefore, transmission lines serve as both circuit components and connection elements. Circuit elements like transmission line stubs, T-junction connections, Metal Insulator Metal (MIM) capacitors, and NMOSFETs are integrated alongside transmission line blocks of varying lengths.

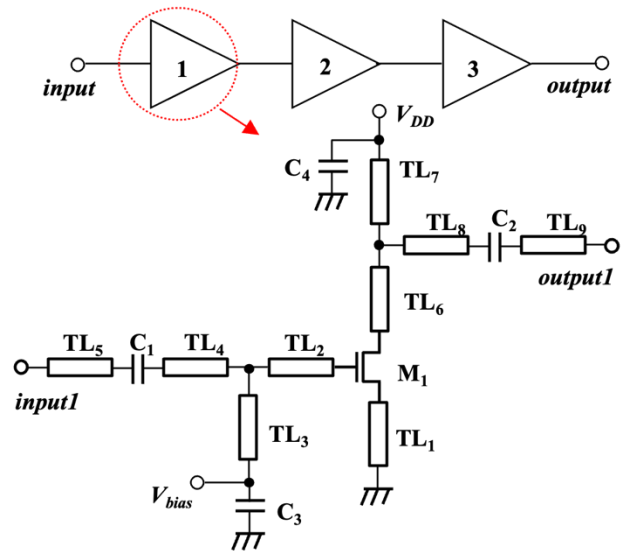
The model parameters for the on-chip 60 GHz transmission line, utilized in the design of the VGA, are provided in Table 1. This transmission line exhibits excellent performance within the 60 GHz millimeter-wave band, particularly in the design of RF circuits, including VGAs.

**Table 1.** Transmission line parameters

Parameter	Symbol	Value
Characteristic impedance	$Z_o$	$58.7+j1.9 \Omega$
Propagation constant	$\gamma$	$100.1+j2654.1 \text{ rad/m}$
Attenuation	$L$	0.87 dB/mm
Wavelength	$\lambda$	2.37 mm

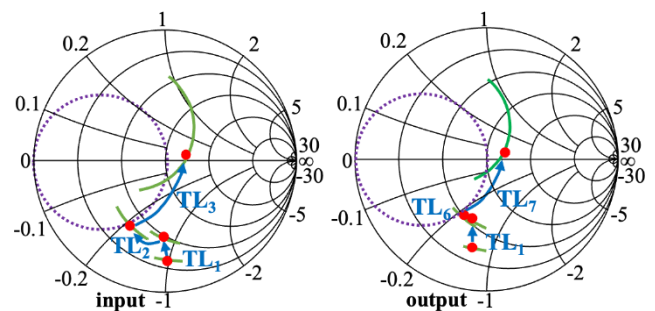
The millimeter-wave amplifiers, seen in Fig. 1, constitute the first and the most important block of the pulse receiver network such that the incoming signal is first amplified, adding noise as low as possible. VGAs are crucial with the fact that their performance directly contributes to the receiver’s performance itself. Because of this, the design steps should be carefully picked, and the trade-offs between many figure-of-merits, such as power consumption, gain-bandwidth product, and noise figure, must be well defined.

There are several structures for implementing an amplifier to determine a core topology. These structures include cascode, common-source, and common-source with source degeneration. Cascode topology offers good isolation between input and output, whereas the voltage headroom for the gain transistor is less than VDD. On the other hand, common-source topology is fast enough with the downside of impedance matching difficulty, but the voltage on the gain transistor is close to VDD. As for the common-source topology with source degeneration, high-speed operation is possible with easy impedance matching, which provides a preferable core topology for millimeter-wave impulse receiver designs. The circuit schematics of the designed 60 GHz VGA is shown in Fig. 3.



**Fig. 3.** Schematics of the 60 GHz CMOS VGA circuit

In this implementation, a three-stage Variable-Gain Amplifier is meticulously impedance matched to 50  $\Omega$  input and output impedances using single short stub impedance matching configurations between consecutive stages. The circuit schematic of the single short stub impedance matching using on-chip transmission lines is provided in Fig. 3. To enhance impedance matching, 130  $\mu\text{m}$  long transmission lines are strategically positioned at the source terminals of the NMOSFET devices. These transmission lines confer an inductance of 56 pH. In the design of impedance-matching stages, shunt transmission lines are judiciously connected to the gate terminals of the NMOSFET devices. These shunt transmission lines serve a dual purpose by aiding in impedance matching and regulating the bias voltages, denoted as  $V_{\text{bias}}$ , applied to the gates. Consequently, they facilitate control over power consumption.



**Fig. 4.** Input/output impedance matching in Smith chart

For every stage within the VGA, the single short stub impedance matching using on-chip transmission line impedance matching of  $50\ \Omega$  for both input and output is performed by following Smith Chart. The input and output matching procedures are shown in Fig. 4. The short connections are made to give the bias voltages at those nodes. In contrast, the open connections are terminated with high impedance instead of leaving the nodes unconnected. Once the input and output impedance of a single stage amplifier is designed to be matched  $50\ \Omega$ , three stages are connected to cascade to obtain better gain performance.

The NMOSFET transistors employed in the three-stage VGA are uniformly biased to the threshold voltage level using the same  $V_{\text{bias}}$  voltage. This consistent biasing strategy ensures the operation remains low-power. It is worth noting that there exists a trade-off between power consumption and gain, and this trade-off is scrutinized to establish an optimal operating point, as visually depicted in Fig. 5. The adoption of this low-power biasing approach may potentially lead to reductions in the 1 dB compression point and third-order intercept points, which could pose challenges for Orthogonal Frequency-Division Multiplexing (OFDM) or high-order Quadrature Amplitude Modulation (QAM) wireless communication systems due to the inherent nonlinearity of operation. However, it is important to underscore that this nonlinearity can be leveraged as an advantage in impulse receiver applications such as 60 GHz high data-rate OOK receivers [20].

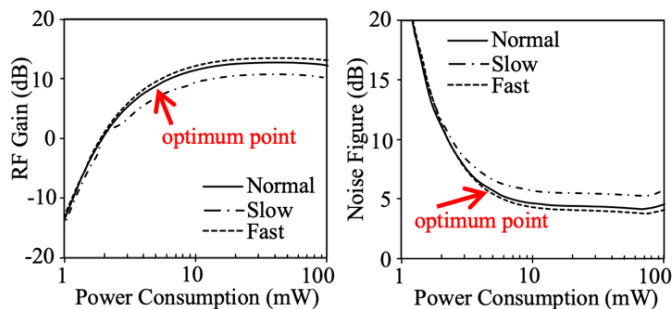


Fig. 5. Optimum operating point of the VGA

### 3 Results and discussion

The 60 GHz VGA aimed for millimeter-wave pulse receiver has been designed and implemented using the 1P8M 90 nm CMOS technology optimized for standard digital applications. Figure 6 shows the die photo of the realized circuit while it is measured on an on-chip probe station connected to a vector network analyzer (VNA),

and the dimension of the test circuit is  $740\ \mu\text{m} \times 920\ \mu\text{m}$  and its core size is  $400\ \mu\text{m} \times 500\ \mu\text{m}$  equal to  $0.2\ \text{mm}^2$ . The circuit has been tested on-chip probe station under the supply voltage of 1.2 V. Millimeter wave signals are applied to the input and output of the VGA using Ground-Signal-Ground (GSG) RF probes. Additionally, the DC supply voltage (VDD) and the analog gain control voltage ( $V_{\text{bias}}$ ) are applied using a Power-Ground-Power (PGP) multi-contact DC probe as shown in Fig. 6.

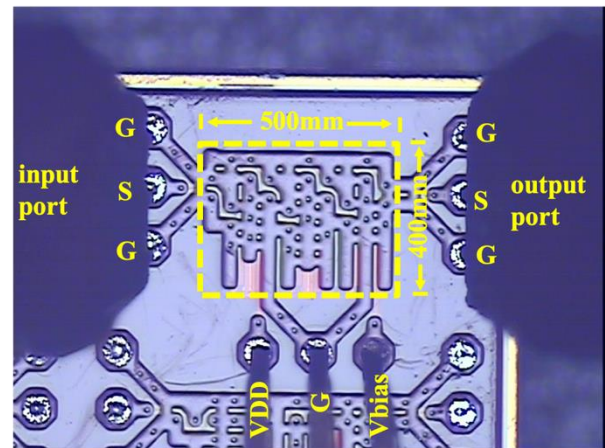
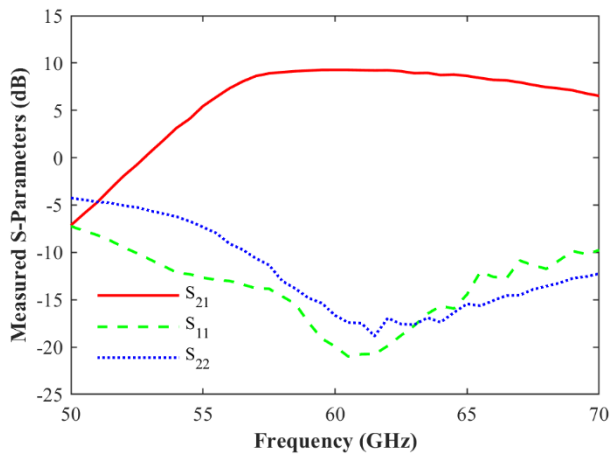


Fig. 6. Die photograph

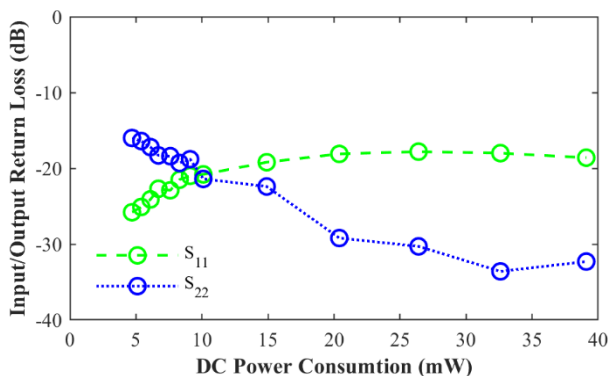
The gain, input, and output return loss measurements are done by using a 2 port VNA. Figure 7 illustrates a performance measurement graph for the implemented VGA operating at a gain of 9.3 dB with a 3 dB bandwidth of 14.4 GHz. This demonstrates the circuit's effective support for 60 GHz millimeter-wave impulse communication systems. Notably, the VGA can operate under a range of gain conditions, from 5.5 dB to 12.3 dB, while maintaining consistent input and output matching and bandwidth. The specific gain condition of 9.3 dB was chosen for presentation in this figure as it represents a median value within this operational range, providing a balanced example of the VGA's capabilities. The input and output return losses are measured  $-19$  and  $-20$  dB at 60 GHz center frequency. Moreover, input and output return losses are better than  $-10$  dB within the operating region of the VGA. As shown in Figure 8, it was determined that the input and output return loss remained below  $-10$  dB for all gain states of the circuit. In all measurements, this amplifier circuit successfully covers a wide bandwidth of 14.4 GHz. In addition, the simulated noise figure is obtained to be 5.1 dB.



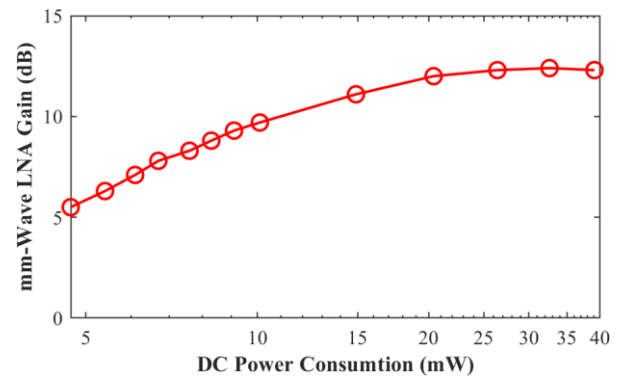


**Fig. 7.** Measured S-parameters of the ultra-wideband 60 GHz VGA

The performance of the examined amplifier was evaluated by meticulously controlling the  $V_{bias}$  signal. This circuit demonstrates a power consumption range from 4.7 mW to 39.1 mW, crucial for its amplification functionality. At a power consumption of 4.7 mW, the amplifier maintains its lowest gain of 5.5 dB, whereas its highest gain of 12.0 dB is achieved at 20.4 mW. Notably, saturation begins when the VGA gain reaches 12 dB, with further increases in bias leading to no additional gain enhancement. At a power consumption level of 39.1 mW, the gain plateaus at 12.3 dB. This study successfully validated the gain controllability of the proposed circuit. Figure 9 depicts the correlation between measured gain and power consumption for the VGA. The VGA operates within a gain range of 5.5 dB to 12.0 dB, corresponding to power consumptions of 4.7 mW to 20.4 mW, respectively, while ensuring a 14.4 GHz bandwidth and maintaining input matching well below  $-10$  dB across all bias conditions.



**Fig. 8.** Input/output return loss of the VGA versus DC power consumption



**Fig. 9.** Millimeter-wave band VGA gain versus DC power consumption

The performance of our designed and implemented VGA is rigorously compared against leading VGAs in the field [21-27], with a comprehensive summary presented in Table 2.

We introduce a novel figure of merit (FOM) for this comparison, defined by the ratio of energy consumption (in femtojoules) per bandwidth unit (Hz) to gain (dB). This FOM is particularly relevant for comparing on-off keying receiver circuits, as it correlates energy per bit with bandwidth-specific energy consumption and linear power gain. Our VGA exhibits a dynamic gain range from 5.5 dB to 12.0 dB across a 14.4 GHz bandwidth. The corresponding FOM fluctuates between 59 and 118 fJ per dB gain, indicating lower power consumption per Hz and thus superior performance. Notably, our circuit achieves the lowest FOM among the surveyed state-of-the-art VGAs. While advanced technologies can attain an FOM of up to 128, our design, leveraging passive modeling on a microstrip transmission line, outperforms even 65 nm CMOS technologies. This enhanced performance is achieved at the cost of a marginally increased chip area, necessary for the on-chip shunt transmission line matching circuit.

**Table 2.** Measurement performance summary of state of the art 60 GHz band VGA

Parameters	Units	This work	[21]	[22]	[23]	[24]	[25]	[26]	[27]
Technology	-	90nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	180nm SiGe	90nm CMOS	65nm CMOS	65nm CMOS
Gain range	dB	+5.5 to +12.0	-39.4 to +20.2	-29 to +23	+3 to +31	-2.7 to 17.7	-5.4 to 0.8	2.3 to 9.3	-9.4 to 6
3-dB bandwidth	GHz	14.4	4	1.25	1	9	7	14.1	10
Noise figure	dB	5.1	10 to 22	-	6 to 21	-	-	-	-
Core Area	$\mu\text{m}^2$	400×500	75×80	71×490	330×470	680×460	600×400	210×500	580×200
Power consumption	mW	4.7 to 20.4	26	31.2	48	50	31.2	16.8	25
Gain control mode	-	Analog voltage	Analog voltage	Digital voltage	Digital voltage	Analog voltage	Analog voltage	Analog voltage	Digital current
FOM	fJ/dB	59 to 118	322	1085	1548	314	5571	128	417

$$\text{FOM} = [\text{Power Consumption (W)}] / [\text{Bandwidth(Hz)}] / [\text{Gain(dB)}]$$

#### 4 Conclusion

In this study, a three-stage ultra-wideband 60 GHz variable gain amplifier utilizing a standard 90 nm CMOS process has been successfully developed and tested. Our design breakthroughs are evidenced by the VGA's dynamic gain range, which we tuned between 5.5 dB and 12.0 dB. Significantly, this gain variation is achieved with a minimal power consumption range of 4.7 mW to 20.4 mW, underscoring the efficiency of our design.

A standout feature of the VGA in all gain conditions is its robust performance metrics, particularly a return loss surpassing -19 dB and bandwidth that exceeds 14.4 GHz. These characteristics not only demonstrate the amplifier's high fidelity but also its capability to operate effectively over a broad frequency spectrum.

Our empirical findings are in close agreement with our simulation outcomes, lending credence to the reliability of our modeling approach. This correlation is especially pertinent in the context of millimeter-wave frequencies, where precision in modeling transistors and passive elements is crucial.

Given the encouraging results, we propose that our VGA design is highly appropriate for wide-band, low-power applications, especially in the context of 60 GHz millimeter-wave communications. Its application is notably pertinent in scenarios that demand multi-gigabit-rate transmissions over short distances. This is particularly true for point-to-point communications where high-data-rate transmission is essential while maintaining low power consumption, especially in battery-powered devices.

This work not only contributes to the advancement of CMOS technology in high-frequency applications but also opens new avenues for developing energy-efficient, high-performance communication systems.

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