Journal of Electrical Engineering, Vol. 75, No. 3, 2024, pp. 198-203

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PAPERS

Mutually coupled dual-stage RC feedback LNA for RF applications

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The designed circuit features a dual-stage Low Noise Amplifier (LNA) in which, a common source (CS) configuration is employed to achieve high gain, while the subsequent stage adopts a Complementary Common Gate (CCG) setup provide the low power consumption. This arrangement ensures that both transistors share the same biasing current, promoting energy efficiency. The two stages are interconnected in a cascade configuration, amplifying the overall gain and concurrently mitigating noise. To facilitate wideband matching in the input stage, a parallel RC feedback mechanism is implemented. Additionally, a pair of mutually coupled inductors in the CS and CCG stages contribute to rendering the input impedance exclusively resistive, concurrently minimizing the overall size of the circuit. All simulations were done using 65 nm CMOS technology in Cadence Virtuoso. The proposed LNA showcases a Noise Figure (NF) of 3.2 dB, a Peak Power Gain (S_{21}) of 19.8 dB, and an input reflection coefficient (S_{11}) of –16.2 dB, spanning a bandwidth of 3.1-6.2 GHz. Operating on a 1V power supply, the proposed LNA demonstrates power efficiency by consuming only 2.8 mW. The overall performance assessment of the LNA is gauged using the Figure of Merit, yielding an obtained value of 18.2. Comparative analysis with other cutting-edge designs is presented in Table 1.

Keywords: LNA, noise figure (NF), complementary common gate (CCG), mutually coupled, feedback, ultrawide band (UWB)

1 Introduction

In the realm of wireless communication, Radio Frequency (RF) transmitters play a vital role. Their adaptability is demonstrated by the diverse applications in various industries such as medical devices, Internet of Things (IoT) devices, satellite communication, healthcare, industrial settings, agriculture, and telecommunications [1]. Analyzing real-world applications provides crucial insights into the practicality and potential future developments of RF transmitter technology [2].

To achieve high data rates in the transmission of data, ultra-wideband technology operating within the frequency range of 3.1 GHz to 10.6 GHz is employed. Within the receiving chain of the RF receiver, the initial block is the LNA, tasked with amplifying exceedingly weak signals received from the antenna [3]. Consequently, the design of the LNA necessitates a careful trade-off to attain optimal performance concerning factors such as Gain, NF, matching networks, chip area, linearity, and biasing techniques [4, 5].

A number of LNA topologies are available: (A) Distributed amplifier in which a number of transistors are connected in parallel [6]. It has high gain but faces a large chip area. (B) Common gate topology, in which good input impedance matching are obtained as $R_{in}=1/g_m$ where g_m is the transconductance [7]. By setting the value of g_m, input impedance can be set for 50 Ω or 75 Ω as required but this topology suffer with high NF [8,9]. (C) The resistive feedback is another one well-known topology, which provides high gain and wide band matching. But NF is increased due to the number of resistances used in the same [10]. (D) Noise cancellation topology is used to increase gain and reduced in the NF [11,12]. (E) The inductive source degeneration provides a proper narrow band impedance matching at the input terminal [13]. Therefore, for large bandwidth source degeneration can combined with other topologies.

In this paper a combination of CCG stage is cascaded with CS used to increase the gain and low power consumption. A parallel RC feed-back is used at input stage for impedance matching to extend the bandwidth. Section 2 comprises circuit design and analysis. Section 3 analyses the result and discussion. Conclusion is given in Section 4.

2 Circuit analysis

The circuit depicted in Figure 1 comprises two stages. In the initial stage, NMOS transistors M_1 and M_2 are configured in cascode, resulting in the equivalent trans-conductance of the first stage being the product of g_{m1} and g_{m2}, where g_{m1} and g_{m2} represent the trans-conductance of transistors M_1 and M_2, respectively.

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https://doi.org/10.2478/jee-2024-0024, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

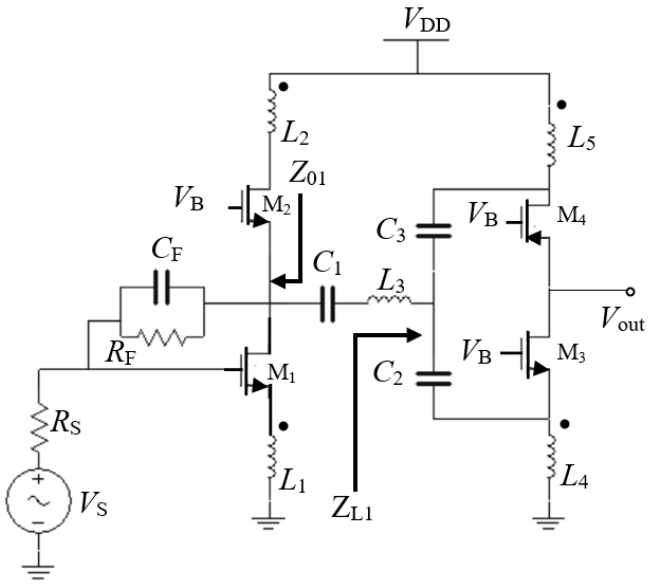

Fig. 1. Proposed LNA schematic

Inductors L_1 and L_2 are mutually coupled so that large value of inductance can be obtained with small area. A feedback path parallel combination of resistance R_F and Capacitor C_F is connected from output to input terminal for wide band input matching. Henceforth a large band width is obtained.

The second stage involves a complementary CCG configuration, where the PMOS transistor (M_4) is stacked atop the NMOS transistor (M_3). This arrangement ensures that M_3 and M_4 share a common biasing current, resulting in a reduction in power consumption. Stage-1 is cascaded with the CCG stage, leading to an overall gain that is the product of the gains of the individual stages. Capacitances C_1, C_2, and C_3, along with inductor L_3, are utilized for impedance matching in the first and second stages. Notably, inductors L_4 and L_5 are mutually coupled and play a crucial role in rendering the input impedance of the second stage purely resistive

(a) Input impedance

The input impedance looking from the gate terminal of transistor M_1 is given by equation (1) [14].

$$Z_{in}' = g_{m1}\frac{L_1 + M}{C_{gs1}} + L_1 s + M + \frac{1}{sC_{gs1}} \qquad (1)$$

where C_{gs1}, g_{m1} are the source gate capacitance and transconductance of transistor M_1 respectively; M is mutual inductance between inductors M_1 and M_2 and given by $M = \sqrt{kL_1L_2}$.

The coupling coefficient (k) represents the degree of coupling between inductors L_1 and L_2. A large impedance is obtained when looking from the drain terminal of M_1 towards M_2. So equivalent circuit is shown in Figs. 2(a), (b). Using Miller's effect, R_F' and C_F' are given by $R_F' = \frac{R_F}{1+A_{V1}}$ and $C_F' = C_F(1 + A_{V1})$, where A_{V1} is the gain of the first stage given by equation

$$A_{V1} = \frac{(Z_{in}'\, s\, C_{gs1} - g_{m1} Z_F)Z_{L1}}{(Z_{in}'\, s\, C_{gs1})(Z_F + Z_{L1})} \qquad (2)$$

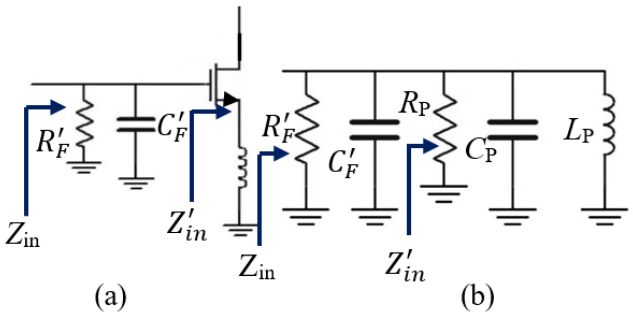

Fig. 2. (a) Miller's equivalent, (b) series to parallel conversion

Here, Z_F and Z_{L1} are the feedback impedance [15, 16] and load impedance of the first stage. Equation (1) is a series combination of inductive, capacitive and resistive terms. For simplicity it can be converted into parallel terms

$$R_P = \frac{R^2 + (\omega(L+M) - 1/\omega C)^2}{R}$$

$$L_P = \frac{R^2 + (\omega(L+M) - 1/\omega C)^2}{\omega^2 L}$$

$$C_P = \frac{1}{R^2 + (\omega(L+M) - 1/\omega C)^2 \omega^2 C}$$

as shown in Fig. 2(b). Therefore, the input impedance Z_{in} is approximately given by equation

$$Z_{in} = \left(sL_P \left\| \frac{1}{s(C_F' + C_p)} \right\| \frac{R_F'.R_P}{R_F' + R_P}\right). \qquad (3)$$

The input impedance can be matched for 50 Ω by adjusting the value L_P, R_P, C_P for UWB frequency range.

(b) Noise figure

From a reduction standpoint, the noise of the first stage should be taken into consideration [18]. The noise of the subsequent stage can be neglected because its value is divided by the preceding stage noise figure of first stage is given by equation

$$F_{in} = \frac{V_{n1}^2}{A_{v1}^2}\frac{1}{4kTR_s}, \tag{4}$$

where V_{n1}^2 depicted the total noise power at the output of the first stage. Mathematically, noise power V_{n1}^2 is given by equation

$$V_{n1}^2 = 4kTR_{L2}\ \frac{Z_{01}^2}{Z_{01}\ R_{L1} + Z_{LC}}, \tag{5}$$

where Z_{01} is the output impedance of first stage and R_{L1} and Z_{LC} are resistive and total impedance of the second stage, respectively. By optimizing the value of Z_{LC}, the noise figure can be reduced.

3 Results and discussion

3.1 *S*-parameters

S-parameters are shown in Fig. 3. *S*-parameters represent the way the electrical signal is transmitted and reflected by network of components. These parameters are crucial in the design and analysis of high-frequency circuits, such as those in communication systems. Forward voltage gain (S_{21}) depicts the voltage transferred from the input to output, and the input reflection coefficient (S_{11}) represents the reflection at input side.

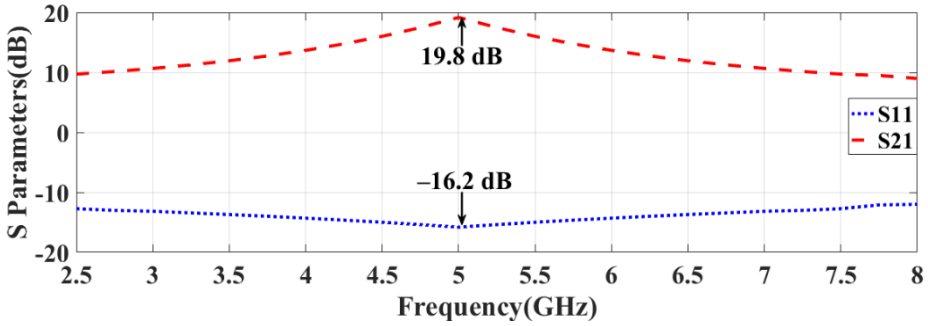

Fig. 3. Proposed LNA with *S*-parameters S_{21} and S_{11}

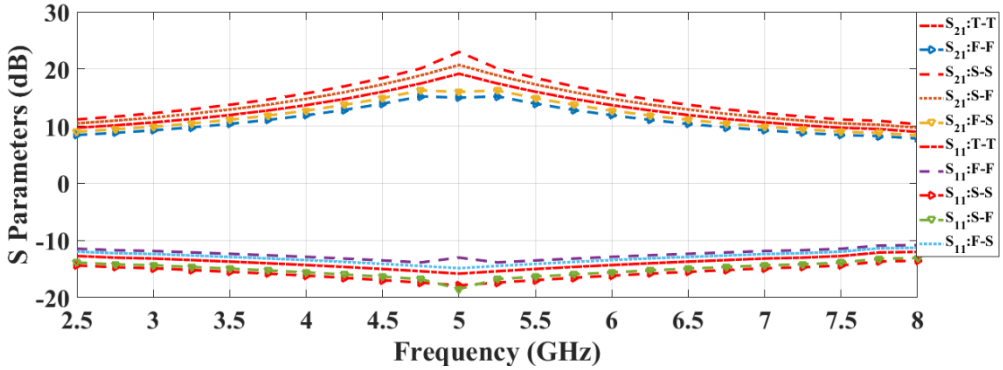

Fig. 4. Process corner simulation (S_{21}, S_{11})

S_{21} and S_{11} are simulated for frequency range 2.5 GHz to 8 GHz in cadence virtuoso software and shown in Fig. 3. S_{21} is positive for the frequency range and depicted maximum value 19.8 dB at frequency 4.9 GHz. S_{11} is also negative for frequency range 2.5 to 8 GHz. and the minimum value –16.2 dB is obtained at frequency 4.9 GHz.

3.2 Process corner simulation

Process corner simulation shown in Fig. 4 refers to the analysis and simulation of how variations in manufacturing processes can affect the performance of electronic components. Simulations is done for all corners. (a) Slow-Slow (SS) the worst-case scenario,

where transistors are slow due to process variations. (b) Fast-Fast (FF) the best-case scenario, where transistors are fast due to process variations. Slow-Fast (SF) and Fast-Slow (FS) corner simulations have also been done. Figure 4 shows no variations more than ten percent for all corners for the whole frequency range from 2.5 GHz to 8 GHz.

3.3 Noise figure

The noise figure of a device is a measure of how much the device degrades the signal-to-noise ratio of an input signal. Mathematically NF is given by

$$\text{NF (DB)} = 10\log_{10}\frac{\text{signal-to-noise ratio at input}}{\text{signal-to-noise ratio at output}}$$

Simulation is done for a frequency range 2.5 GHz to 8 GHz and shown in Fig. 5. The result shows the minimum NF of 3.2 dB at a frequency of 5.1 GHz.

IIP3 is the third order input intercept point which measures how well an LNA can handle multiple input signals without generating significant intermodulation distortion. Specifically, it represents the input power level at which the third-order nonlinear product will increase by 3 dB in power when the input power is raised by 1 dB.

Figure 6 represents the input and output power levels and depicted the IIP3 of 3.95 dBm. FoM typically stands for Figure of Merit and is used to analyze the performance of LNA on single platforms [18]. It includes the term NF, bandwidth, IIP3, power gain and power supply voltage and mimetically given by Eqn. (6). Table 1 is used to compare the proposed work with existing state of arts.

$$\text{FoM} = 20\log_{10}\frac{BW_{GHz}\times S_{21}\times IIP3_{mW}}{P_{dc(mW)}\times(F_{av(ln)}-1)} \quad (6)$$

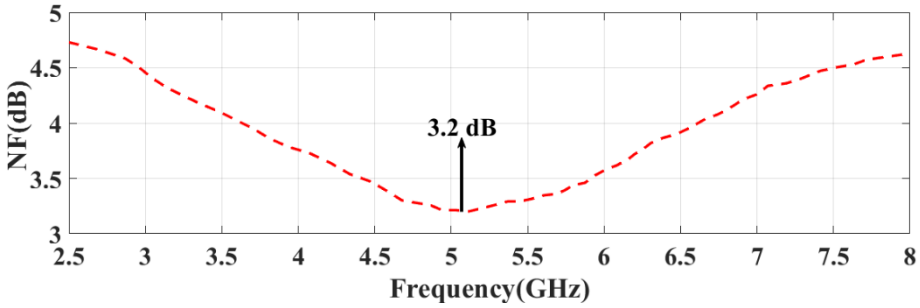

Fig. 5. NF for proposed LNA

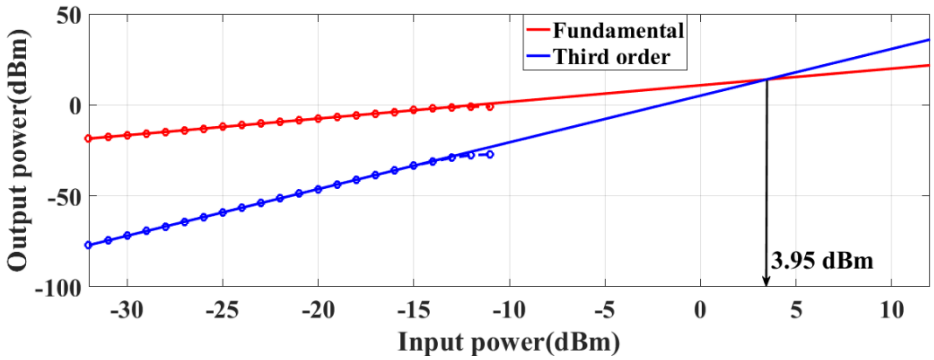

Fig. 6. IIP3 in high gain mode

Table 1. Comparison of current state-of-the-art with the proposed LNA

References	[12]	[19]	[17]	[3]	Proposed work[s]
NF_{min} (dB)	2.8	3.8	2.76	3.9	3.2
Bandwidth (GHz)	0.3-3.9	0.2-2.0	0-5	1.7-9.8	3.1-6.2
S_{11} (dB)	<–11	<–12	<–11	<–1	<–12.5
P_{DC} (mW)	5.7	3	10.4	10.6	2.8
S_{21} (dB)	18	7.9	12.8	13.4	19.8
Power supply (V)	1.1	1.3	1.8	1.8	1
Technique	Noise cancel-lation	Feed-back	Dual feed-back	Post distor-tion	CCG-CS current reuse
FoM	22	12	–5.9	-	18
Technology	130 nm	130 nm	180 nm	180 nm	65 nm

4 Conclusion

The proposed LNA circuit is comprised of two stages: the first stage adopts a CS configuration, and the second stage is a CCG setup. The CS stage is cascaded with the CCG stage to enhance the overall gain, as the total gain is the product of individual gains. A parallel RC feedback is implemented in the input stage for broad input matching, and the impedance characteristics are mathematically analyzed using Miller's theorems. To achieve a purely resistive input impedance and reduce the circuit's size, a pair of mutually coupled inductors are incorporated into both the CS and CCG stages. All simulations are conducted using Cadence Virtuoso with 65 nm CMOS Technology. The proposed LNA demonstrates a NF of 3.2 dB, a peak power gain (S_{21}) of 19.8 dB, and an input reflection coefficient (S_{11}) of –16.2 dB. Operating at a 1 V power supply, the LNA consumes 2.8 mW. The overall performance is assessed through the figure of merit, yielding a value of 18.2.

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Received 20 February 2024