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Area and energy optimized Hamming encoder and decoder for nano-communication

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The Hamming code or Linear block code is used in communication to identify and repair errors. Redundancy bits are introduced to the Hamming communication network (HCN) for error detection and correction. It can detect two errors and correct one error. Quantum-dot Cellular Automata (QCA) is used for designing circuits with high switching speed and low energy dissipation. This work proposes a cost-effective QCA-based (7, 4) Hamming encoder and decoder design. Hamming encoder is designed using coplanar structure and the error detector used in Hamming decoder uses a multilayer structure. The effort is to optimize the area, cost, and energy dissipation. The work proposes a coplanar (7, 4) Hamming encoder and decoder. Hamming decoder is implemented in two parts a syndrome calculator and an error detector. Proposed (7, 4) Hamming encoder circuit reduces cell count by 49.47% compared to [1] and 9.52% compared to [12]. The proposed (7, 4) syndrome calculator has reduced cell count by 56.54%, an 11.11% reduction in total area compared to [1]. The proposed design reduces the cell area, QCA cost, and also energy dissipation. The designs are realized and QCA parameters are assessed in QCADesigner2.0.3 and energy is analyzed in QCADesigner-E.

Keywords: clocking, error detector, Hamming decoder, Hamming encoder, QCA, latency, syndrome calculator

1 Introduction

Device density, operating speed, and power loss are challenging aspects for nano-computer and nano-communication devices. The extensively used CMOS technology must be replaced since it has reached its physical limits. Quantum-dot cellular automata (QCA) is among the best CMOS alternatives. QCA is recognized as the best CMOS successor due to the development of extremely dense and compact Nano scale designs. The technology comprises a QCA cell, a majority voter (MV) gate, an inverter, a simulation engine setup, and a simulation-type setup. For developing digital logic circuits with a high level of integration, switching speed, and lower energy dissipation, QCA is preferred [1-3].

The QCA's quantum-dots are an essential component. In cellular automata, self-production results from the Columbic force of attraction between QCA cells. QCA is characterized by smaller device sizes, higher switching speeds, and lower energy dissipation. Here, electrons are essential for many logic operations as well as the transmission of digital information. An electron, or electrical charge, is held there by a three-dimensional structure. The QCA-based structures can also be used to realize sequential circuits [4, 5].

Noise and other external factors might skew the data sent during digital transmission. When the sent data and the input data are not the same an error occurs. The error causes significant data to be lost. Bits '0' and '1' are used to transfer data. Any alteration to one of the bits could have an impact on the system's overall performance. Bit errors occur when the bit '1' is transformed into the bit '0' or vice versa.

Hamming codes, also known as linear block codes, are a class of codes that, by combining parity and parity bits, conduct detection of error and error correction, resulting in efficient error detection and correction coding methods [6]. Redundancy bits are introduced to a Hamming communication network (HCN) for error detection and correction [1]. Parity and message bits are sent through the channel in a coded manner. When a coded signal is received, the receiver identifies the parity bits from the data bits and, if an error is found, further corrects it. By including three parity bits, the Hamming encoder (7, 4) converts four bits of data into seven bits. It has single-bit error detection and correction capabilities. After being examined for errors or corrected if any do occur, the received data is decoded using the (7, 4) Hamming decoder back into its original four bits.

The objective of the work is to design and implement an area and energy-efficient Hamming code circuits. These circuits can be used to detect up to two-bit errors and correct one-bit errors. The proposed Hamming encoder and decoder structures are constructed with fewer cells than the reference structure, which lowers the

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overall QCA cost. The Hamming coding circuit has a significantly lower cell count, overall area, and QCA cost, which results in low energy dissipation. Energy analysis is carried out using QCADesigner-E, and all the structures are constructed using QCADesigner2.0.3.

The rest of the article is devised as follows. Section 2 discusses the literature review of different papers. Section 3 deals with the basics of QCA. Sections 4 and 5 deal with the QCA realization of (7, 4) Hamming encoder and Hamming decoder respectively. Section 6 deals with the results and discussion and lastly, the conclusion derived has been discussed in Section 7.

2 Literature review

Device scaling with higher switching speed and reduced power consumption are some benefits of CMOS technology, which has long been the industry standard for creating VLSI devices. Because of the QCA design, which decreases energy dissipation at the nanoscale, information may be processed more quickly. Since there are four clocks present rather than just one, CMOS requires a set of special design rules [1]. QCA requires the clock to be used for both combinational and sequential circuits, in contrast to traditional CMOS technology. Clocks are required in all QCA cells to control and synchronize the information flow. QCA has four clock phases [2].

Like other error detection and repair codes, parity bits are used in the Hamming code [3], to read or receive them during data transmission and verify their accuracy; these bits are appended to the data. An error-correction algorithm can point to the precise location of a single-bit fault using several parity bits.

Four quantum dots are present in each QCA cell. The electrons are compelled to inhabit the cell's furthest corner due to electrostatic interactions (repulsion) between the adjacent dots [4]. Additionally, the QCA cell has unique measurements that are essential for calculating area. These cells are 18 nm in height and width and are separated from one another by 2 nm [5].

To identify and rectify bit errors that occur during data storage or transmission, the Hamming code network is used for error detection and correction. The hamming code generator encrypts message bits using extraneous bits [6]. Parity or redundant bits are positioned at various points in the message/input bits. The required calculation is finished once the coded bits are received and performs a new calculation to obtain the error bits. Single-bit errors can be found when a data bit has been altered by noise during transmission, as indicated by the parity count displaying an incorrect number of ones. By combining codes with multiple parity bits, two-bit mistakes can be found, and each is computed on a distinct set of bits (data). The bit count of the data determines how many parity bits are required in this case [7].

There are several 3:8 decoders implemented using QCA, but the majority of their input/output ports are located inside the unit, hidden from view by other cells, making it complex to use extensively and as a foundational element to create more intricate circuits [8]. The 3:8 decoder circuit proposed in [9] is very optimized and cell area usage is better with less QCA cost and also dissipates less energy.

The ability of a receiver to repair errors in the data it receives is referred to as forward error correction (FEC), used in data transfer [9]. To achieve this, a transmitting station must amplify the transmission's data. Hamming codes lower the cost of implementing FEC by adopting a block parity approach. By including three parity bits, the Hamming encoder converts four data bits into seven bits. It can repair one bit of error and identify two bits of errors [10]. The receiver side of digital data transmission employs a Hamming decoder circuit. It is used to identify and decode faults in received data packets [11].

3 Basics of QCA and HCN

3.1 QCA cell

QCA circuit is constructed using a set of cells (quantum cells), which is a benefit of QCA. Four quantum dots make up each QCA cell, arranged in the corners of the cell. Two free electrons, often referred to as active electrons, are put opposite one another in a QCA cell to charge it [3]. Two different types of configurations are created depending on where the electron pair positions are in the cell. The polarizations $P = +1$ and $P = -1$ are used to denote these setups. $P = +1$ denotes logic '1', while the latter logic '0'. The two polarizations' values are formulated [8].

The QCA benefit is that it does not require a supply source; rather, the logical value is determined by the locations of the electrons. The QCA cell's adjacent dots (with a dot diameter of 5nm) are attracted to the neighboring cell electrostatically. This phenomenon causes quantum tunneling, which causes the electrons to occupy the corner positions of the cell the majority of the time. The QCA gates used to build logic circuits are the wire, inverter, and majority voter (MV) gates. When two cells are aligned in a canted pattern in a QCA, a corner cell inverter, which is a NOT gate, is achieved. The robust inverter, used in QCA, is realized using an arrangement of seven cells. In a QCA, wires are realized by placing the cells in a vertical or horizontal array pattern to transmit data between two sites [12]. The three-input logic circuit also known as MV gate is the core element of QCA. QCA speeds up operations and increases operating frequency while reducing data processing latency [13].

3.2 QCA clocking

Clocking is a feature that QCA offers and is essential for developing logical cells/ circuits. Four clock phases are used for each QCA cell, which are switch, hold, release, and relax. The barriers are raised, the pressures opposing the movement of the electrons inside each cell, and the flow of the electrons is moderately reduced during the switch phase. Barriers are increased high enough during the second clock (hold) phase to use the outputs as inputs during the next phases. The barrier force reduces during the clock's release phase, causing the electrons to relax into an unpolarized condition [13]. Cellular barriers were significantly decreased during the relax phase. They have no polarization, and inside the cell, electrons can go back and forth [15].

3.3 Crossover

Two types of crossovers are used in QCA, one coplanar and another multilayer. For coplanar, crossings can be regular or rotated cells [17]. Rotated cells are used in coplanar wire crossing. When aligned properly, the rotated and regular cells do not interact with one another. This intersection is based on the idea that, when placed next to one another, a consistent cell with dots placed transversely and a cell with dots swapped by 45 degrees exhibit extremely small mutually beneficial interactions. With the two different cell positions: one with conventional cells and the other with rotated cells. The coplanar crossing can communicate information on its own [18].

If the coplanar crossing does not meet the requirements of the archetype, it is necessary to provide an alternative for some marginal approaches to signal crossing. Signals can efficiently cross over to another surface when using multi-layer crossing [19].

The vertical QCA cells are used to stack the different layers of the logic architecture on top of one another. In the topmost layer, there are crossover wires. Between the top and bottom layers, the intermediate layers serve as a connecting element [20]. The middle layer serves as the active element that unites the two levels' designs. As a result, designs implemented in a multilayer approach have superior area optimization than coplanar crossings and have a more reliable signal connection.

3.4 Hamming communication network

Hamming codes are used to detect and correct errors that happen when data is sent from the sender to the receiver. Hamming codes are used to develop a systematic error detection and correction coding scheme. Redundancies are an essential component of these codes' error-detection and -correction mechanisms. Like other error-correcting codes, hamming code makes use of parity bits. To maintain the accuracy of the data, parity bits are inserted when it is received. It may locate the data unit and identify a one-bit error within the data unit by utilizing the parity bits. Once data bits are received at the receiver, the message and parity bits are separated. Any errors if identified are corrected.

Figure 1 illustrates the system-level diagram of the HCN. Message bits $I = (I_1, I_2, \ldots, I_k)$ are to be fed to the Hamming encoder and are encoded as code word $E = (E_1, E_2, \ldots, E_k)$. The codeword is constructed by considering (n-k) parity check bits followed by k message bits. For HCN, the codeword has to satisfy

$$E = I \times \mathbf{G} \tag{1}$$

where **G** is the generator matrix.

The code word is sent via the channel, presence of the channel noise may change the received data (different from E). Bits $R = (R_1, R_2, \ldots, R_k)$ represent the received vector at the channel output with an error e. The received data is decoded using the Hamming decoder [12].

The syndrome of the received vector is represented as

$$S^T = \mathbf{H}R^T \tag{2}$$

$$\mathbf{H}\mathbf{G}^T = 0 \tag{3}$$

where **H** is the parity check matrix.

The decoded codeword I^* is given by

$$I^* = R \oplus e \tag{4}$$

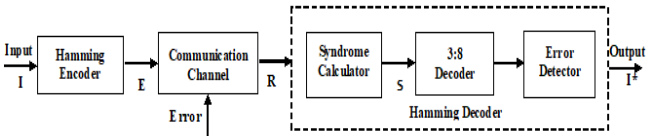

Fig. 1. System-level diagram of Hamming communication network

4 QCA implementation of (7, 4) Hamming encoder

In (7, 4) Hamming encoder, the output bits (E3 to E6) are obtained directly from the message bits (I3 to I6), and the next three bits (E0 to E2) by XOR operation of the bits as per Eqns. (5) to (7).

$$E0 = I6 \oplus I4 \oplus I3 \tag{5}$$

$$E1 = I6 \oplus I5 \oplus I3 \tag{6}$$

$$E2 = I6 \oplus I5 \oplus I4 \tag{7}$$

The block diagram of the (7, 4) Hamming encoder (HE) circuit is shown in Fig. 2. It consists of three 3-input XOR gates, inputs I6 to I3, and outputs E6 to E0.

The QCA-based realization of the proposed (7, 4) HE is shown in Fig. 3.

QCA cell specifications are as follows: cell width 18 nm, cell height 18 nm, and dot diameter 5 nm [21]. HE in [1] uses a multilayer crossover structure and has the disadvantage of increased cell area. The proposed coplanar design overcomes this by using simple gates with reduced cells and compact area usage. The proposed design is more compact than in [1] and has an area of 0.13 μm^2. The proposed design is more compact (occupies less cell area) and structured input and output terminals. The proposed coplanar HE can be used in the implementation of complete HCN.

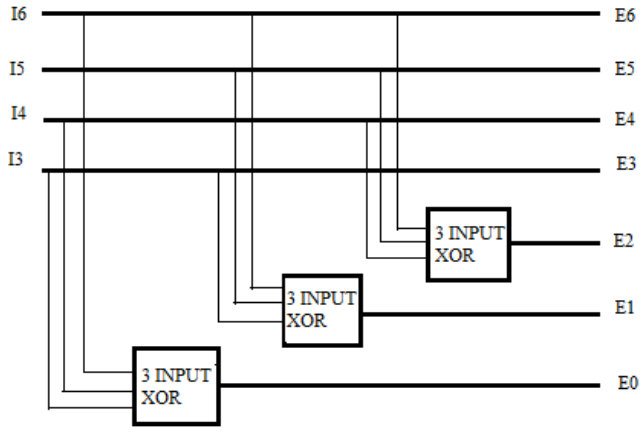

Fig. 2. High-level representation of (7, 4) Hamming encoder

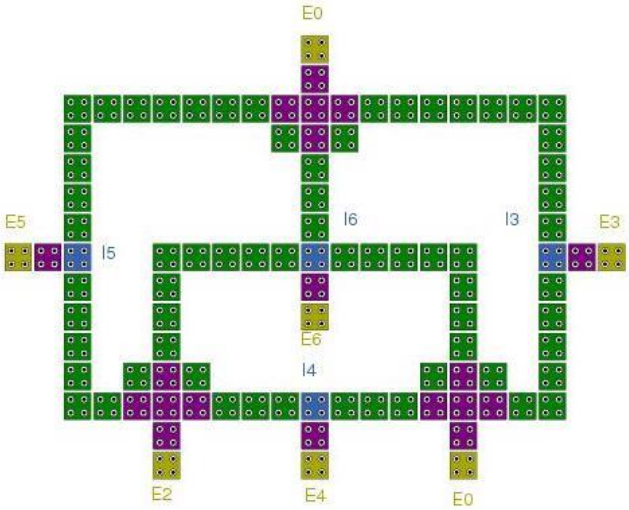

Fig. 3. QCA-based proposed coplanar (7, 4) Hamming encoder circuit

5 QCA implementation of (7, 4) Hamming decoder

For the implementation of the QCA-based (7, 4) Hamming decoder (HD), three syndromes are calculated using Eqns. (8) to (10). The four-input XOR gate can be used to produce the syndrome. It is possible to identify errors and their locations by the 3-bit syndrome's value, but at this time, errors cannot be corrected.

$$S1 = E6 \oplus E5 \oplus E4 \oplus E2 \quad (8)$$

$$S2 = E6 \oplus E5 \oplus E3 \oplus E1 \quad (9)$$

$$S3 = E6 \oplus E4 \oplus E3 \oplus E0 \quad (10)$$

The 3:8 decoder's input is connected to the 3-bit syndrome, and then the exclusive OR operation is conducted with the output and matching input code to get the right code group. The system-level diagram of the HD circuit is shown in Fig. 4. The 3:8 decoder circuit proposed in [9] is more compact and has better cell area usage with less energy dissipation and cost. Hence, it is used in the design of the proposed HD. The HD consists of three three-input XOR gates, seven, two-input XOR gates, and a 3:8 decoder. For the HD circuit, the input bits are E6 to E0, and the output bits I6 to I3.

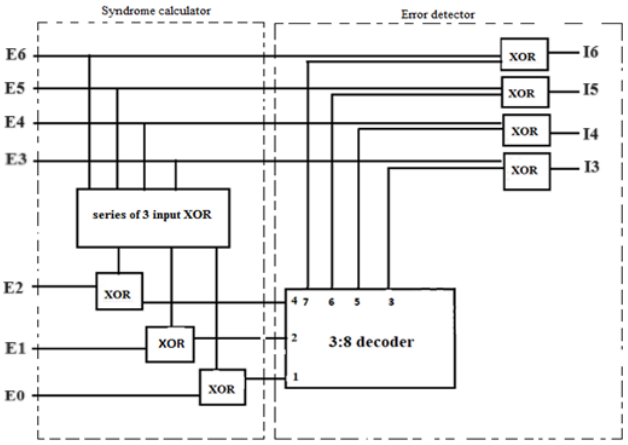

Fig. 4. Block diagram of (7, 4) Hamming decoder circuit

The proposed HD is composed of a syndrome calculator and an error detector. To design a 3-bit syndrome calculator, the information bits first perform a 3-input XOR operation and then a 2-input XOR operation with the matching supervisory bit as shown in Fig. 5. Table 1 shows the corresponding syndrome and the error code positions. The relation between the eight syndrome bits and the 3:8 decoder is mapped in Tab. 2. An incorrect error bit position is selected; this process is called error detection. Using the Hamming circuit two errors can be detected and one bit error can be corrected.

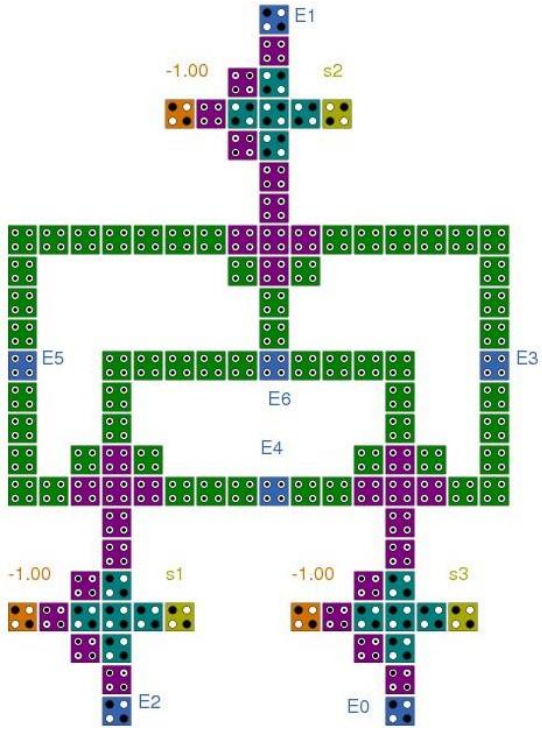

Fig. 5. Proposed QCA-based syndrome calculator

Table 1. The syndrome values with error code position

$S_1S_2S_3$	Error position	$S_1S_2S_3$	Error position
001	e0	101	e4
010	e1	110	e5
011	e2	111	e6
100	e3	000	

Table 2. A set of test vectors for the error detector

$E_6E_5E_4E_3$	$S_1S_2S_3$	Error in position	$E_6E_5E_4E_3$
0000	000	-	0000
0001	000	-	0001
0101	000	-	0101
1010	000	-	1010
1111	000	-	1111
0001	011	e3	0000
0011	101	e4	0001
0001	110	e5	0101
0010	111	e6	1010
1111	100	e2	1111

The error detector is implemented using a 3:8 decoder and 2-input XOR gates. The 3:8 decoder uses the 3-bit syndrome as its input, and the exclusive OR operation is conducted with the output and matching error code to get the right code group I6, I5, I4, and I3 as shown in Fig. 6. The circuit is realized in multilayer structure using four layers. The error detector consists of a 3:8 decoder and four XOR gates. Designing error detectors in a single layer will increase the number of cells. To decrease the area usage and cell count, the error detector is designed in four layers. In which three layers are used for decoder implementation and the fourth layer is used for the XOR gates and outputs. Further, HCN can be designed by changing the intermediate connecting lines without any significant changes to the circuit topology.

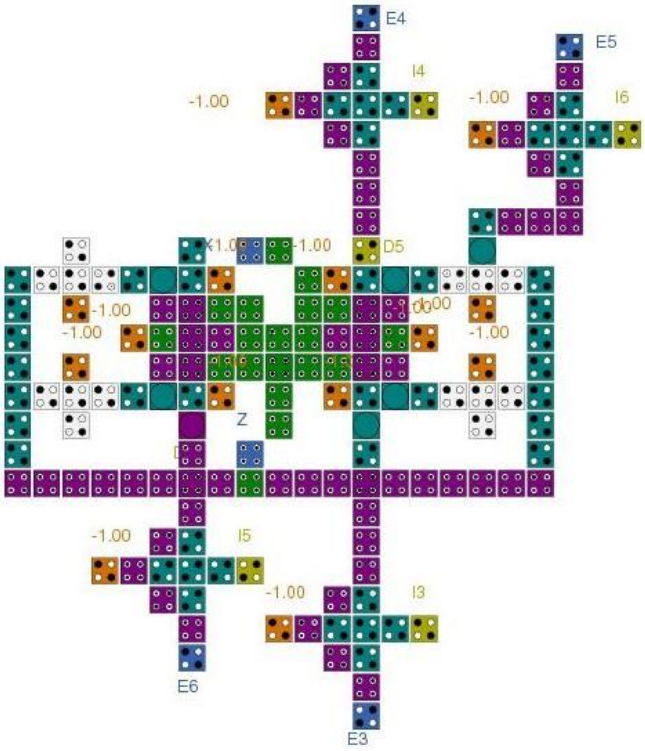

Fig. 6. Proposed QCA-based error detector

6 Results and discussion

The circuits discussed in Sections 4 and 5 are realized and analyzed with respect to QCA performance parameters (cell count, total area, latency, cost, …) in QCADesigner2.0.3 and computed the energy dissipation in QCADesigner-E. The Hamming encoder and syndrome calculator are simulated using the Bistable approximation method and the error detector using the coherence vector method. The obtained results along with the inferences drawn are discussed in this section.

6.1 (7, 4) Hamming encoder

The designed (7, 4) HE circuit has been analyzed for the cell count, latency, energy dissipation, and cost functions. The simulated waveforms of the Hamming encoder are shown in Fig. 7. The inputs are represented as I3 to I6 and outputs E0 to E6. The output signals E3

to E6 are the same as inputs I3 to E6 whereas E0 to E2 are computed using Eqns. (5-7). The results obtained are tabulated in Tab. 3. The HE structures in [1] and [12] have the disadvantage of increased cell count. The results are compared with the coplanar encoder design presented in [12].

Table 3. Performance analysis of QCA-based (7, 4) Hamming encoders

QCA Parameters	[1] coplanar	[12] coplanar	Proposed coplanar
Cell count	188	105	95
Total area (μm^2)	0.16	0.13	0.129
Cell area (μm^2)	0.061	0.034	0.031
Delay (Clock zones)	2	2	2
ADC	0.64	0.52	0.516
Average ED (meV)	6.8	5.65	5.61
Total ED (meV)	74.8	62.2	61.5
EDC	0.0224	0.0155	0.0151

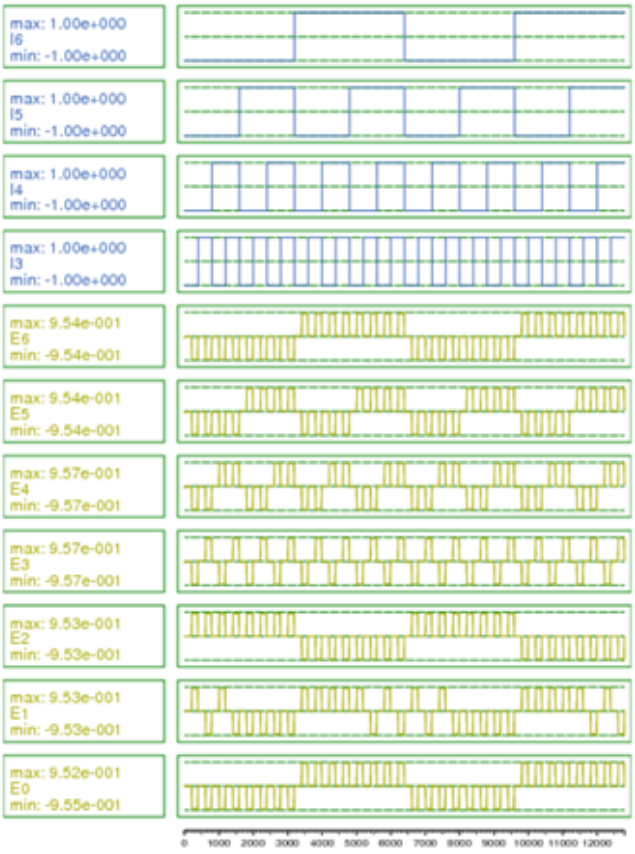

Fig. 7. Simulation results of the Hamming encoder

The proposed coplanar design has minimized cell count by 49.47% and 9.52% compared to [1] and [12] respectively. The proposed encoder's total area is reduced by 19.38% compared to HE in [1]. The proposed structure has minimized cell area by 49.18% and 8.82% compared to [1] and [12] respectively. The QCA cost functions are used to verify the designs. The area-delay cost (ADC) and energy-delay cost (EDC) metrics [4] are calculated. The smaller values are desirable. The ADC is a product of the total area and delay^2 [4] is computed for the encoder circuits. The proposed encoder has ADC 18.75% less than [1]. The average and total ED is reduced by 17.5% and 17.78% over the design in [1] and less than [12]. The EDC is calculated as the product of total area^2 and delay^2 [4]. The proposed design has 32.59% and 2.58% less EDC than the designs in [1] and [12] respectively.

6.2 Syndrome calculator and error detector

The proposed syndrome calculator circuit is analyzed w.r.t. various parameters such as area, latency, cost functions, and energy dissipation (ED). The simulated waveforms of the syndrome calculator are shown in Fig. 8. The output of three syndromes is calculated using Eqns. (8-10). The obtained results are tabulated in Tab. 4. The reference structure in [1] has been designed using a multilayer cross-over structure, which has the disadvantage of several cells and increased area. It is observed that the total cell count is reduced by 56.54% and the ADC is minimized by 11.1% compared to the design in [1].

The ED (total and average) values are tabulated in Tab. 4. The proposed decoder dissipates less energy compared to [1]. The average energy dissipation has been reduced by 18.8%. A similar reduction is seen in total energy dissipation. Hence, the proposed syndrome calculator is both area and energy-efficient compared.

Table 4. Performance analysis of syndrome calculators

QCA parameters	[1]	Proposed
Cell count	260	113
Total area (μm^2)	0.18	0.16
Cell area (μm^2)	0.084	0.037
Delay (Clock zones)	3	3
ADC	1.62	1.44
Average ED (meV)	9.63	7.82
Total ED (meV)	87.8	86
EDC	0.069	0.066

The proposed error detector is designed using a multilayer approach. The input test set applied to analyze the proposed error detector is listed in Tab. 2. The parameters of the proposed error detector are listed in Tab. 5. The error detector is realized using 189 cells and occupies an area of 0.24 μm^2. It has an average ED of 7.77 meV and a total ED of 85.5 meV.

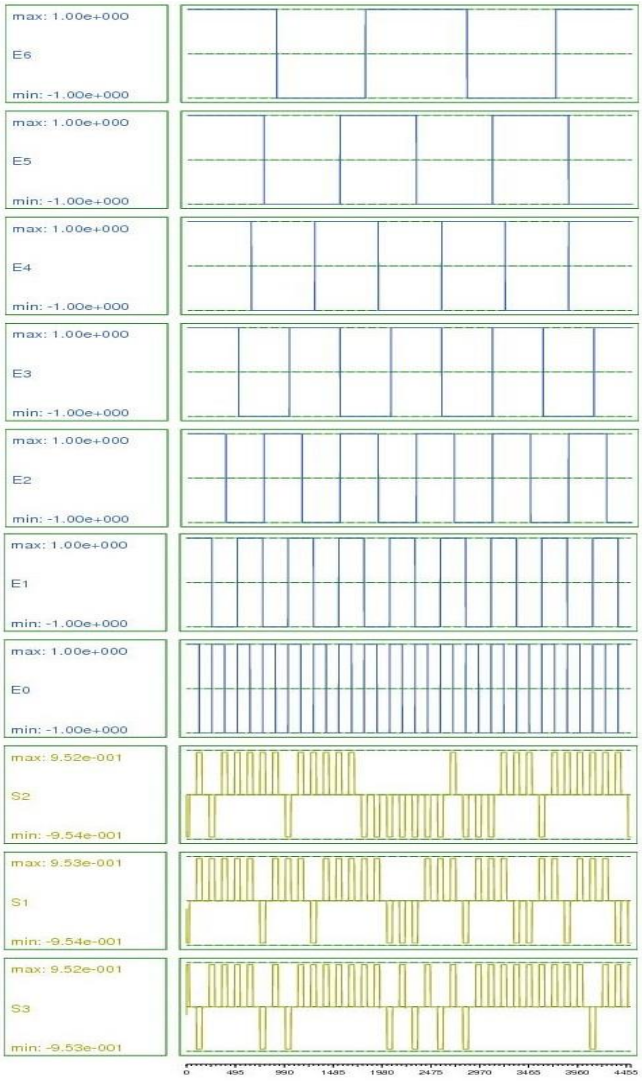

Fig. 8. Simulation results of the syndrome calculator

Table 5. Performance analysis of the proposed error detector

QCA parameters	Error detector
Cell count	189
Total area (μm^2)	0.24
Cell area (nm^2)	61,236
Delay (Clock zones)	4
ADC	3.84
Total ED (meV)	7.77
Average ED (meV)	85.5
EDC	0.117

7 Conclusion and future scopes

The work illustrates the implementation of QCA-based Hamming encoder and decoder circuits. The CAD tools QCADesiger2.0.3 and QCADesigner-E are used. The proposed Hamming encoder, syndrome calculator, and error detector require fewer QCA cells for implementation and also dissipate less energy. The proposed (7, 4) HE cell count has reduced by 49.47% and 8.82% when compared to designs in [1] and [12] respectively. The proposed syndrome calculator has reduced cell count by 56.54% and average energy dissipation by almost 19%. The proposed Hamming encoder and syndrome calculator in terms of various QCA cost functions (ADC and EDC) are also found to be more efficient compared to the design in [1]. Further, the proposed Hamming code components can be used to build a complete Hamming communication network. The same result can be obtained for various generator matrices by altering the connector lines of the circuit, without making significant structural changes. Hamming code can be further extended to design higher-order networks such as (15, 11) HCN without making any significant changes to the topology.

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