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EFFECT OF THE DC CONTROL ON RECOVERY FROM COMMUTATION FAILURES IN AN HVDC INVERTER FEEDING A WEAK AC NETWORK

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Recovery from commutation failures after inverter side faults can be problematic. This paper explores the effect of the DC control on recovery from commutation failures in an HVDC inverter, due to AC system fault in line commutated thyristor inverter connected to a weak AC network. The AC system fault is a single phase ground fault. MATLAB Simulink is used for the simulation studies.

K e y w o r d s: HVDC transmission, commutation failures, recovery, voltage dependent current order limits (VDCOL), short circuit ratio (SCR)

1 INTRODUCTION

AC system faults in the electrical proximity of the inverter station causing inverter AC busbar voltage reductions in any or all phases may cause commutation failures in some or all of the connected valve groups. During the period of commutation failures, usually the fault duration, the associated valve groups cannot deliver any power into the AC network. The energy loss to the AC system during the fault is unavoidable [1, 2].

The importance of commutation failures during system faults, and therefore also the importance of commutation failure probability for remote faults in low and very low SCR systems, depends on the sensitivity of the receiving AC system to the energy deficit during the failure and the converter behaviour during the subsequent recovery period. If the recovery period is not smoothly controlled, the effects on the AC system can be aggravated. After fault clearing, the DC would normally be required to recover as quickly as possible to minimize the energy loss and prevent transient instability of the AC system.

A CIGRÉ document released in 1992 [3] is valuable for understanding these AC-DC interactions. Their influence on station design and performance is assessed with reference to the AC-DC system strength, a relative term which is generally expressed by the short-circuit ratio (SCR), *ie*, the ratio of the AC-system short-circuit capacity to DC-link power [4–6]:

$$SCR = \frac{S}{P_{dc}} \,. \tag{1}$$

Here S is the AC system three-phase symmetrical short-circuit level in megavolt-amperes (MVA) at the converter terminal AC bus with 1.0 pu AC terminal voltage, and P_{dc} is the rated DC terminal power in megawatts (MW). The following SCR values can be used to classify AC systems [7]:

a) a strong AC system is categorized by $SCR \geq 3$,
b) a weak AC system is categorized by $2 \leq SCR < 3$,
c) a very weak AC system is categorized by $SCR < 2$.

The most common failure type in an AC transmission network is a single-phase short circuit to earth, and we have therefore investigated only this type of fault.

2 DESCRIPTION OF THE EVENT

The basic module of an HVDC converter is the three-phase, full-wave bridge circuit shown in Fig. 1, where V_a, V_b and V_c represent the AC side phase-voltage. X_C is the commutating reactance of the external circuit. I_d represents the DC side current. The circuit is known as Graetz bridge.

Figure 2 shows the basic equivalent circuit of a line commutated converter for which the process of commutation between valve 1 and valve 3 is illustrated. Under normal circumstances, the voltage across the valve being turned off has to remain negative for a certain period after extinction of its current (denoted by the extinction angle γ in Fig. 3) so that it becomes capable of blocking the forward voltage. Should the valve voltage become positive prematurely, the valve may turn on even without a firing pulse, resulting in a failure of the commutation process.

Figure 3 illustrates the angle relationships and angle definition for an inverter. During the commutation, the two valves involved in the commutation (valve 1 and valve 3) conduct simultaneously and the phase-voltages in phase a and phase b will be short circuited through the two commutation reactances, X_C. Eventually, the current will be transferred from valve 1 to valve 3 and the

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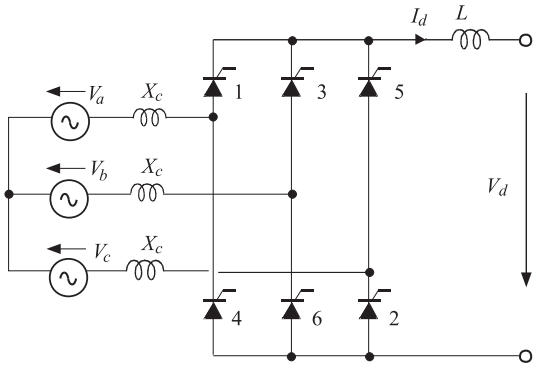


Fig. 1. Equivalent circuit for three-phase full-wave bridge converter

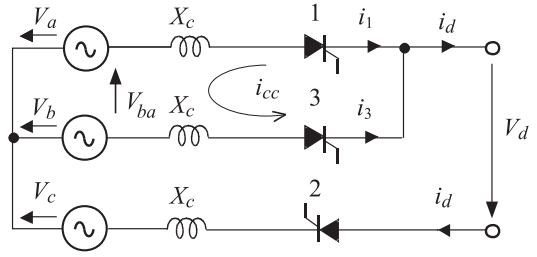


Fig. 2. Basic equivalent circuit during the commutation

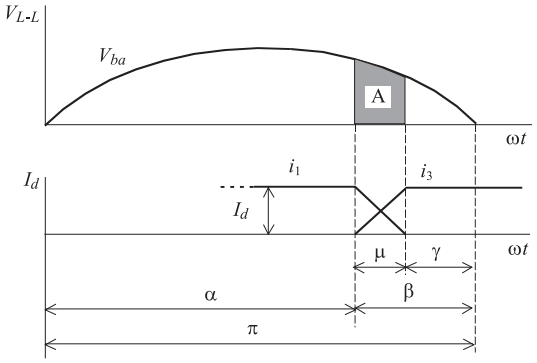


Fig. 3. Commutation process between valve 1 and valve 3

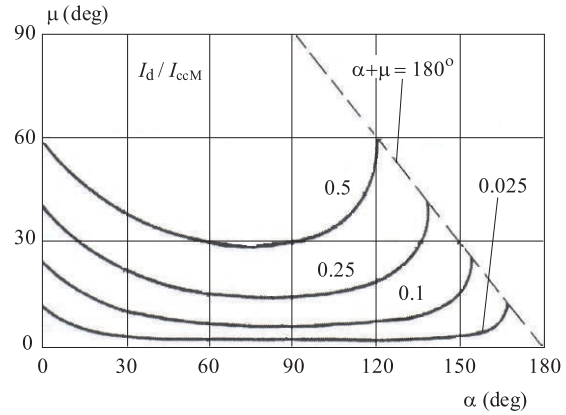


Fig. 4. Variation of the overlap angle μ as a function of delay angle α

commutation will be finished. The time this takes is measured by the commutation interval angle, or overlap angle, that is denoted μ. The volt-time area A, which is shown in Fig. 3, is required for the commutation.

During the interval μ, the DC current is transferred from valve 1 to valve 3. At the beginning of the interval, $\omega t = \alpha$ and $i_1 = I_d$ and $i_3 = 0$. At the end of the interval, $\omega t = \alpha + \mu$, $i_1 = 0$ and $i_3 = I_d$. From the circuit of Fig. 2 we can write

$$V_b - V_a = \frac{X_C}{\omega}\frac{\mathrm{d}i_3}{\mathrm{d}t} - \frac{X_C}{\omega}\frac{\mathrm{d}i_1}{\mathrm{d}t} = L_C\frac{\mathrm{d}i_3}{\mathrm{d}t} - L_C\frac{\mathrm{d}i_1}{\mathrm{d}t}\,, \quad (2)$$

where $\frac{X_C}{\omega} = L_C$ is the AC inductance.

The total DC current I_d is shifted from valve 1 to valve 3. At every instant

$$i_1 + i_3 = I_d \quad (3)$$

$$\frac{\mathrm{d}i_1}{\mathrm{d}t} + \frac{\mathrm{d}i_3}{\mathrm{d}t} = \frac{\mathrm{d}I_d}{\mathrm{d}t} = 0\,, \quad (4)$$

$$\frac{\mathrm{d}i_1}{\mathrm{d}t} = -\frac{\mathrm{d}i_3}{\mathrm{d}t}\,. \quad (5)$$

The AC voltage can be represented by an ideal sinusoidal source:

$$V_b - V_a = \sqrt{3}V_m \sin(\omega t)\,. \quad (6)$$

Inserting eq (5) and (6) into (2) yields

$$\sqrt{3}V_m \sin(\omega t) = 2L_C\frac{\mathrm{d}i_3}{\mathrm{d}t}\,. \quad (7)$$

Integrating equation (7) over the duration of the commutation gives

$$i_3 = \frac{\sqrt{3}V_m}{2\omega Lc}[\cos\alpha - \cos(\omega t)] \quad (8)$$

and substituting the final condition, *ie* $i_3 = I_d$ at $\omega t = \alpha + \mu$ yields

$$I_d\frac{\sqrt{3}V_m}{2\omega Lc}[\cos\alpha - \cos(\alpha + \mu)]\,. \quad (9)$$

From equations (8) and (9) we can write

$$i_3 = \frac{I_d(\cos\alpha - \cos\omega t)}{\cos\alpha - \cos(\alpha + \mu)}\,. \quad (10)$$

When a converter bridge is operating as an inverter, a valve will turn off when its forward current falls to zero and the voltage across the valve remains negative. The period for which the valve stays negatively biased is the extinction angle γ, the duration beyond which the valve then becomes forward biased. Without a firing pulse, the valve will ideally stay non-conductive or blocked. The angle of advance β is related in degrees to the angle of delay α by

$$\beta = 180^\circ - \alpha \quad (11)$$

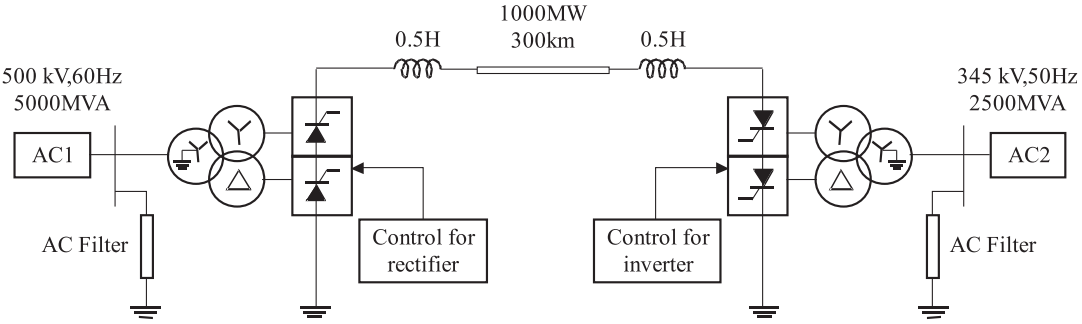


Fig. 5. HVDC system model

and

$$\alpha = 180^\circ - (\gamma + \mu)\,. \tag{12}$$

The μ commutation or overlap angle can be also calculated. Its theoretical value depends on α, the DC current I_d and the commutation reactance X_C:

$$\mu = ar\cos\Big[\cos(\alpha) - \frac{X_C I_d\sqrt{2}}{V_{LL}}\Big] - \alpha \tag{13}$$

V_{LL} is the line-to-line rms commutating voltage that depends on the AC system voltage and the transformer ratio. The DC inverter therefore requires a period of negative bias or minimum extinction angle γ (15° for 50 Hz, or 18° for 60 Hz) for forward blocking to be successful. If forward blocking fails and conduction is initiated without a firing pulse, commutation failure occurs. This also results in an immediate failure to maintain current in the succeeding converter arm as the DC line current returns to the valve which was previously conducting and which has failed to sustain forward blocking. Commutation failures at a converter bridge operating as an inverter are mainly caused by voltage dips due to AC system faults. Voltage dips may cause both voltage magnitude reduction and phase-angle shift. Voltage dips may affect the commutation in three ways [4, 8, 9]:

1. Increased DC current
2. Voltage magnitude reduction of the AC side
3. Phase angle shift

Figure 4 [10] illustrates the dependence of the overlap angle μ on to the delay angle α with the parameter (I_d/I_{ccM}), where I_{ccM} is the peak value of the current of short-circuit $(i_{cc} = i_3)$ during the commutation interval (μ). From equation (8) it follows

$$I_{ccM} = \frac{\sqrt{3}V_m}{2\omega Lc} \tag{14}$$

and from equation (9) we can write:

$$\cos(\alpha + \mu) = \cos\alpha - \frac{I_d}{I_{ccM}}. \tag{15}$$

From equation (9) we show that the overlap angle μ depends on the delay angle α and on the direct current I_d to be commutated. The overlap angle μ increases with (I_d/I_{ccM}), it becomes maximum for $\alpha = 0$, and this corresponds to the operation of a pure rectifier. If α increases, the overlap angle μ decreases to reach a minimal value. For $\alpha > 90^\circ$, μ increases again, however, a limit of operation exists by the fact that $\alpha + \mu$ must be lower than 180°.

3 SYSTEM UNDER STUDY

A 1000 MW (500 kV, 2 kA) DC interconnection is used to transmit power from a 500 kV, 5000 MVA, 60 Hz network (AC system 1, having a SCR of 5) to 345 kV, 2500 MVA, 50 Hz network (AC system 2, having a SCR of 2.5). The AC networks are represented by damped L-R equivalents with an angle of 80 degrees at fundamental frequency (60 Hz or 50 Hz) and at the third harmonic. The rectifier and the inverter are 12-pulse converters using two universal bridge blocks connected in series. The converters are interconnected though a 300 km distributed parameter line and 0.5 H smoothing reactor. The converter transformer $(Yg/Y/\Delta)$ is modelled with a three-phase transformer (three-windings). The tap position is rather at a fixed position determined by a multiplication factor applied to the primary nominal voltage of the converter transformers (0.9 on rectifier side; 0.96 on inverter side). The configuration of the system is given in Fig. 5.

3.1 The AC systems

The AC networks, both at the rectifier and inverter end, are modelled by AC sources separated from their respective commutating buses by system impedances. The impedances are represented as L-R/L networks having the same damping at the fundamental and the third harmonic frequencies. The impedance angles of the receiving end and the sending end systems are selected to be 80 degrees. This is likely to be more representative in the case of resonance at low frequencies [11].

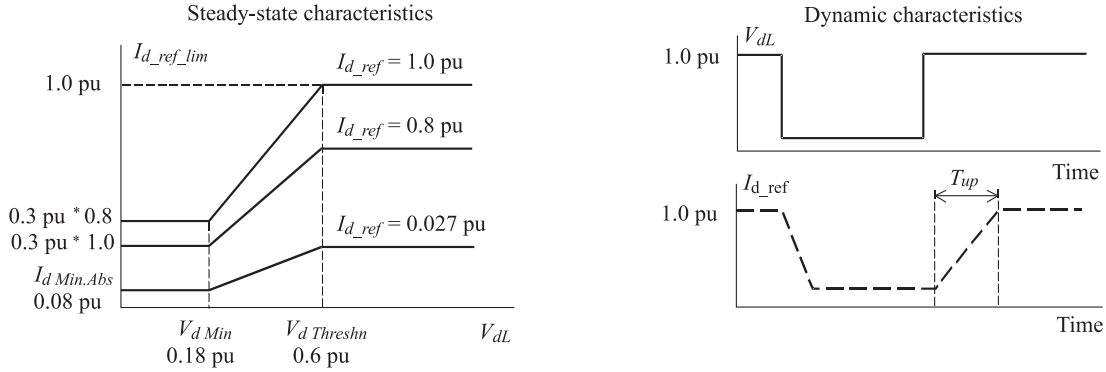


Fig. 6. The VDCOL Characteristics

3.2 DC system

The DC system is composed of smoothing reactors and a DC transmission line modelled with distributed parameter line with lumped losses. This model is based on the Bergeron's travelling wave method used by the Electromagnetic Transient Program (EMTP).

3.3 The converter transformers

The 1200 MVA converter transformer is modelled with three-phase transformer (Three-Windings). The parameters adopted (based on AC rated conditions) are considered as typical for transformers found in HVDC installation such as leakage: $X_C = 0.24$ p.u.

3.4 AC filters and capacitor banks

On AC side of 12-pulse HVDC converter, current harmonics of the order of 11, 13, 25 and higher are generated. Filters are installed in order to limit the amount of harmonics to the level required by the network. In the conversion process, the converter consumes reactive power, which is compensated in part by the filter banks and the rest by capacitor banks of 600 Mvar on each side.

3.5 Control systems

The rectifier and the inverter control both have a voltage and a current regulator operating in parallel calculating firing angle αv and αi. Both regulators are of the proportional and integral type (PI). In normal operation, the rectifier controls the current at the Id_ref reference value whereas the inverter controls the voltage at the Vd_ref reference value. The I_margin and Vd_margin parameters are respectively 0.1 p.u. and 0.05 p.u.

3.5.1 The VDCOL function

An important control function is implemented to change the reference current according to the value of the DC voltage. This control named Voltage Dependent Current Order Limits (VDCOL) automatically reduces the reference current (Id_ref) set point when VdL (Vd line) decreases (as for example, during a DC line fault or a severe AC fault). Reducing the Id reference currents also reduces the reactive power demand on AC network, helping to recover from fault [7 ,12]. The VDCOL parameters of the discrete 12-Pulse HVDC control are presented in Fig. 6.

The Id_ref value starts to decrease when the Vd line voltage falls bellow a threshold value VdThresh (0.6 p.u.). The actual reference current is named Id_ref-lim. IdMinAbs is the absolute minimum Id_ref set at 0.08 p.u. When the DC line voltage falls bellow the VdThresh value, the VDCOL reduces instantaneously Id_ref. However, when the DC voltage recovers, VDCOL limits the Id_ref rise time with a time constant defined by parameter (Tup).

4 SIMULATION RESULTS

For two different values of Tup (Id_ref rise time), a single phase-to-ground fault at inverter side is examined in this paper. For each of the transient case considered above, plots of rectifier and inverter DC current, DC voltage, and firing angle, are given. Also the inverter valves current of two Graetz bridges connected in series (The bridges are connected to the AC system by means of converter transformers, one of Y-Y winding structure and another Y-Δ winding structure, as shown in Fig. 5).

4.1 Single phase-to-ground fault at inverter ($Tup = 10$ **ms**)

A single phase-to-ground fault was applied to the A-phase of the inverter bus, and the duration of the fault was 5 cycles, and the Id_ref rise time $Tup = 10$ ms. Results of this study are shown in Figs. 7 and 8.

When this fault is applied at $t = 0.6$ s, due to a reduction in AC voltage of the inverter bus, the inverter DC voltage decreases. The DC current therefore shoots up. The rectifier current controller attempts to reduce

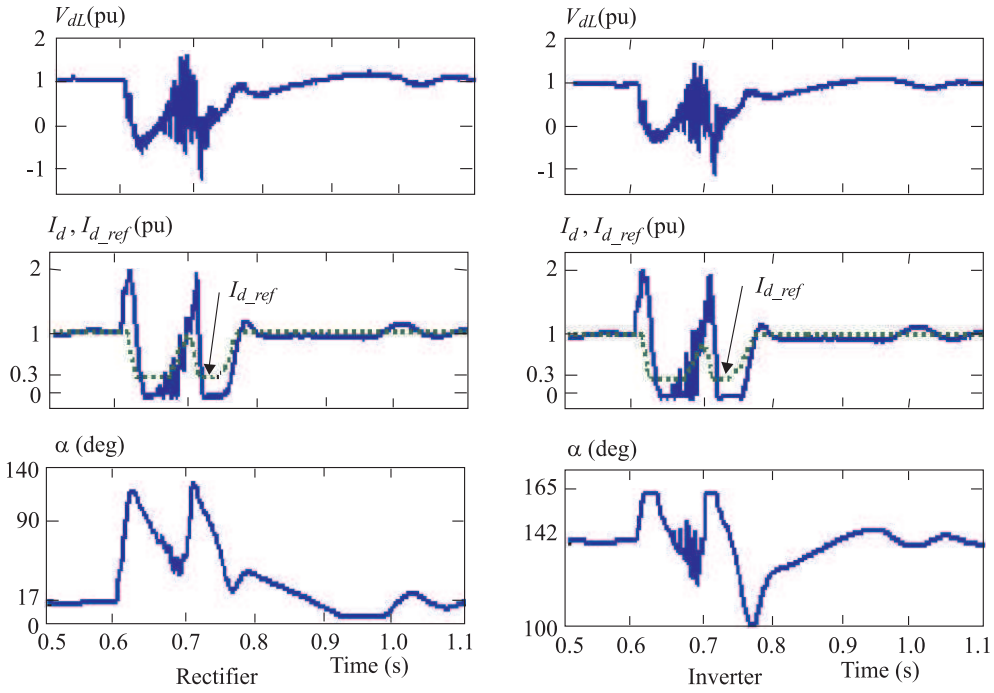


Fig. 7. Single phase-to-ground fault at inverter ($Tup = 10$ ms)

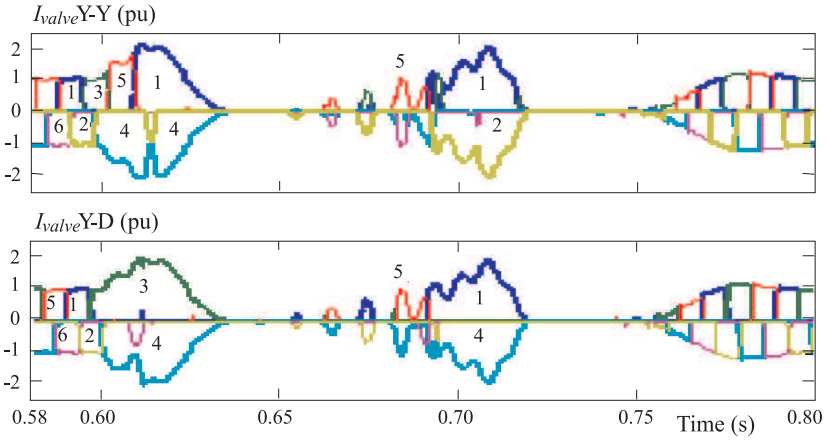


Fig. 8. Inverter valves current during the fault ($Tup = 10$ ms)

the current by increasing its firing angle and the rectifier therefore goes into the inverter region. The DC current decreases to a low average value as determined by VDCOL (0.3 p.u.).

From Fig. 8, the inverter valves current plots indicate a number of commutation failures of the corresponding valve groups, which translates by an increase in the DC current because the valves 1 and 4 in the (YY) bridge are conducting current at the same time, and that the (YY) Graetz bridge is short-circuited on the DC side.

When the fault is cleared at $t = 0.7$ s, another commutation failure will accrue during the recovery in the second bridge $(Y\Delta)$. Since the DC voltage is zero during a period following the commutation failure, no active power will be transmitted during this time. The system recovers in approximately 0.4 s after fault clearing.

4.2 Single phase-to-ground fault at inverter ($Tup = 80$ ms)

For the same fault, and a $Tup = 80$ ms, the waveforms resulting are displayed in Figs. 9 and 10. When this fault is applied at $t = 0.6$ s, commutation failure will accrue, and we can show that the valves 1 and 4 are conducting current at the same time, and that the (YY) Graetz bridge is short-circuited on the DC side. The DC current therefore shoots up; the VDCOL operates and reduces the reference current to 0.3 p.u. When the fault is cleared at $t = 0.7$ s, the DC voltage starts to increase, following commutations take place in a normal way, and normal operation is resumed. The system recovers in approximately 0.3 s after fault clearing.

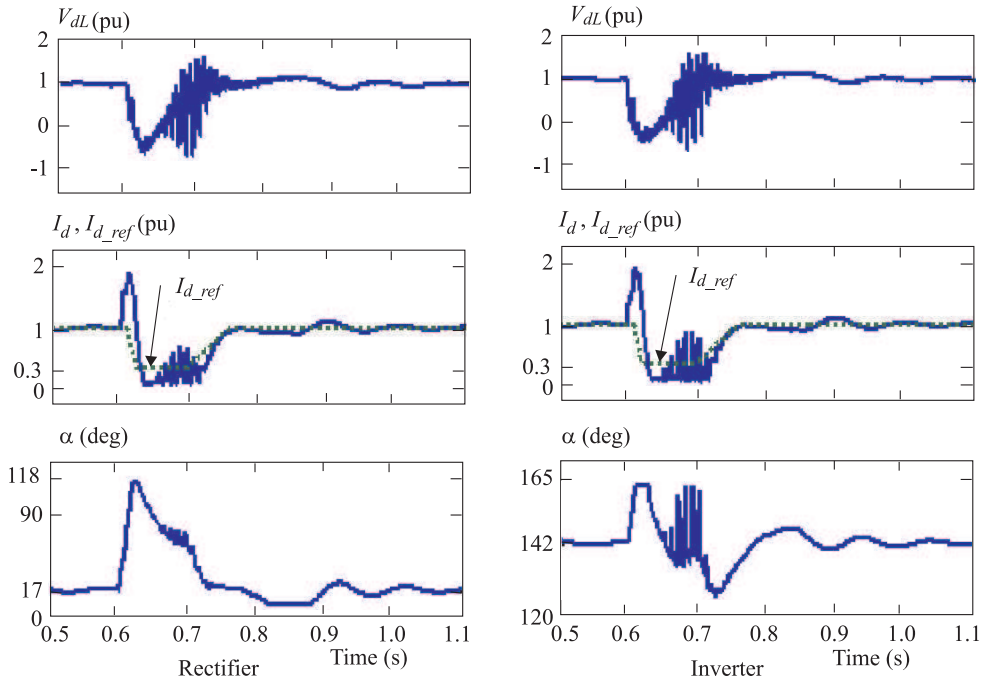


Fig. 9. Single phase-to-ground fault at inverter ($Tup = 80$ ms)

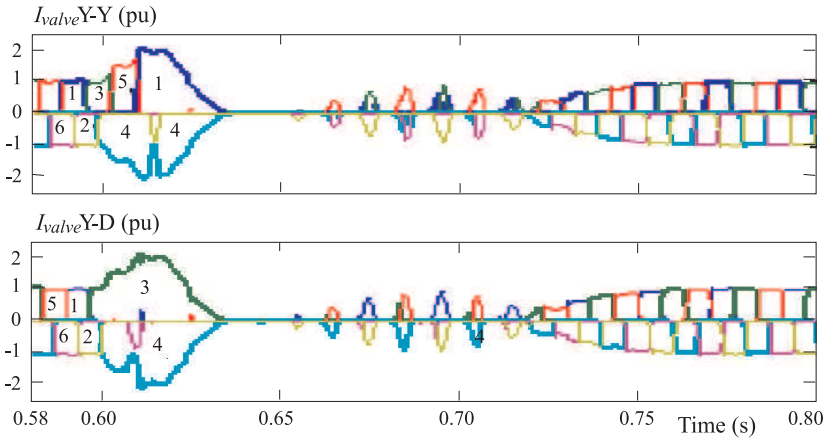


Fig. 10. Inverter valves current during the fault ($Tup = 80$ ms)

4.3 Discussion of the results

From the results given above results it is concluded that:

1. VDCOL function has an important role in determining the DC system recovery from commutation failures.
2. Following fault clearing, the VDCOL function current limit may be delayed and ramped so as to maximize the recovery rate while avoiding subsequent commutation failures.

5 CONCLUSION

To obtain good DC system recovery from commutation failure, control strategy alternatives can include delay or slow ramp recovery, reduced current level, and reduced power level at recovery (especially when the end system is disconnected due to some faults).

A voltage-dependent current order limit (VDCOL) function has an important role in determining the DC system recovery from faults, particularly from faults in a weak receiving-end AC system. The action of this function is to limit the current order as a function of the reduction in DC line voltage.

In the case of severe single line to ground faults, the VDCOL may also help to recover normal commutation and thus some power transfer can resume during the fault. Following fault clearing, the removal of the VDCOL function current limit may be delayed and ramped so as to maximize the recovery rate while avoiding subsequent commutation failures.

Appendix. Data for the system model

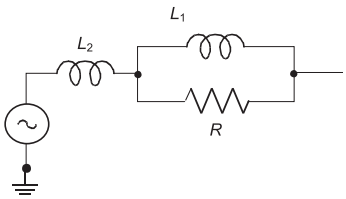
Firing angle: $\alpha = 17°$ (for the rectifier); $\alpha = 142°$ (for the inverter).

Rectifier end: The rectifier end AC system 1 representing a strong system ($SCR = 5$), consists of one source with an equivalent impedance of: $R = 26.07\,\Omega$, $L_1 = 48.86$ mH, $L_2 = 98.03$ mH.

Inverter end: The inverter end AC system 2 representing a weak system ($SCR = 2.5$), consists of one source with an equivalent impedance of: $R = 24.82\,\Omega$, $L_1 = 55.84$ mH, $L_2 = 112$ mH.

DC line parameters: $Rdc = 0.015\,\Omega$/km, $L = 0.792$ mH/km, $C = 14.4$ nF/km.

Details of AC system representation



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