Journal of ELECTRICAL ENGINEERING, VOL. 60, NO. 4, 2009, 185–191

INDUCTIVE CLAMPING CIRCUIT FOR DC LINK VOLTAGE BALANCING OF FIVE–LEVEL NPC–VSI

Rédha Chibani — El Madjid Berkouk — Mohamed S. Boucherit *

A new control solution to compensate the unbalanced DC voltages for the five-level Neutral Point Clamped Voltage Source Inverter (NPC-VSI) is presented. It provides a fast and flexible control of the inverter capacitor voltages. The inverter capacitor voltage control is completely independent from the load control, leading to a simpler implementation.

K e y w o r d s: multilevel inverter, neutral point clamped, voltage source inverter, sliding mode, equalizing problem, clamping bridge

1 INTRODUCTION

One important problem associated with the NPC three-level inverter is its Neutral Point (NP) variation [1] under certain conditions, the DC link NP potential can significantly fluctuate or continuously drift to unacceptable levels. The causes of NP potential drift can be non uniform switching device or DC link capacitor characteristics or fluctuation due to the irregular and unpredictable charging and discharging in each capacitor [2–4]. The voltage across the capacitor may grow or decay so that the NP voltage fails to keep the half of the DC link voltage. Therefore, an excessive high voltage may be applied to the switching devices of DC link capacitors and this affects the converter performance due to the generation of uncharacteristic harmonics and the presence of overvoltages across the semiconductor switches.

Therefore, the choice of appropriate modulation techniques and the development of advanced neutral point potential control techniques is necessary to overcome the NP potential problems. Some solutions have been proposed, which are based on redundant switching configurations [1, 5–12] or on the addition of zero-sequence voltage components to the output voltage [6]. However, all these methods seem to be not always useful in no-load or low-load operations, when the supplied current tends to zero. In real systems, no-load conditions determine almost always the loss of DC-link capacitors voltages balance, owing to converter non ideality. Unfortunately, these methods modify the output voltage waveform. As the number of inverter-levels increases, the problem of capacitor balancing becomes more complex and the solution very drastic.

The unbalance DC voltage problem can also be solved by separate DC sources [3] or by adding electronic circuitry. In [13] and [14], clamping bridges based on transistors and resistors are proposed as a solution to this problem. Disadvantages of this method are the requirement for large power dissipating resistors, high current switches, and thermal management requirements. This method is best suited for systems that are charged often with small currents.

This paper deals with a new clamping bridge for the DC capacitor voltage equalisation has been proposed to compensate DC-link capacitors voltages fluctuations in a NPC VSI that permits to achieve a correct capacitors voltages sharing, when conventional balancing methods fail.

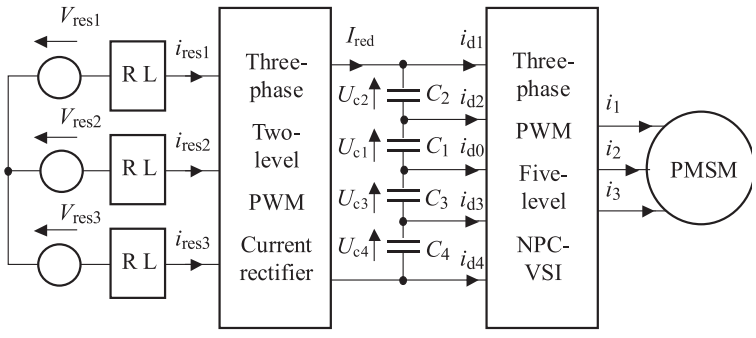

Fig. 1. Structure of the cascade proposed

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ISSN 1335-3632

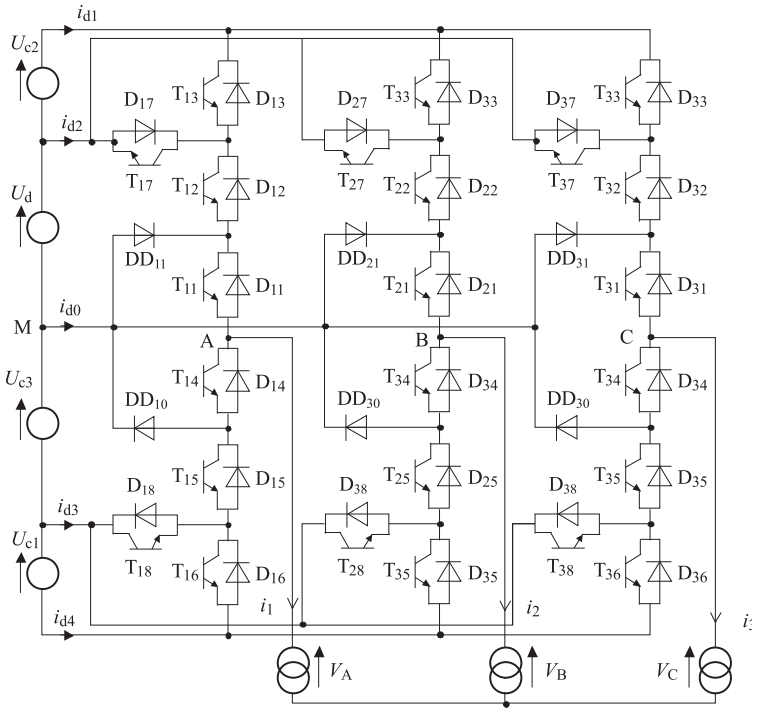

Fig. 2. General structure of the three phases five-level NPC VSI

In order to stabilize these DC voltages, we propose in this paper to study the cascade constituted by three phases two-level PWM rectifier-clamping bridge — five-level NPC VSI — Permanent Magnet Synchronous Machine. In the first part, the authors present a topology of five-level NPC, then they propose a model of this converter and the PWM strategy to control it. In the second part, we study the two-level PWM rectifier controlled by sliding mode. In the last part of this paper, the authors study the stability problem of the input DC voltages of the inverter. To remedy to this problem, a new control solution to compensate the unbalanced DC voltages for the five-level Neutral Point Clamped Voltage Source Inverter is presented. It provides a fast and flexible control of the inverter capacitor voltages. The results obtained are full of promise to use the inverter in high voltage and great power applications.

2 FIVE–LEVEL CASCADE

The global scheme of the cascade is given on Fig. 1.

2.1 Five-level NPC-VSI modelling

The general structure of the three phases five-level NPC voltage source inverter is shown on Fig. 2. It is composed by 24 pairs transistor-diode.

Every leg of this inverter includes eight pairs, four on the upper half leg and four on the lower one.

The optimal control law is given below

$$\begin{aligned} B_{k1} &= \overline{B_{k5}}\,, \\ B_{k2} &= \overline{B_{k4}}\,, \\ B_{k3} &= \overline{B_{k6}}\,, \\ B_{k7} &= B_{k1}B_{k2}\overline{B_{k3}}\,, \\ B_{k8} &= B_{k4}B_{k5}\overline{B_{k6}}\,. \end{aligned} \tag{1}$$

B_{ks} is the control signal of TD_{ks}. TD_{ks} represent every pair transistor-diode by one bi-directional switch.

The voltage of the three phases A, B, C relatively to the middle point M and using the half leg connection functions F^b_{kM} are given by V_{XM} with $x =$ point A, B or C.

$$\begin{aligned} V_{kM} = \big[F^b_{k1}(U_{c1}+U_{c2}) + F_{k7}(U_{c1})\big] \\ - \big[F^b_{k0}(U_{c3}+U_{c4}) + F_{k8}(U_{c3})\big]. \end{aligned} \tag{2}$$

The input currents of the three phases five-level inverter using the load currents are given by the following relations

$$\begin{aligned} i_{d1} &= F^b_{11}i_1 + F^b_{21}i_2 + F^b_{31}i_3\,, \\ i_{d2} &= F^b_{11}{}'i_1 + F^b_{21}{}'i_2 + F^b_{31}{}'i_3\,, \\ i_{d3} &= F^b_{10}{}'i_1 + F^b_{20}{}'i_2 + F^b_{30}{}'i_3\,, \\ i_{d4} &= F^b_{10}i_1 + F^b_{20}i_2 + F^b_{30}i_3\,, \\ i_{d0} &= i_1 + i_2 + i_3 - i_{d1} - i_{d2} - i_{d3} - i_{d4}\,. \end{aligned} \tag{3}$$

2.2 Control strategy of the inverter

This strategy uses four bipolar carriers (U_{p1}, U_{p2}, U_{p3}, U_{p4}). It is characterized by two parameters $\boldsymbol{m}$ the

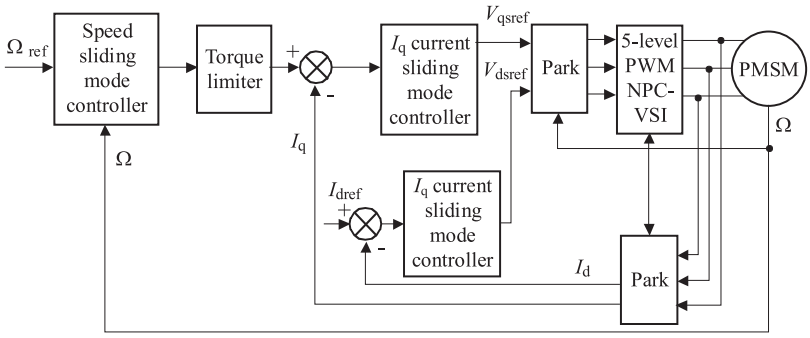

Fig. 3. Permanent Magnet Synchronous Machine speed control scheme based on sliding mode

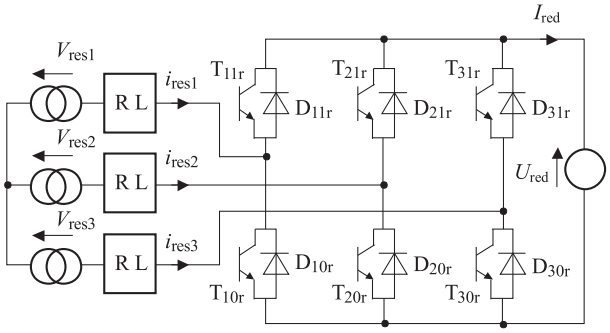

Fig. 4. Structure of the two-level PWM current rectifier

index modulation and $\boldsymbol{r}$ the modulation rate. The algorithm of this strategy can be summarized as follows Step 1: Determination of the intermediate voltages

$$\begin{aligned}
&\text{if } V_{\text{refk}} > U_{p1} \text{ then } V_{kM1} = +U_c\,,\\
&\text{if } V_{\text{refk}} < U_{p1} \text{ then } V_{kM1} = 0\,,\\
&\text{if } V_{\text{refk}} > U_{p2} \text{ then } V_{kM2} = +2U_c\,,\\
&\text{if } V_{\text{refk}} < U_{p2} \text{ then } V_{kM2} = +U_c\,,\\
&\text{if } V_{\text{refk}} > U_{p3} \text{ then } V_{kM3} = 0\,,\\
&\text{if } V_{\text{refk}} < U_{p3} \text{ then } V_{kM3} = -U_c\,,\\
&\text{if } V_{\text{refk}} > U_{p4} \text{ then } V_{kM4} = -U_c\,,\\
&\text{if } V_{\text{refk}} < U_{p4} \text{ then } V_{kM4} = -2U_c\,.
\end{aligned} \tag{4}$$

Step 2: Determination of the output voltage

$$V_{kM} = V_{kM1} + V_{kM2} + V_{kM3} + V_{kM4}\,. \tag{5}$$

3 PERMANENT MAGNET SYNCHRONOUS MACHINE MODELLING

The model of PMSM without damper winding has been developed on rotor reference frame as follows [13–15]

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} R_s + L_d s & -\omega L_q \\ \omega L_d & R_s + L_q s \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega K_t \end{bmatrix}. \tag{6}$$

The electric torque is stated as

$$C_{em} = K_t i_q + (L_d - L_q) i_d i_q\,, \tag{7}$$

$$J(s\omega) = C_{em} - C_r - K\omega\,. \tag{8}$$

Control of PM motors is performed using field oriented control for the operation of synchronous motor as a DC motor. For the PM synchronous machine used, we develop the algorithm $i_d = 0$ (Fig. 3). When the d axis current is equal to zero, the block diagram of the q axis becomes similar to that of a DC machine and the speed can be controlled by using a sliding mode controller which generates the q axis voltage. We use a current regulator for the d and q axes [13, 15].

4 TWO–LEVEL PWM CURRENT RECTIFIER

The general structure of the two-level PWM current rectifier is given on the Fig. 4.

4.1 Voltage feedback control

For each phase k ($k = 1$, 2 or 3) of the three phases network feeding the rectifier considered can be represented by a R, L circuit. V_{resk} is the voltage of one phase k of the three phases network and V_k is the voltage of the leg k of the rectifier.

The voltage loop imposes the effective value of the reference current of the network corresponding to the power exchanged between the network and the continue load (Fig. 5).

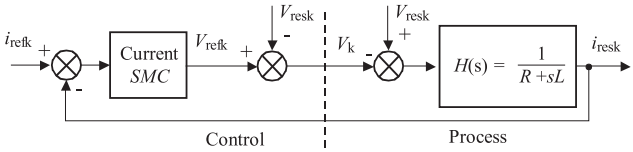

Fig. 5. Control algorithm of the output DC voltage of the two-level PWM current rectifier

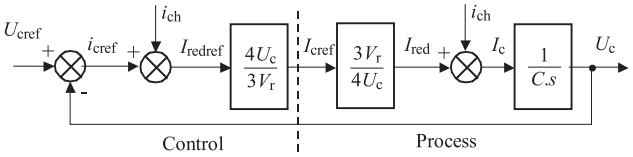

Fig. 6. Control algorithm of the network current i_{resk} of the two-level PWM rectifier.

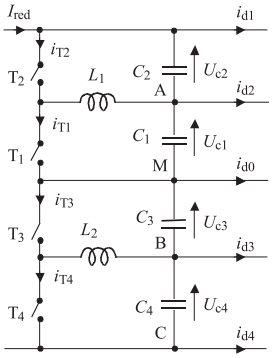

Fig. 7. Structure of the clamping bridge

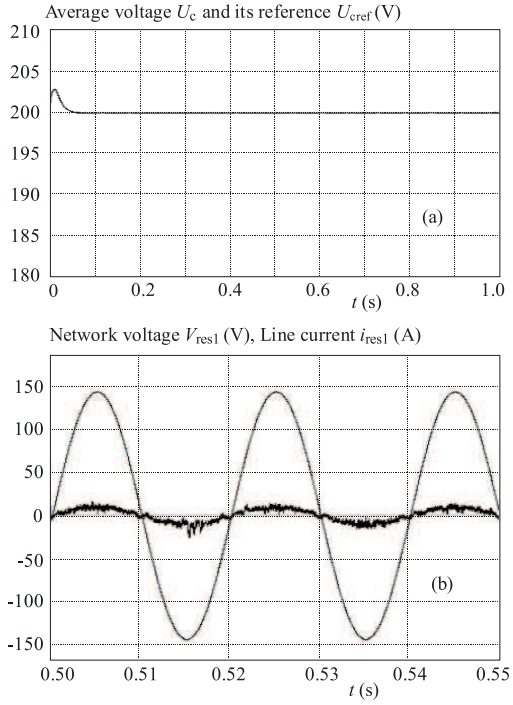

Fig. 8. Output DC voltage, network voltage and current of the two-level PWM current rectifier: (a) – voltage U_c and its reference, (b) – V_{res1}, i_{res1} and its reference

We want to regulate the voltage U_c of the rectifier. For that we choose for sliding surface

$$S = U_c - U_{\mathrm{cref}}\,. \tag{9}$$

Its derivative is

$$\dot{S} = \dot{U}_c\,, \tag{10}$$

$$\dot{U}_c = \frac{I_{\mathrm{red}} - i_{ch}}{C}\,, \tag{11}$$

$$\dot{U}_c = \frac{1}{C}\Big(\frac{3V_r I_e}{4U_c} - i_{ch}\Big). \tag{12}$$

The condition $s\dot{s} < 0$ insures the attractibility of the trajectory towards the sliding surface. For that, we choose

$$\dot{s} = -K_1\,\mathrm{sign}(S) - k_2 S\,. \tag{13}$$

The output of the sliding mode controller gave

$$I_e = -\frac{4U_c}{3V_r}\big[C\big(k_1\,\mathrm{sign}(U_c - U_{\mathrm{cref}}) + k_2(U_c - U_{\mathrm{cref}})\big) - i_{ch}\big]\,. \tag{14}$$

4.2 Current feedback control

We control the network current of the phase 1 and 2 by a Lyapunov function regulator. The algorithm of this current loop is given on the Fig. 6. In this scheme, the transfer function $H(p)$ is expressed as follows

$$H(s) = \frac{I_{\mathrm{resk}}}{V} = \frac{1}{R + sL}\,. \tag{15}$$

From the network equations we have

$$\begin{aligned} V_{\mathrm{res1}} - V_A &= RI_{\mathrm{res1}} + L\dot{I}_{\mathrm{res1}}\,,\\ V_{\mathrm{res2}} - V_B &= RI_{\mathrm{res2}} + L\dot{I}_{\mathrm{res2}}\,, \end{aligned} \tag{16}$$

$$\begin{aligned} V_A &= N_{g1}U_c\,,\\ V_B &= N_{g2}U_c\,. \end{aligned} \tag{17}$$

We choose the following sliding surfaces

$$\begin{aligned} S_1 &= I_{\mathrm{res1}} - I_{\mathrm{ref1}}\,,\\ S_2 &= I_{\mathrm{res2}} - I_{\mathrm{ref2}}\,. \end{aligned} \tag{18}$$

To satisfy the attractability condition, we choose

$$\begin{aligned} \dot{S}_1 &= -k_{11}\,\mathrm{sign}(S_1) - k_{21}S_1\,,\\ \dot{S}_2 &= -k_{12}\,\mathrm{sign}(S_2) - k_{22}S_2\,,\\ \dot{S}_k &= \dot{I}_{\mathrm{resk}} - \sqrt{2}\omega I_e\cos\Big(\omega t - \frac{2(k-1)\pi}{3}\Big) \end{aligned} \tag{19}$$

with $k = 1, 2, 3$.
We obtain

$$\begin{aligned} N_{g1} &= \frac{1}{4U_c}\big[V_{\mathrm{res1}} - RI_{\mathrm{res1}} + Lk_{11}\,\mathrm{sign}(I_{\mathrm{res1}} - I_{\mathrm{ref1}})\\ &\quad + Lk_{21}(I_{\mathrm{res1}} - I_{\mathrm{ref1}}) - \sqrt{2}L\omega I_e\cos(\omega t)\big],\\ N_{g2} &= \frac{1}{4U_c}\big[V_{\mathrm{res2}} - RI_{\mathrm{res2}} + Lk_{12}\,\mathrm{sign}(I_{\mathrm{res2}} - I_{\mathrm{ref2}})\\ &\quad + Lk_{22}(I_{\mathrm{res2}} - I_{\mathrm{ref2}}) - \sqrt{2}L\omega I_e\cos(\omega t)\big], \end{aligned} \tag{20}$$

5 CLAMPING BRIDGE

In order to remedy to the unbalance problem, we suggest a solution which consists in establish a bridge balancing between the rectifier and the intermediate filter (Fig. 7). The aim of this use is to limit and stabilise variations of the input DC voltage of the inverter.

A cell equalization scheme for capacitors has been proposed to equalize input DC voltages. The capacitor voltage equalization clamping bridge scheme has many advantages such as higher equalization efficiency and a modular design approach.

Capacitor voltage equalization control should be implemented to restrict the charge-discharge current to the allowable cell limitations in the capacitor string.

The balancing algorithms search to efficiently remove energy from a strong capacitor and transfer that energy into a weak one until the capacitor voltage is equalized across all capacitors.

Every switch T_x $(x = 1, 2, 3, 4)$ represents a pair transistor-diode.

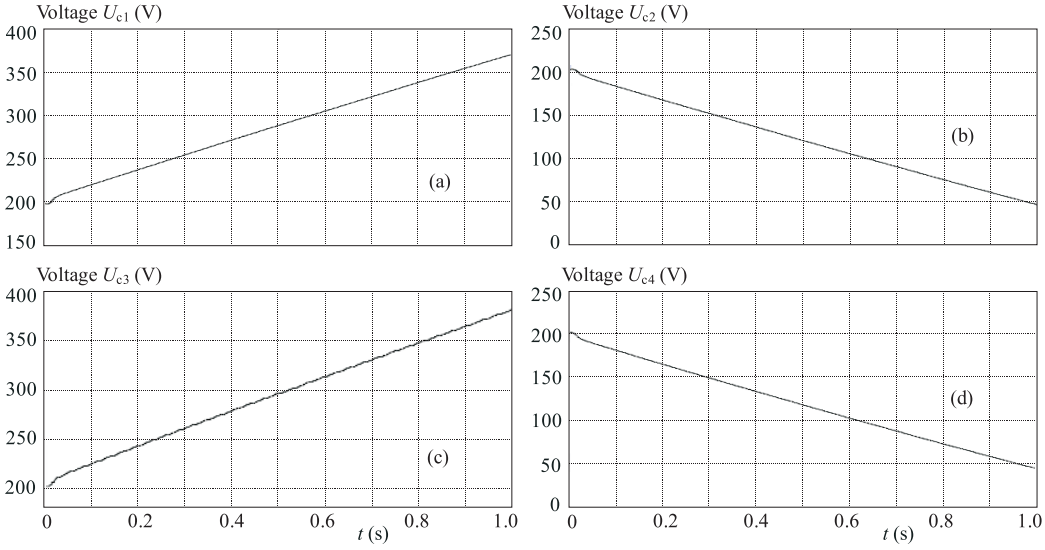

Fig. 9. DC input voltages of the five-level NPC-VSI without using the clamping bridge

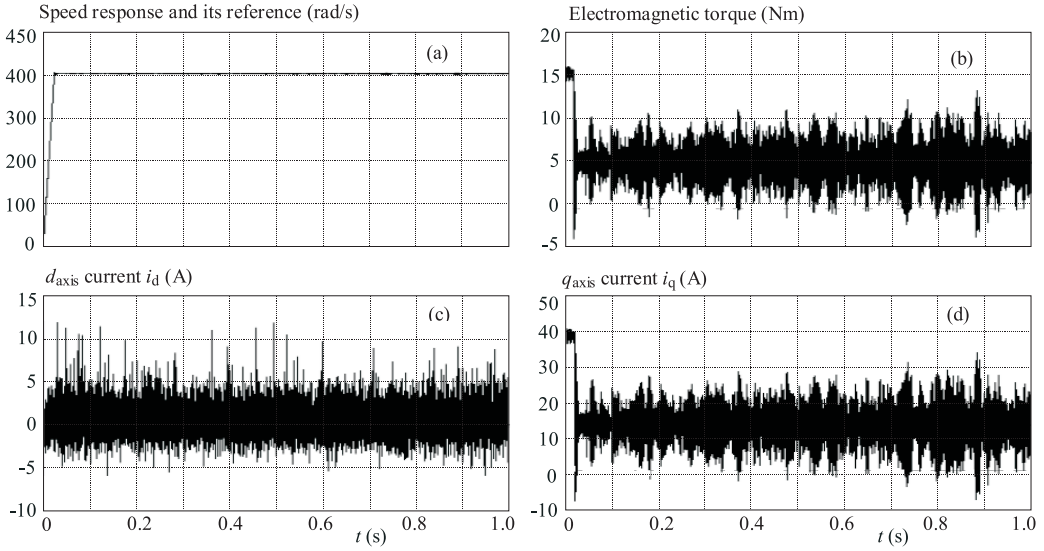

Fig. 10. Performances of the Permanent Magnet Synchronous Machine without using the Clamping bridge

5.1 Switch control strategy of the clamping bridge

Step 1: Deduction of the sign of the differences. We use the following equations

$$C\frac{\mathrm{d}(U_{c1}-U_{c2})}{\mathrm{d}t} = (i_{L1}+i_{c2}-i_{d2}-i_{c1})\,,$$
$$C\frac{\mathrm{d}(U_{c3}-U_{c4})}{\mathrm{d}t} = (i_{L2}+i_{c3}-i_{c4}-i_{d3})\,. \qquad (21)$$

Step 2: Deduction of the command of the transistors

$$\begin{aligned} U_{c2} > U_{c1} &\Longrightarrow T_2 = 1; T_1 = 0\,,\\ U_{c1} > U_{c2} &\Longrightarrow T_2 = 0; T_1 = 1\,,\\ U_{c3} > U_{c4} &\Longrightarrow T_3 = 1; T_4 = 0\,,\\ U_{c4} > U_{c3} &\Longrightarrow T_3 = 0; T_4 = 1\,. \end{aligned} \qquad (22)$$

6 SIMULATION RESULTS

6.1 Results interpretation

Figure 8 shows the voltage U_c and its reference obtained by controlling the two-level PWM rectifier controlled by sliding mode control function. This voltage follows perfectly its reference (200 V). The network current i_{res1} is in phase with the network voltage V_{res1}.

On Fig. 9, we show perfectly the problem of the unbalance of the four DC voltages of the intermediate capacitors bridge. The voltages U_{c2} and U_{c4} are decreasing and the voltages U_{c1} and U_{c3} are increasing.

Figure 10, the characteristics of the drive of the PM synchronous machine (Speed, torque and different currents) fed by a two-level PWM current rectifier — five-level NPC VSI cascade show that the undulations of the currents id, iq and the electromagnetic torque are very

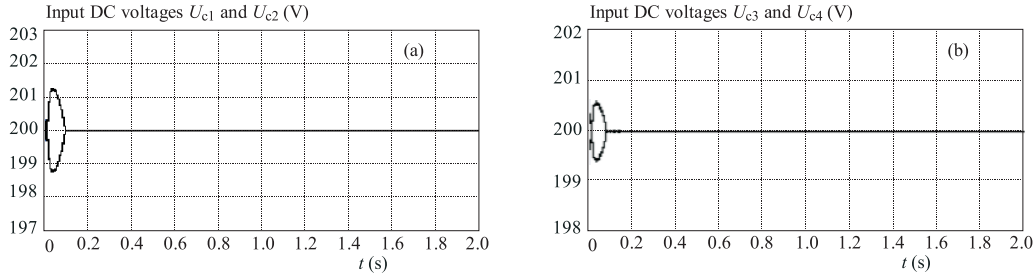

Fig. 11. DC input voltages of the five-level NPC-VSI by using the clamping bridge

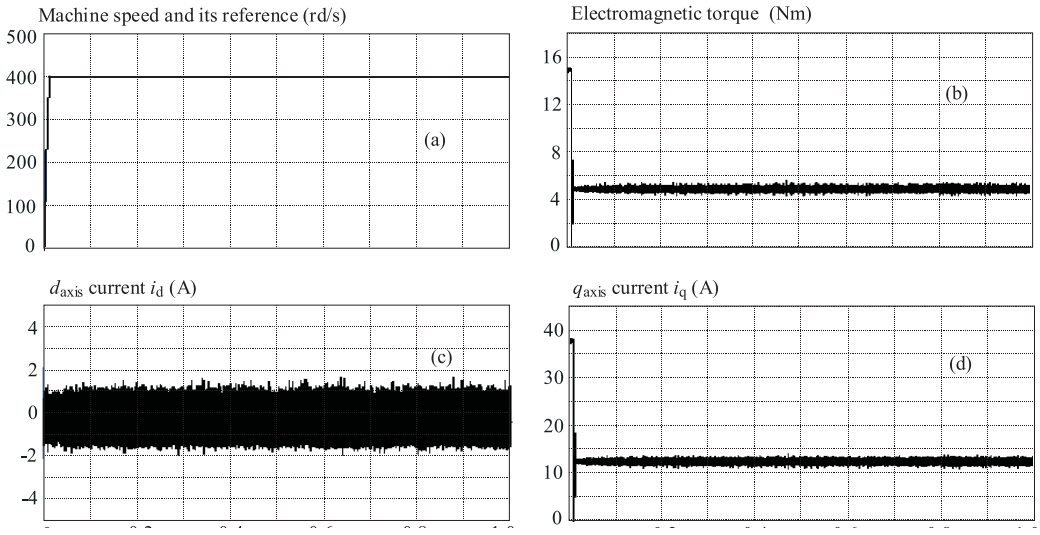

Fig. 12. Performances of the Permanent Magnet Synchronous Machine without using the Clamping bridge

important. These results show the importance of the stability of the input DC voltages of the inverter to have good performances for the speed control of the PM synchronous machine.

Figure 11 shows the different input DC voltages obtained by using the stabilisation bridge. We can see that the output voltages of the rectifier (U_{c1}, U_{c2}, U_{c3} and U_{c4}) stabilise around 200 V. By using this technique of stabilisation, we can remark on Fig. 12, the undulations on the performances (Torque and currents i_d and i_q) of the PMSM disappear and those performances are improved by using the inductive Clamping bridge.

7 CONCLUSION

The present contribution intends to demonstrate that permanent magnet synchronous machine control based on sliding mode control when applied with a two-level PWM current rectifier — Five-level PWM NPC-VSI may contribute both for functional performances improvement and attenuation of some technological limitations. With a high number of semi-conducting devices, current and voltage quality are improved and weight reduced by avoiding heavy filters.

The input DC voltages are generated by a five-level PWM current rectifier controlled by sliding mode function control. By this study, we have particularly shown the problem of the stability and its effects on the speed control of PMSM and the input DC voltages sources of the inverter.

In the last part of this paper, we propose a simple solution to stabilise the four DC voltages and this by using a new clamping bridge composed by four switches (pair transistor-diode) and two inductances.

This technique permit an economic and simple electronic implementation, whereas in the space vector modulation control the computational burden, the complexity of the algorithms and the number of instructions are drastic especially when the number of levels of the inverter is greater than three.

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Received 31 October 2008

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