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PAPERS

Design of area-efficient GHz range current mode frequency synthesizer using standard CMOS technology

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In this paper, an area and power efficient current mode frequency synthesizer for system-on-chip (SoC) is proposed. A current-mode transformer loop filter suitable for low supply voltage is implemented to remove the need of a large capacitor in the loop filter, and a current controlled oscillator with additional voltage based frequency tuning mechanism is designed with an active inductor. The proposed design is further integrated with a fully programmable frequency divider to maintain a good balance among output frequency operating range, power consumption as well as silicon area. A test chip is implemented in a standard 0.13 μm CMOS technology, measurement result demonstrates that the proposed design has a working range from 916 MHz to 1.1 l GHz and occupies a silicon area of 0.25 mm^2 while consuming 8.4 mW from a 1.2 V supply.

K e y w o r d s: frequency-locked loop, CMOS, integrated circuit, active inductor

1 Introduction

The complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) has been one of the key momentums of the information technology in recent decades. There is always of a great interest in the application of low power computing techniques at the system, algorithmic and circuit level [1–5]. Phase-locked loops (PLLs) or frequency synthesizers have been studied extensively for their key roles as a clock generator in many applications such as microprocessors, computer networks and data links [6–10]. However, the design of PLL is still a challenge since the key desires at different applications can be quite different from each other. In CMOS SoC, *eg*, the major consideration will be a high level of integration. Fully integrated PLLs have been extensively reported in literatures [10-15]. However, it is still of a great interest that the designs can be implemented using a standard CMOS technology with a low supply voltage and power consumption, while a high area-efficiency is still maintained. In a PLL, the silicon area is mainly occupied by the large capacitor of the loop filter (tens of pF or above) and the on-chip inductor (several nH) of the LC tank based oscillator. Certain techniques, such as capacitor multiplier and current mode filter based on active inductor have been proposed to solve the issue of loop capacitor [6, 7, 10–15]. For the inductor which working at GHz range or lower, it would be too large to be integrated on-chip since its dimension is almost inversely proportional to the operating frequency. A ring oscillator can be used to achieve a very high area efficiency, but it has a poor phase noise or jitter performance [9]. At the GHz or below, the LC oscillator with active inductor is a potential candidate where silicon area can be significantly reduced while an acceptable phase noise performance is still maintained. In [6], this design concept is demonstrated with a simulated 3 GHz PLL using a 0.18 μm CMOS technology. However, without a frequency divider, this design can only provide the output at the same frequency of input, incapable of working as a frequency synthesizer. It is therefore necessary to design a PLL which can generate programmable output frequency signal to meet the requirement of clock generator and other building blocks should be designed more compatible to digital circuit to further improve the level of integration.

In this paper, we propose a current-mode PLL that can be used in a CMOS SoC. It is featured with an active transformer loop filter, fine-tuned LC oscillator with active inductor, and fully programmable frequency divider. It can work at GHz while maintaining a good balance among all design specifications such as working range, silicon area and power consumption.

2 Active transformer current mode PLL

Phase-locked loop is a negative feedback loop used to generate a precisely controlled output frequency. In such as system, the phase frequency detector (PFD) detects the difference between the input reference signal and the feedback signal, hence providing UP (or DN) signal to speed up (or slow down) the output frequency of the oscillator. The loop filter is an essential building block to provide a smoothly changed control voltage (or current). The current mode PLL is first proposed in [5], where the voltage-mode RC loop filter is replaced with a current-mode RL loop filter using active inductors, or transformers with enhanced equivalent inductance as

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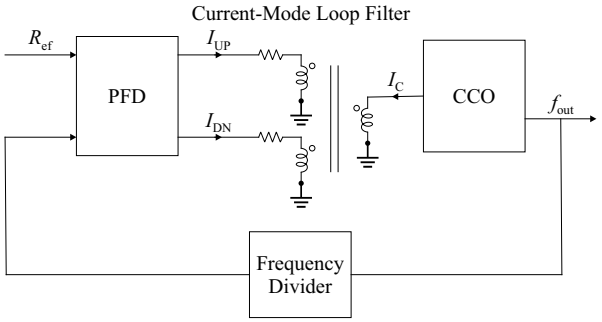

Fig. 1. The architecture of the proposed current-mode PLL

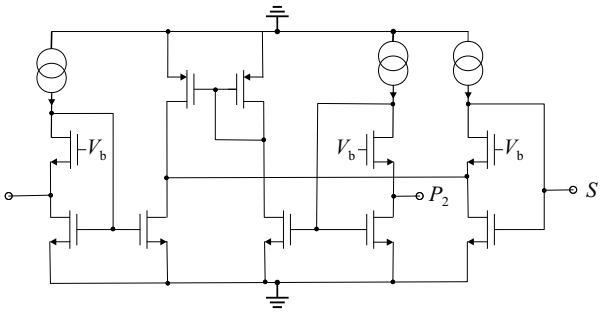

Fig. 2. The topology of the active transformer

shown in Fig. 1. The loop filter is used to generator a current I_c that controls the output frequency of a current-controlled oscillator (CCO) [5–7]. The proposed work, a current mode frequency synthesizer is an improved design based on this concept. The CCO is implemented with additional voltage controlled frequency tuning mechanism and a fully programmable frequency divider is added so that the output frequency of the PLL can be arbitrarily generated from a low frequency input signal, Ref. Therefore, the proposed work operates with more flexibility in loop dynamics and output frequency.

2.1 Current-mode Transformer Loop Filter

Transformer in the loop filter is designed at the transistor level as shown in Fig. 2, which includes three active inductors, implemented with two back-to-back connected transconductors. In this design, the low supply voltage Wu's current reuse active inductors, instead of the cascaded design, are used to achieve a supply voltage of 1.2 V, which is a standard one compatible with other digital blocks in 0.13 μm CMOS. The two input ports, $P1$ and $P2$ relate to the UP and DN signals of the PFD respectively through a 6K resistor, and L_s is the secondary winding connected with the CCO. At the output port of S, to save silicon area, the load capacitor is implemented with a MOS transistor, which has the size of 8μm/8μm.

The RL low-pass filter can be constructed by connecting a resistor in series with the transformer. It has a cut-off frequency of

$$\omega_{(-3)dB} = \frac{R_1}{L_{11}} \frac{1}{(1 - \frac{M_{12}M_{21}}{L_{11}L_{22}})} . \tag{1}$$

where R_1 is the loop resistor, L_{11} and L_{22} are the self-inductors of the primary and secondary windings, L_{P1} and L_S, respectively, M_{12} and M_{21} are the mutual inductances between the two windings. The designer will have several design freedoms to make the design flexible at bandwidth, and more importantly, it is possible to design on-chip equivalent inductance up to tens of nH. The self-impedance of the primary inductor, P_1, is given by [6]

$$Z_{11}(s) = \frac{g_0}{C_{gs}^2} \frac{1 + s\frac{C_{gs}}{g_0}}{(s^2 + s\frac{g_m}{c_{gs}} + \frac{g_m^2}{c_{gs}^2})} . \tag{2}$$

It exhibits an inductance between the frequency zero and self-resonant frequency that are given as g_0/C_{gs} and g_m/C_{gs} respectively. Likewise, the impedance looking into the secondary winding is given by

$$Z_{22}(s) = \frac{g_0}{C_{gs}^2} \frac{1 + s\frac{C_{gs}}{g_0}}{(s^2 + s\frac{g_m}{c_{gs}} + \frac{g_m g_0}{c_{gs}^2})} . \tag{3}$$

There is a mutual inductance between the two windings that is given by

$$Z_{21}(s) = -\frac{g_m^3}{2} \frac{(sC_{gs} + g_0)}{(sC_{gs}+g_m)(s^2C_{gs}^2+sC_{gs}g_m+g_m g_0)^2} . \tag{4}$$

The cutoff frequency of the mutual inductance is given by $\sqrt{g_m g_0}/C_{gs}$ approximately. It is possible to design a low pass filter with a small silicon area since the inductance can be easily obtained by properly sizing of the transistor. simulated inductances of the proposed active transformer is shown in Fig. 3. At 900 MHz, the inductances of the primary and secondary windings are still 12 nH and 5 nH respectively.

2.2 Current-controlled oscillator

Current-controlled oscillator (CCO) is the key building block in the proposed system. The basic topology of the CCO is shown in Fig. 4(a), the cross-coupled MOS provides the negative g_m for oscillating, while the upper part is the active inductor. The current reuse technique is used to improve the power efficiency and the biasing voltage, V_b is used to adjust the current of the active inductor enhance to change the equivalent inductance.

The input admittance of the circuit is given as

$$Y_{in}(s) = sC_1 + g_m + \frac{g_m^2}{sC_2 - g_m} .$$

C_1 and C_2 are the equivalent capacitors of the two input ports. For a Wu's gyrator-C active inductor, the equivalent inductance is $C/(g_{m1}g_{m2})$,where C is the equivalent capacitance and g_{m1} and g_{m2} are the g_m of the two MOS transistors [6]. In practice, the biasing current can not be too low, otherwise the output amplitude will be too small

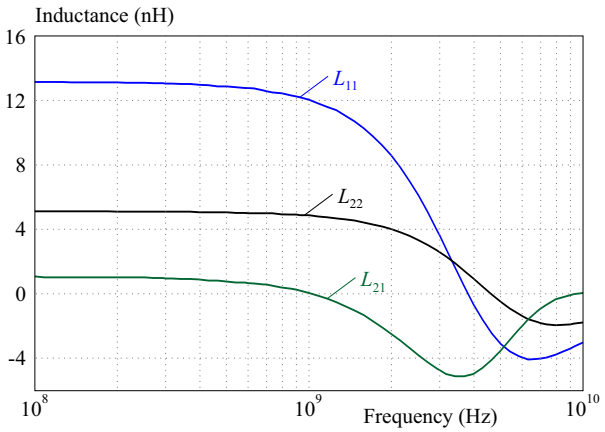

Fig. 3. The simulated inductances of the transformer

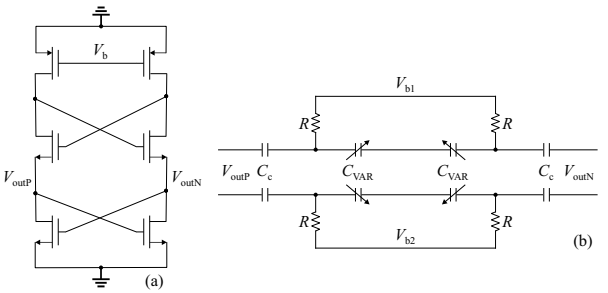

Fig. 4. The topology of the CCO, (a) – core, (b) – tuning circuit-one set of capacitor array

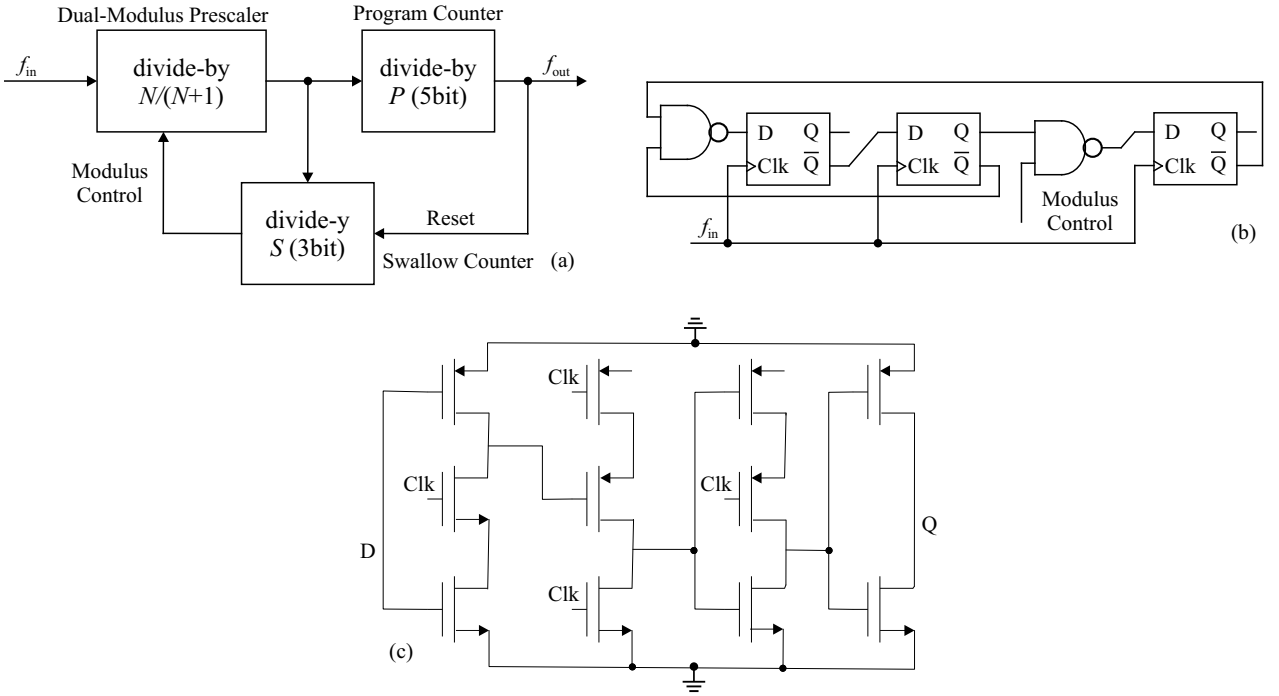

Fig. 5. The topology of the frequency divider, (a) – architecture, (b) – presclaer, (c) – TSPC DFF

to sustain robust operation against PVT variations. However, a higher current result in a smaller inductance and higher quality factor, which is suitable for high frequency operation only. To overcome this design trade-off, the oscillator is integrated with a tuning capacitor and varactor array as shown in Fig. 4(b), hence the tuning of output frequency can be performed by changing capacitance as well.

More importantly, it is now possible to use a relatively high biasing current to obtain a robust operation with a high-quality factor. Even with additional tuning mechanism, the capacitor array should be carefully designed to avoid any malfunction. The major challenges include the monotonicity and linearity of output frequency tuning. In this work, the output frequency is adjustable by changing inductance (current biasing) or capacitance (voltage biasing). For current biasing tuning, the equivalent inductance can variate significantly, *eg*, over 20 nH from 100 MHz to 1 GHz as simulated in [6]. The change of inductance will cause a large K_{CCO}, which consequently leads a poor phase noise or malfunction of the whole loop. Therefore, in this work, the biasing of the current is kept stable after a coarse tuning is fixed and the output frequency is mainly fine tuned by the varactor and capacitor array. Similarly, the varactor (usually a MOS transistor) exhibits a non-linear C–V curve and the K_{CCO} may change at different tuning curves of capacitor array. It is therefore necessary to compensate this non-linearity using certain techniques. In this work, six sets of varactor arrays with differential tuning voltage as shown in Fig. 4(b). The basic idea is that each set of capacitances is biased at different voltages, and exhibits certain ranges of linear-

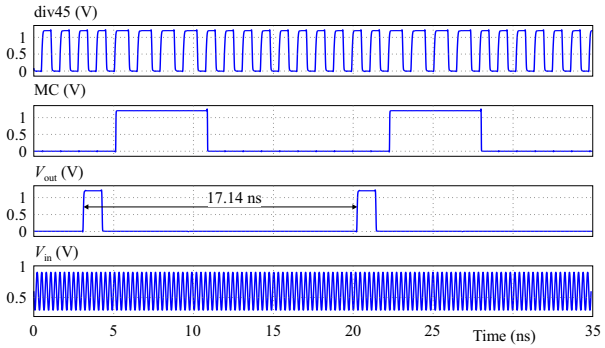

Fig. 6. The input and output waveforms of the frequency divider

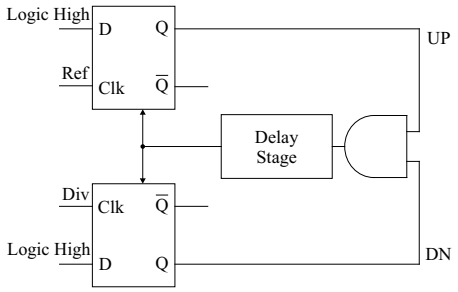

Fig. 7. The PFD

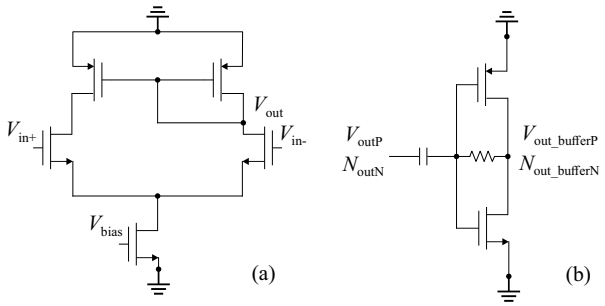

Fig. 8. The buffer stages, (a) – MCML-to-CMOS, (b) – Self-biased CMOS

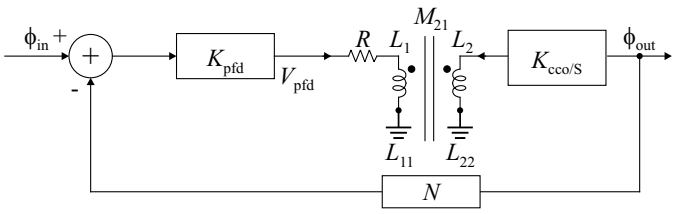

Fig. 9. The phase domain model of the PLL

ity and non-linearity, but the combination of the whole array has a overall linear tuning range. By implementing this technique, the equivalent capacitance exhibits good linearity *vs* tuning voltage [14–16].

2.3 Frequency divider

As a frequency synthesizer, a programmable frequency divider should be included in the feedback loop. In this work, a pulse-swallow integer-N frequency divider is used as shown in Fig. 5(a) [4]. It includes a divide-by-4/5 prescaler, a 5-bit P-counter and a 3-bit S-counter, which can provide a fully programmable division ratio from 14 to 129. The divide-by-4/5 prescaler includes three D-flip-flops (DFF) and two NAND gates, while the modulus control signal is used to disable one DFF so that the circuit work as a divide-by-4 as shown in Fig. 5(b) To achieve a high operating frequency, the DFFs in prescaler are implemented with True-Single-Phase-Clock (TSPC) logic as shown in Fig. 5(c) while the static CMOS logic is used in the counters since the operating frequency is 4 or 5 times lower than the prescaler. A differential to single-ended buffer (MCML-to-CMOS) is used to convert the differential signal of the oscillator to the input of the frequency divider. In simulation, the circuit can work up to 3.5 GHz when implemented with a standard 0.13 μm CMOS technology. Figure 6 shows the input and output waveform of the frequency divider. The the output frequency after divide-by-60 is now 58.33 MHz, with a period of 17.14 ns.

2.4 Other building blocks

Other building blocks include the phase-frequency detector (PFD), biasing circuit as well as the input and output buffers of the key building blocks. The PFD is a standard design as shown in Fig. 7, several inverters are added in the reset path to remove the potential dead zone that is caused by finite rise time of the reset signal [4].

The biasing circuits including the bandgap circuit and voltage regulation. They are implemented with standard MOS transistors or PNP devices. Since the high frequency oscillator signals and the loop filter are differential signal, several input and output buffers are designed to change the MOS current mode logic (MCML) to single-ended CMOS logic, and vice versa. The output of the oscillator is separated into two paths, one to drive several stages of self-biasing buffer then consequently a 50 Ohm of the off-chip measurement facility. As shown in Fig. 8(a), the PMOS transistors are used as active load to change the differential signals (V_{in+} and V_{in-}) to the singled-ended signal, V_{out}. Similarly, the input buffer is used where the off-chip reference can be changed to differential signals with a dummy connection of one input terminal. For measurement proposal, the output signals are differential since there are still many off-chips parasitic that may impact the measurement. Therefore, the two output signals of the oscillator, V_{outP} and V_{outN} are each connected with a self-biased inverter followed by a chain of inverters so that the output can be at amplified till full swing and to drive off-chip 50 Ohm measurement facilities as shown in Fig. 8(b).

Table 1. Summary of the PLL performance

Spec	This work	(6)	(7)	(8)	(9)
Process(nm)	130	180	180	55	40
Frequency(GHz)	0.91-1.1	3	2.4	0.1-1.5	0.1-3.1
Silicon Area(mm2)	0.25	2.8	0.013	0.05	0.045
Power(mW)	8.4	16	34	2.8	5
Vdd(V)	1.2	1.8	1.8	N/A	N/A
Oscillator Type	Act. LC	Act. LC	Act. LC	LC	Ring
Experimental Results	Yes	No	No	Yes	No

*fixed output frequency, **only a core circuits

2.5 System optimisation

The system should be planned based on the loop dynamics after the design of each building blocks. In [6], the system is designed without a frequency divider, which has a division ratio of N. In this work, the optimisation is carried out as follows.

The close loop transfer function of the PLL with a frequency divider is given as

$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_{pfd}M_{21}K_{CCO}/N}{s^2L_{11}L_{22} + sRL_{22} + K_{pfd}M_{21}K_{CCO}/N}.$$

The natural frequency and damping factor are therefore given as

$$\omega_n = \sqrt{\frac{K_{pfd}K_{CCO}M_{21}}{NL_{11}L_{22}}}, \quad \xi = \frac{R}{2}\sqrt{\frac{NL_{22}}{K_{pfd}K_{CCO}M_{21}L_{11}}}.$$

This system is a type I PLL, and the damping factor can be determined by properly sizing of the resistor without trading off the loop bandwidth. A larger inductance is helpful to noise suppression since the bandwidth is narrow, but the mutual inductance plays the opposite role in determining the bandwidth. In this work, since L_{11}, L_{21}, M_{21} and even K_{CCO} are adjustable, the system can be easily changed to meet different applications, making the system flexible with a standard CMOS technology.

3 Design example

Active transformer current-mode PLL has been implemented in a standard 0.13 μm CMOS technology as an example. As shown in Fig. 3, the active inductor becomes a capacitor at the frequency higher than 4 GHz in pre-layout simulation, suggesting that the suitable target frequency at around 1 GHz. Also, as analysed above, the conventional LC tank based oscillator is preferred at several GHz or above since the inductor will be quite small and the phase noise performance will be much better. Using the 0.13 μm CMOS technology, the layout of the PLL, including the core PLL circuits and digital controls (Serial Peripheral Interface, SPI and registers) occupies a silicon area about $500 \times 500\,\mu\text{m}^2$. If advanced CMOS technology such as 40nm CMOS technology [9], the silicon area can be reduced significantly since the components used in this work are quite standard MOS transistors, resistors and capacitors. The circuit is highly flexible at the operating range and resolution of the output frequency since the frequency divider are programmable and the oscillator has both current biasing and varactor tuning mechanisms. If a higher resolution is needed, more stages in the programmable counter can be used and the input reference can be adjusted accordingly. In this design example, the output frequency of the control voltage is shown in Fig. 10. Thanks to the optimisation of loop dynamic, the PLL can lock at several hundred ns.

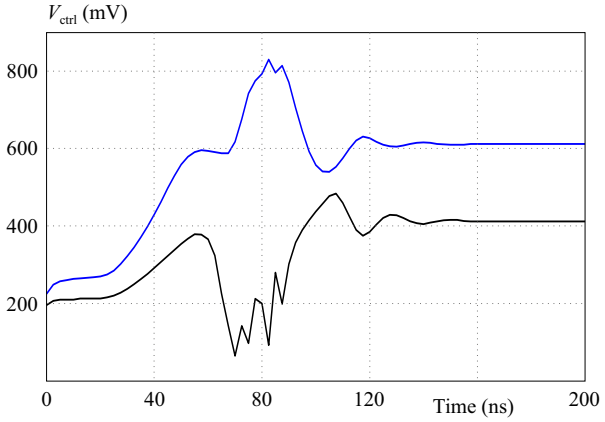

Fig. 10. The differential outputs of the control voltage of the PLL

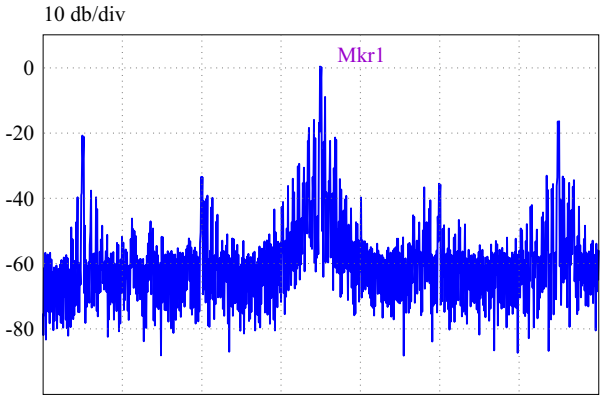

Fig. 11. The output spectrum: 10 dB/div, Mrk 1.1225 GHz,

The die photo of the test chip and the PCB of the proposed work. The full test chip occupies a silicon area of $900\,\mu\text{m} \times 600\,\mu\text{m}$ including the testing buffers and ESD pads. Measurement is carried out on the PCB where the test chip is bonded with a configuration of chip-on-board. The PLL has a maximum operating frequency of 1.1 GHz with a power consumption of 8.4 mW from a 1.2 V supply, excluding the power of external clock generator and buffer for test proposal. The power consuming output buffers, which are designed to match and drive the 50 Ω impedance of the measurement facilities, consume 7 mW. The output signal is measured using a Keysight EXA 9010B signal analyser, where the proposed frequency synthesizer has an output power of 0 dBm (drives 50 Ohm) with the 18 MHz external clock as shown in Fig. 12. By changing the division ratio of the frequency divider or the reference clock, it is possible to have a lowest output frequency of 916 MHz in this test chip. Table I shows the comparison of this work with other reported PLLs. The proposed work exhibits a good balance among output frequency, power consumption and silicon area, and it is suitable to implemented with nanoscale CMOS technology which can significantly reduce the silicon area further.

4 Conclusion

An active transformer current mode PLL has been implemented. By using a low supply active inductor, additional voltage tuning CCO, and a full programmable counter, the proposed work is featured with a fast locking, low supply voltage and flexible in bandwidth working range and resolution. A test chip is fabricated using a standard $0.13\,\mu\text{m}$ CMOS technology, and it is able to work at GHz with a maximum power consumption of 8.4 mW, and it is reconfigurable at different applications and technologies.

Acknowledgements

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