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NEURAL NETWORK–BASED DEFECT DETECTION IN ANALOG AND MIXED IC USING DIGITAL SIGNAL PREPROCESSING

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The major goal of our work was to develop an efficient defect-oriented parametric test method for analog & mixed-signal integrated circuits based on Artificial Neural Network (ANN) classification of a selected circuit's parameter using different methods of signal preprocessing. Thus, ANN has been used for detecting catastrophic defects in an experimental mixed-signal CMOS circuits by sensing the abnormalities in the analyzed circuit's response and by their consequent classification into a proper category, representing either good or defective circuit. To reduce the complexity of neural network, Wavelet Decomposition (WD) is used to perform preprocessing of the analyzed parameter. This brings significant enhancement in the correct classification, and makes the neural network-based test method very efficient and versatile for detecting hard-detectable catastrophic defects. Moreover, investigation of the possibility to utilize this approach also in detection of parametric faults in analog circuits was the subject of our research as well. Therefore, a new methodology for neural network based detection of parametric defects using Principal Component Analysis (PCA) of the analyzed circuit's response has been proposed. Since the training set selection plays a crucial role in achieving desirable classification results, we also propose a new approach to this selection employing Convex hull (qhull) graphics algorithm. As it is shown in the experiments performed, well trained neural network is not only able to detect the faulty devices but also identify the particular parameter deviation in the respective circuit element.

K e y w o r d s: testing analog IC, defect detection, artificial neural networks, wavelet decomposition, principal component analysis, convex hull algorithm

1 INTRODUCTION

In contemporary integrated circuits (IC), testing and test evaluation are becoming very important but very complex tasks. On one side, test efficiency and achieved reliability of IC production are of utmost importance but on the other hand, time and complexity of the test are crucial aspects from test cost point of view. Thus, the main goal of testing is to achieve desired IC reliability in the shortest possible time to satisfy customer's needs with appropriate time to market and profit. The fact that in recent IC designs mixed signal devices are rather common and the use of embedded IP cores is becoming very popular, makes testing even more complicated. Another test difficulty arises from deep sub-micron technologies that bring specific defect mechanisms resulting in new physical defects. Therefore, there is no stand-alone test method that would provide satisfactory defect detection level, and several test strategies have to be combined together to achieve this goal. Thus, complementary defect-oriented test strategies have been developed and used, including the power supply current (IDD) monitoring originally introduced for testing digital CMOS circuits [1–5] as a method that requires dedicated test pattern generation with a significantly reduced number of test vectors [6, 7].

Many defect-oriented test methods might be considered as parametric since their decision criteria are based on the analysis of analog, time continuous parameters, *ie* supply current signal, output current, *etc.* However, in defect-oriented test strategies, a meaningful threshold needs to be defined to distinguish between good and bad circuits. This is the crucial point of all threshold-based test methods because improper setting of the pass/fail limit may essentially reduce either yield, or quality of the production. Moreover, most of the proposed defect-oriented test methods suffer from a poor versatility. They effectively cover a dedicated defect class only, either opens or shorts, and their use for both analog as well as digital circuits is strongly limited.

These difficulties make the application of artificial neural networks (ANN) in the field of analog testing very appealing. Instead of a simple threshold decision used in the most of the parametric methods, neural network approach offers sophisticated and continuous analysis of the selected circuit's parameter, and looks for abnormal behavior expected in a defective circuit. Some works using ANN approach for detection parametric faults (undesired deviations in resistance and capacitance values) in analog circuits by evaluating different circuit responses have been published [8–12]. However, catastrophic faults, such as gate-oxide shorts or drain/source opens, are of the utmost importance from the reliability point of view. Therefore, these physical defects commonly occurring in the CMOS process were addressed in [13], where feasibility of ANN-based identification of defective analog circuits

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was introduced, and its feasibility experimentally verified on a simple analog circuit example. Nevertheless, it has been found out that in order to achieve satisfactory classification results, a significant number of input waveforms in the training phase might be required even for small circuit sizes, and moreover, the network architecture might be rather complex. This makes the training process rather time consuming.

In this paper, we propose further preprocessing of the signals before they are applied to the neural network that offers significant network performance enhancement for reduced training vector set size and the network complexity. This substantial contribution has been proven by experimental results achieved on a mixed-signal test benchmark circuit of sufficient complexity. The neural network is used for identification of a potentially defective circuit by performing analysis of a selected circuit parameter, which is sorted into two categories, good, and bad corresponding to defect-free, and defective chips, respectively. Wavelet decomposition is utilized to preprocess the neural network input signals. Then, significant results, summarizing the efficiency enhancement in covering different physical defects are presented. Consequently, comparison of the previously achieved classification results (in both time and frequency domains) to the results obtained using wavelet analysis preprocessing is performed. In the second part of our work, we investigate ANN approach ability to detect and identify also parametric type of faults in an experimental analog circuit. Statistical method of so called Principal Component Analysis is utilized to preprocess the input signals before being applied to the network and furthermore, and the Convex hull graphic algorithm is used to find the proper training vector set. This could drastically reduce the size of input layer of the neural network and minimize the training set size. All circuit's current responses were gathered from HSpice circuit simulations. The selected artificial neural network structures, algorithms and all the computations were performed in MIDI toolbox, developed by authors, which is an extension of Neural Network Toolbox available in MATLAB environment.

2 NEURAL NETWORKS AND SIGNAL PROCESSING METHODS

2.1 Neural Networks background

The artificial neural networks are computing systems that work in an analogy of the nervous system of the human brain, in which connections organize neurons into networks. ANNs are computational structures that can be configured by examples, and can improve their performance by a dynamic adaptation process. The adaptation process of an ANN is performed once, and only on a finite subset of all possible input instances, also called the training set, which consists of input-output vector pairs. The goal of ANN aimed for signal (pattern) classification is to adapt itself to classify applied input vectors, representing physical objects or events, into several categories. The network selected for the classification of defective analog circuits is a multilayer feed-forward neural network trained by back-propagation [14–15].

Feed-forward ANN is a network of neurons organized into layers: an input layer, one or more hidden layers, and an output layer of neurons. The layer of hidden units allows the network to extract important features from the signal, and a number of hidden neurons are set empirically to achieve the best network performance. Correct neural network-based classification in the time domain requires a significant number of input vectors, and a certain complexity of the neural network. On the other hand, in the frequency domain, the higher classification efficiency even for smaller sizes of the training vector sets is obtained [9]. Therefore, further preprocessing of the input vectors applied to the neural network might significantly enhance its performance, and reduce the complexity of the network.

2.2. Signal processing methods

Wawelet Decomposition

As it was considered above, preprocessing of the network input data can drastically simplify the network architecture, improve its performance, and reduce the number of input vectors needed for the network training. Wavelet transform provides high time resolution, and low frequency resolution for high frequencies (low scales); and low time resolution, and high frequency resolution for low frequencies (high scales). That feature is ideal for preprocessing of non-stationary signals [16].

Wavelet transform of a continuous-time signal $x(t)$ is defined by the following equation:

$$W_{x(a,b)} = |a|^{-\frac{1}{2}} \int x(t)\psi\Big(\frac{t-b}{a}\Big)\mathrm{d}t \tag{1}$$

where function $\psi(t)$ is the so-called wavelet or *mother wavelet*, defined as

$$\psi_{a,b}(t) = |a|^{-\frac{1}{2}}\psi\Big(\frac{t-b}{a}\Big)\,. \tag{2}$$

Coefficients a, and b define degree of scaling, and time shift of the mother wavelet $\psi(t)$, respectively. The wavelet coefficients $W_{x(a,b)}$ give a measure of similarity between shifted, and scaled mother wavelet with an input signal $x(t)$. Calculation of the wavelet coefficients at every scale & position is a very computationally expensive job. To avoid this, one can choose dyadic (discrete) sampling, which leads to a discrete wavelet transform. Wavelet analysis in its discrete form assumes the following sampling points: $a_m = 2^m$, $b_{mn} = a_m nT = 2^m nT$, where T is sampling period, and m, n are integers. By applying dyadic sampling, Equation (1) yields its discrete form

$$W_{(m,n)} = 2^{-\frac{m}{2}} \sum_k x(k)\psi\big(2^{-m}k - n\big) \tag{3}$$

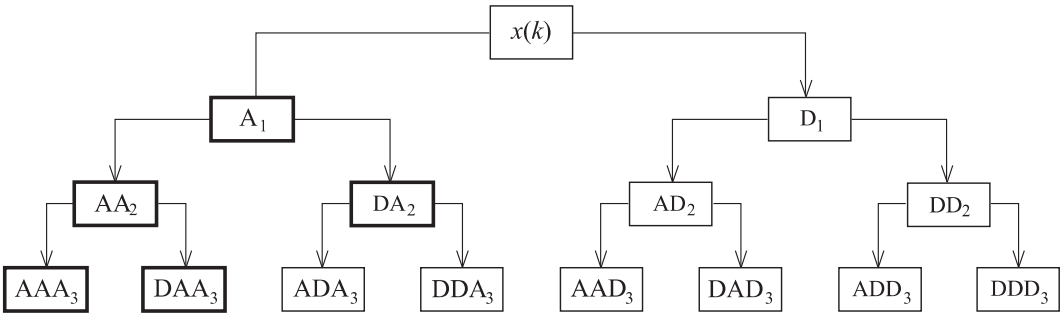

Fig. 1. Wavelet decomposition of a signal into approximations (A), and details (D)

where the discrete wavelet $\psi(k)$ is a sampled version of a continuous $\psi(t)$, and $x(k)$ is a discrete signal.

Discrete wavelet transform, where a signal is decomposed into so-called approximations and details, can be realized by the multi-rate filter bank [17]. Approximations represent low frequency signal content, and details correspond to high frequency components of the processed signal. Each set of the frequency bands of a signal can be decomposed further into other levels of approximations & details. One can construct full binary decomposition tree, known as a wavelet packet decomposition tree, depicted in Fig. 1. In our work, we use a wavelet decomposition tree, where the higher bands (details) become a part of the output while only the lower bands (approximations) are further split into two bands depicted in bold.

The proper choice of the mother wavelet plays a crucial role in the signal preprocessing. Several families have been proven to be useful in signal and image processing (Daubechies, Biorthogonal, Haar, Shanon, *etc.*). Each family has specific properties which make them suitable for certain applications. Haar wavelet has good time localization but poor frequency localization. On the other hand, the Shanon wavelet has poor time localization, but its frequency localization is good because it has the spectrum of an ideal bandpass filter. There are orthonormal wavelets that are between these two types, giving acceptable localizations both in time, and frequency [17]. Therefore, in our work, *db*2 mother wavelet from the Daubechies family, which is orthonormal, was used since wavelet decomposition using this mother wavelet gives the most specific wavelet coefficients across a wide range of the considered defects.

Principal Component Analysis

Another method that might be used to preprocess input signal is *Principal component analysis*. PCA is probably one of the oldest and best known techniques of multivariate analysis that reveals the natural structure of data and reduces dimensionality. Recently, PCA is widely used as a visualization tool for multivariate data sets, as a method for feature extraction, and as a preliminary transformation applied to data before the other analysis tools like clustering and classification are utilized [18, 19]. Main idea of PCA is to reduce dimensionality of multivariate data set while retaining as much variability at the output as possible. It offers linear projection from n-dimensional space into p-dimensional space, where $n > p$. The first principal component is one-dimensional (1-D) linear subspace, where the variance of data is maximal. The second principal component is the direction of maximal variance in the space orthogonal to the first principal component, and so on [20].

2.3. Data normalization

Before feeding the neural network, all input data should be normalized. Data normalization is to avoid large changes in the magnitude of the input signal that may differ by several orders. These variations could represent an undesired domination, and should be removed though a normalization process. In our work, we have normalized the mean and the standard deviation of all processed data according to the following set of equations:

$$x'_I = \frac{x_i - \overline{x}}{s}\,, \tag{4}$$

$$s = \sqrt{\frac{\sum_{i=1}^{N}(x_i - \overline{x})^2}{N}}\,, \tag{5}$$

$$\overline{x} = \frac{\sum_{i=1}^{N} x_i}{N}\,, \tag{6}$$

where x'_i is the normalized form of input vector element x_i, and N is the number of input vector elements. Data normalization avoids undesired large changes in the signal magnitude, and amplifies differences between input vectors that helps learning algorithms to converge.

2.4. Neural Network simulation setup

In order to investigate the influence of the network complexity to its classification efficiency, the number of neurons in hidden layer (hidden units), representing different network topologies and complexity, was determined empirically in the range from 2 to 22 with step of 2. Each training set experiment with the given network topology was repeated 10 times with different initial values

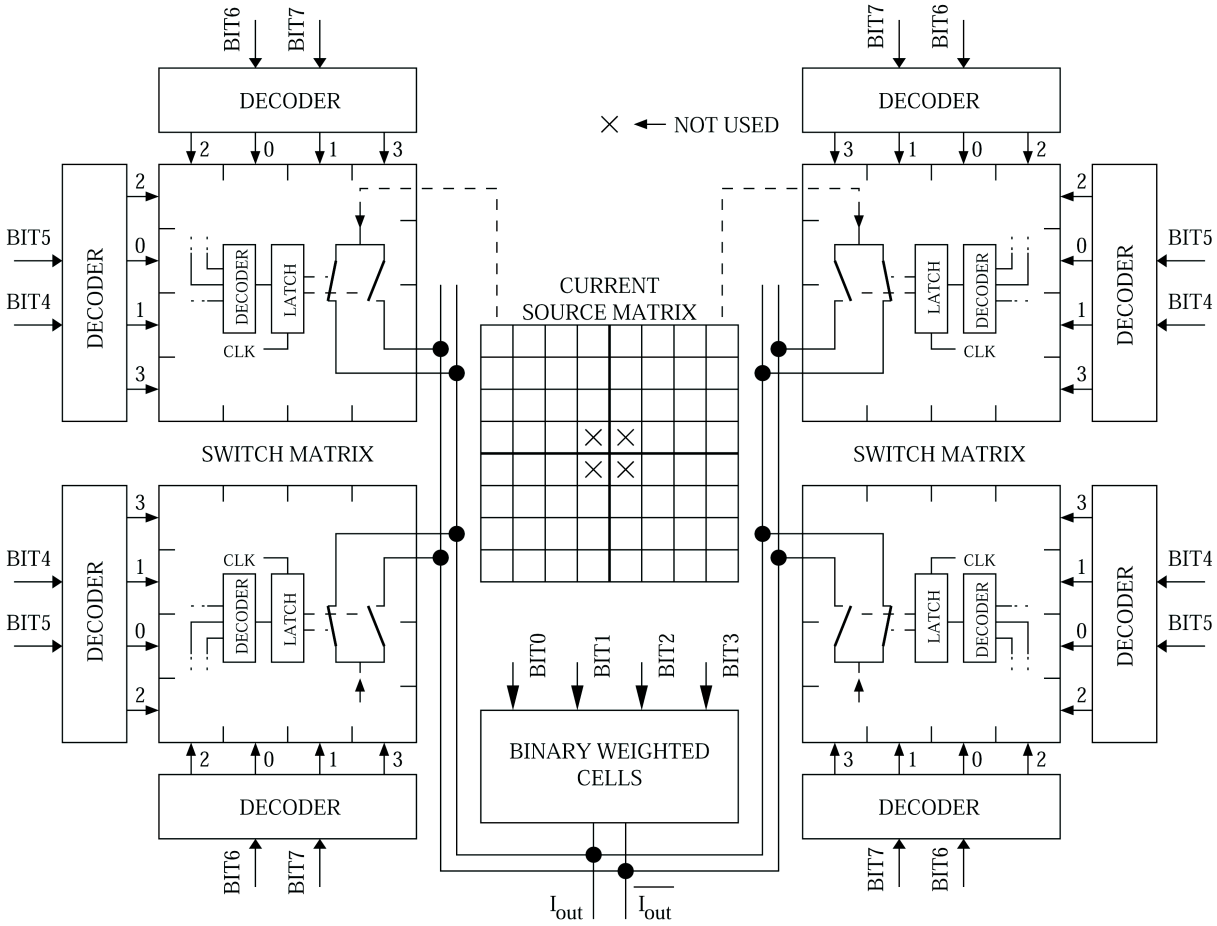

Fig. 2. Block diagram of the designed DAC.

of weight coefficients to average over variations in the network performance due to initial conditions.

There are two experimental circuits with different defect types analyzed and tested in this paper, and the particular neural network simulation setup depends on the respective experiment. Thus, in case of catastrophic defects detection in an experimental D–A converter, the following setup was used: The number of the output neurons was arbitrarily set to two, where the combination of their logic values determines the respective classification category — good or bad one. The decision boundaries for the output neurons were set to 0.25, and 0.75 for logic zero, and logic one, respectively. It means that outputs equal to or greater than 0.75 are rounded toward logic one, and outputs equal to or smaller than 0.25 are rounded toward logic zero. If at least one of the network outputs is in the range from 0.25 to 0.75, the respective input vector is not classified. This determines classification criteria for the respective category.

In case of second experimental circuit, which was used as a test vehicle for evaluating the effectiveness of the neural network in detection of parametric defects in analog IC, the network consisted of 32 neurons in the input layer, and 2 or 5 neurons in the output layer, depending on the particular experiment. Five output neurons are needed if targeting classification of the circuit output into five output classes, where also direction of the particular parameter deviation can be detected. The decision boundaries for the output neurons were set to 0.49 and 0.51 for logic zero and logic one, respectively.

Due to the property of different learning algorithms, in which the network does not converge to the same results and the respective algorithm can lose the local minimum of performance function, it is highly desirable to perform multiple network learning/simulation runs.

3 EXPERIMENTAL CIRCUITS AND DEFECTS

In our research work, efficiency of the proposed test approach in detection of two major defect classes has been investigated: a) *catastrophic defects* that represent physical imperfections and impurities originated in the technology used, such as bridgings, opens, and gate-oxide shorts; b) *parametric faults* represented by an undesired deviation in a particular circuit parameter, *eg* resistance or capacitance. Thus, a proper circuit example has been designed for each considered defect class, then several most frequent catastrophic or parametric defects were injected into the respective circuit, and selected circuit parameters were analyzed by the artificial neural network.

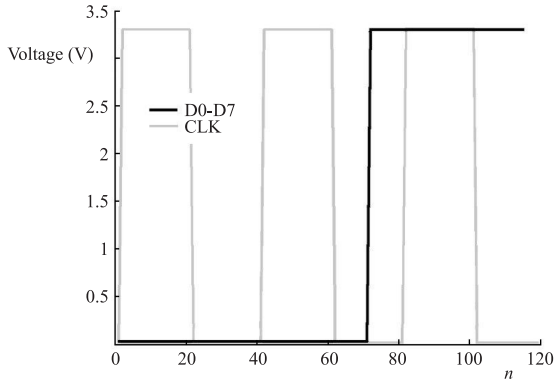

Fig. 3. The input data applied to the converter.

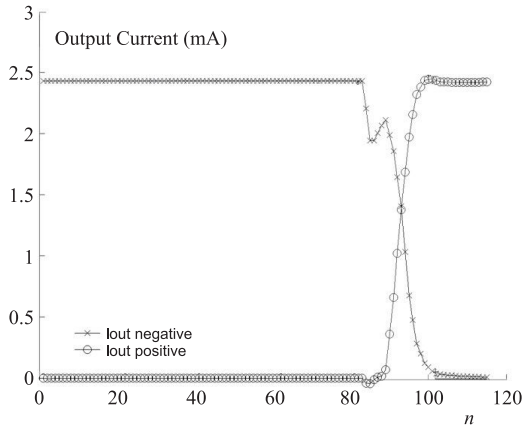

Fig. 4. DAC output currents.

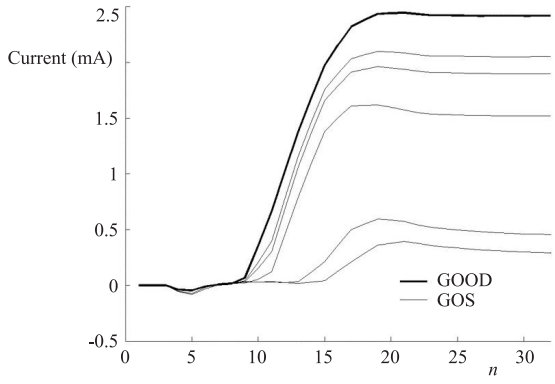

Fig. 5. Range of possible good I_{OUT} responses for worst case transistor parameters.

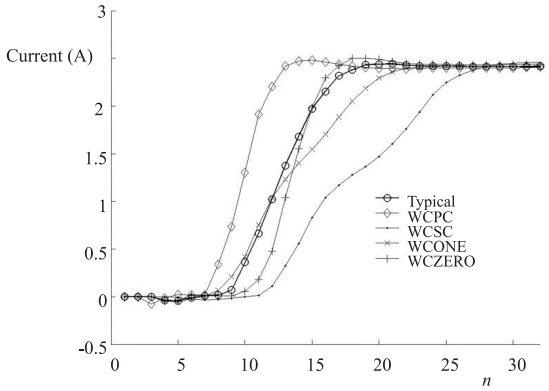

Fig. 6. Effect of a GOS defect on the DAC output current.

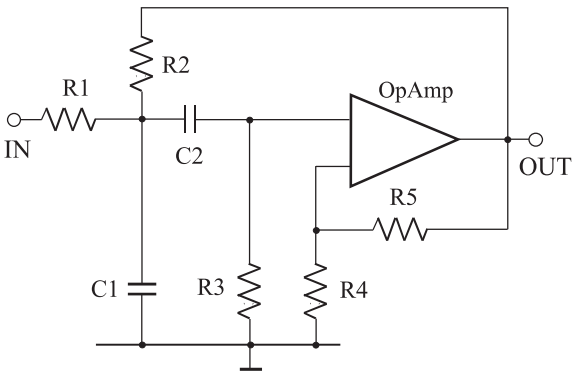

Fig. 7. Sallen-key band pass filter example.

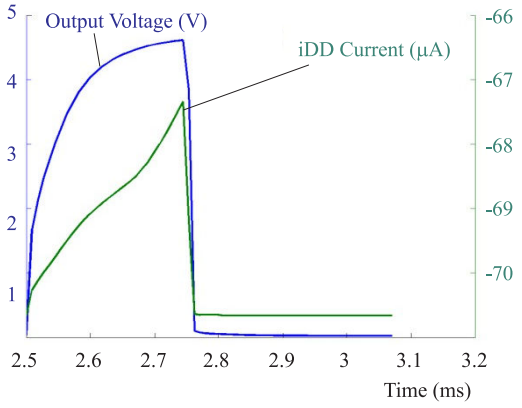

Fig. 8. Output voltage and supply current responses.

3.1. Mixed-signal circuit with catastrophic defects

To evaluate the feasibility and efficiency of the proposed approach in detecting catastrophic defects in mixed-signal circuits of real complexity, an 8-bit current steering digital-to-analog converter (DAC), designed in a standard 0.35 μm CMOS process, has been selected and used as the circuit under test (CUT). The DAC, shown in Fig. 2, has a $4 + 1 + 3$ segmented architecture: the first four most significant bits (MSB) are linearly decoded, then the 3rd bit is also linearly decoded, and the three least significant bits (LSB) are binary weighted [20]. The complementary output scheme was used to achieve a high update rate, where the current sources are continuously supplying current into either I_{OUT} or NI_{OUT} rail. The necessary current switches are placed outside the current source matrix. The analog part of the DAC, mainly formed by the current source matrix, consists of almost 600 MOS transistors; and its digital counterpart is composed of more than 2000 transistors.

Selection of the circuit's parameter to be analyzed by the neural network is the crucial point of the effective defect detection. Therefore, a parameter giving the most valuable information about a possible defect present should be selected. Given by the nature of the current steering DAC, the converter output current, which is very sensitive to possible defects, was the choice for the analyzed parameter. Therefore, the DAC output current obtained under different fault-free and faulty conditions were selected as the proper circuit's response and classified by the neural network. For this purpose, the input code of the 8-bit DAC was switched from the state of all logic zeros to the state of all logic ones, making all the current switches change their states and an eventual defect present in the circuit most observable. The applied input data and the respective I_{OUT} & NI_{OUT} current responses of the converter (sampled later for further processing) are shown in Figs. 3 and 4, respectively. The neural network input waveforms were analyzed in time domain, in frequency domain using fast Fourier transform, and finally by preprocessing using wavelet decomposition.

As it was already mentioned, ANN can conveniently classify applied input waveforms (that might be any circuit's parameter reflecting a present defect) into proper categories, good and bad, corresponding to defect-free and faulty circuits, respectively. Before the neural network is able to classify an unknown signal, the adaptation (learning) process of the network, performed on a training set of waveforms, has to be carried out. The training set represents a subset of all possible instances, and it contains waveforms from both considered categories (*bad* and *good*). Therefore, both types of input vectors are needed for this phase.

In reality, the behavior of good circuits might vary in a certain range, given by technology parameters' deviations and different temperature conditions, also fault-free output current responses should represent these natural variations. Therefore, good waveforms were obtained by varying temperature, and transistor model parameters. Temperature was changed within the range from 30 °C to +120 °C, and five different transistor models: one typical, and four worst cases (power, speed, zero, one worst cases) were used.

Faulty circuit responses, reflecting faulty behavior of the tested circuit, were obtained by injecting basic MOS transistor faults into the DAC circuit. Following most significant catastrophic faults were used: DOP, SOP (drain open, source open), GDS, GSS, DSS (gate-drain short, gate-source short, drain-source shorts), and GOS (gate-oxide short). The value of the resistors in open fault models was changed within the range from 1 KΩ to 10 MΩ, in GOS faults within the range from 30 KΩ to 150 KΩ, and in short faults they varied from 1 KΩ to 100 KΩ. The faults were injected randomly, always only single fault at a time. As a result, we obtained the total number of 590 I_{OUT} waveforms (90 good, and 500 defective). Examples of good and defective I_{OUT} waveforms, sampled to 32 samples (with 0.25 ns sampling period), are depicted in Figs. 5 and 6, respectively.

3.2. Analog circuit example with parametric faults

In our second experiment, a simple analog integrated circuit, Sallen-key bandpass filter, shown in Fig. 7, has been used as an experimental circuit under test, in order to investigate feasibility of the ANN in identification of different parametric faults. Since parametric faults are associated with passive components only, an active analog filter, most usually consisting of a few such devices and frequently used in IC, has been considered. The filter was excited by a pulse input signal. The output voltage and supply current responses, depicted in Fig. 8, were mathematically preprocessed and analyzed by the neural network consequently. As a result, the analyzed signal was classified by the network to a respective category representing either good or faulty state of the circuit.

Two parametric faults were considered and introduced into the circuit, namely into devices' R1 and C1, where resistance and capacitance values have been varied, respectively. To keep the simulation close to the real chip

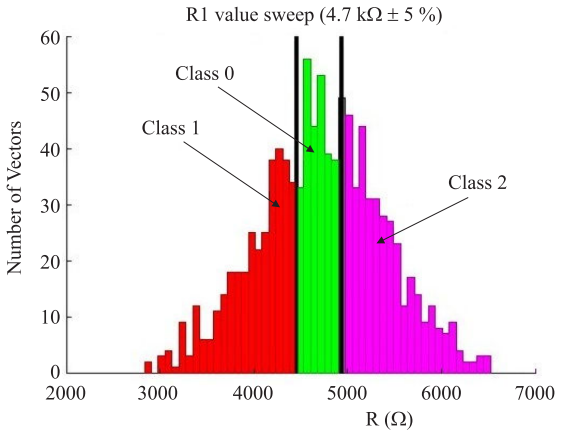

Fig. 9. R1 value histogram with the output classes definition.

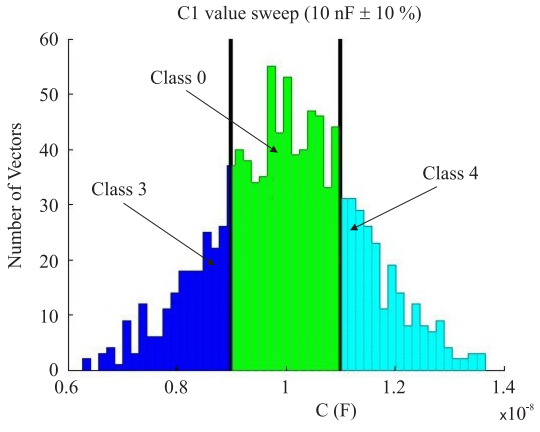

Fig. 10. Considered output classes for C1 value.

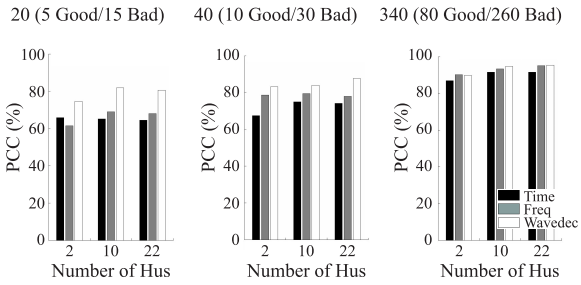

Fig. 11. Percent correct classification (PCC) results for the DAC.

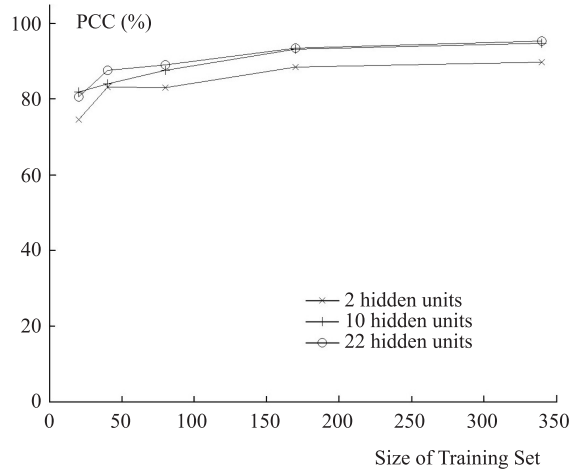

Fig. 12. Classification efficiency for the DAC using wavelet signal decomposition.

conditions, parameter deviations were produced by Gaussian sweeping of the respective parameter value. This approach counts with randomness and probability distribution factors, and the resulting histogram for R1 value and C1 parameter values is depicted in Figs. 9 and 10, respectively. Consequently, the following five output classes have been defined: *class 0* representing good circuits (value of R1 and C1 is within the tolerance range of $\pm 5\,\%$ and $\pm 10\,\%$, respectively), *class 1* representing circuits with the value of $R1 < -5\,\%$ from the reference value, *class 2* for the value of $R1 > +5\,\%$ from the reference value, and *class 3* and *class 4* for the value of C1 outside the range of $\pm 10\,\%$ from the nominal value (Figs. 9 and 10).

4 EXPERIMENTAL RESULTS

Experiment A:

In the first experiment, the efficiency of the approach in detection of catastrophic defects present in the 8-bit DAC has been investigated. The converter output current was selected as the proper parameter analyzed and classified by the neural network. The total number of 590 output current waveforms (90 good, and 500 faulty) was generated. Randomly selected subsets of 20, 40, and 340 patterns formed the network training sets. Figure 11 shows the average percent correct classification (PPC) of the network for the given sizes of the training set, achieved for different signal preprocessing domains. Each bar represents the average defect detection results for ten different network adaptations with a given network topology with 2, 10, and 22 hidden neurons.

The obtained results indicate that a high efficiency of the neural network correct classification can be achieved even for complex mixed-signal circuits if a proper circuit parameter is analyzed, and sufficient training of the network is performed. Wavelet preprocessing of the input signal significantly improves the network performance while its complexity can be reduced. Very high percent correct classification over 90 % for 340 training vectors, and only

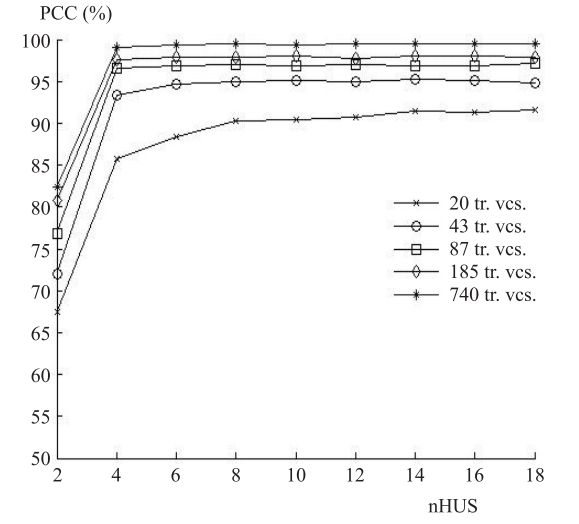

Fig. 13. PCC versus number of hidden neurons (network complexity) for 5 output classes.

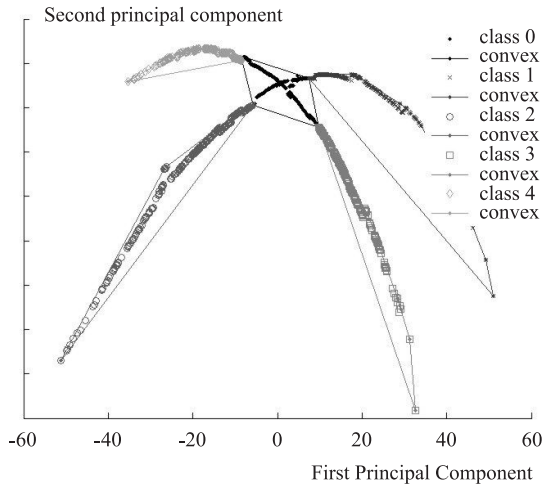

Fig. 14. PCA with 1st versus 2nd principal component plot.

Table 1. Training sets composed of all class vectors.

ANN output category	Training set size				
	20	43	87	185	740
good	8	16	32	75	300
bad (class 1)	4	8	16	32	128
bad (class 2)	4	9	18	36	144
bad (class 3)	2	5	10	20	80
bad (class 4)	2	5	11	22	88

2 hidden units can be achieved. Wavelet decomposition of the signal significantly enhances the network correct classification ability, particularly for small training set sizes (20 vectors). Average defect detection results as a function of the number of training set vectors for wavelet analysis is shown in Fig. 12.

Experiment B:

As it was already mentioned, efficiency of the ANN in covering different parametric faults present in a pure analog circuit has been investigated in the second experiment. The total number of 1869 vectors and several sizes of the training set (20, 43, 87, 185 and 740) have been used. Each training set was composed of both good and bad responses, where the defective subset contained vectors from all defective classes (Tab. 1).

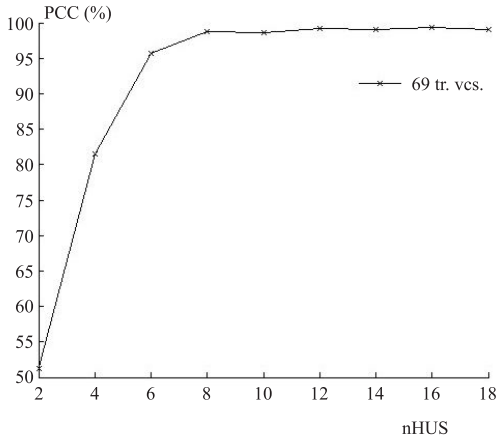

Fig. 15. Correct classification versus network complexity (using PCA data processing).

The results obtained prove the neural network capability to successfully face complicated signal classification problems. Figure 13 shows the classification results obtained for 5 output neurons, where the following output vectors were used for the respective class representation: [1 0 0 0 0], [0 1 0 0 0], [0 0 1 0 0], [0 0 0 1 0], [0 0 0 0 1]. The experimental results show the need for a rather complex network, where the hidden layer size composed of 2 to 4 neurons is not enough to achieve satisfactory level of PCC. The crucial problem is a sophisticated training set selection, since PCC higher than 99 % was achieved for rather large training set sizes over 340 vectors that represents more than 18 % of all classified circuit responses. To solve this problem there are generally two possibilities. One is to move to another domain *eg* frequency domain and use discrete Fourier transformation as a data transform procedure. However, for non-stationary signals Short Time Fourier Transform or Wavelet decomposition can be more useful due to good localization in time property. Another way to the training set minimalization, with still acceptable network classification performance, is to use some feature extraction method to present the data to the neural network from statistical point of view.

Therefore, Principal Component Analysis has been used as a multivariate analysis to reveal the natural structure of data and reduce size of the network training set. Figure 14 shows all circuit responses after applying PCA with first versus second principal component plotted. Resulting convex polygons, displayed with lines represent the ideal training set selected algorithmically using PCA. Each polygon represents *convex hull* for each output class and therefore, it creates the respective class outer border in 2D space.

Total size of the optimal training set determined by PCA algorithm is 69 vectors that represent less than 4 % of the overall 1869 classified responses. This is an excellent result since it proves that PCA can minimize the training set and make the network training process very short while still achieving very high network classification performance. Average PCC results achieved with the mentioned training set selection is shown in Fig. 15. However, the necessity to use more complex neural network (number of neurons in the hidden layer) might be observed. This behavior is due to the input vector dimensionality reduction, which leads to less input neuron connections and therefore, also to fewer variables to iterate for learning algorithms.

5 CONCLUSIONS

An efficient neural network-based test approach to detection both catastrophic physical defects as well as parametric defects in analog and mixed-signal circuits using different methods of digital signal processing is proposed. Two circuit examples have been used to show that artificial neural networks are able to identify defective circuits. Nevertheless, if certain classification efficiency is expected, the network training may be a time consuming job that requires a rather large number of training patters even for small circuits. The results obtained through our experiments prove that preprocessing of the analyzed signal can drastically reduce the number of input patterns applied to the neural network. The presented approach offers the excellent correct classification above 98simple network topology. In our first experiment, the training vectors were selected randomly, and it is important to note that the network effectiveness might be affected by

the improper training process. Therefore, a novel methodology of the optimal training set selection for feed-forward neural networks using PCA and qhull algorithms is proposed. This improvement in the network training and data preprocessing brings significant enhancement in the network correct classification ability since the neural networks categorize the analyzed circuit's response with the excellent accuracy over 99 %.

The results achieved indicate the possibility to use this approach as an effective and flexible test method, especially in analog and mixed-signal testing, where conventional test methods are either insufficient or inapplicable. This is exactly the area where the neural network approach seems to be a good alternative, easily adaptable for an arbitrary circuit parameter (*eg*, output voltage, output current, *etc*). However, in real testing, availability of a sufficient number of training vectors might be a problem. This could be avoided by employing neural network structures able of signal classification without the necessary learning process, *eg* self-organizing maps that will be also subject of our interest in the future.

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