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A NEW MODELLING AND CONTROL ANALYSIS OF AN ADVANCED STATIC VAR COMPENSATOR USING A THREE–LEVEL (NPC) INVERTER TOPOLOGY

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This paper presents a study of the dynamic performance analysis of an Advanced Static Var Compensator (ASVC) using a three-level voltage source inverter. The analysis is based on the modelling of the system in the d-q axis. The dynamic behaviour of the system is analysed using P-spice (Simulation Program with Integrated Circuit Emphasis) as a simulation program. Various transient simulation results are reported and discussed.

K e y w o r d s: P-spice, advanced static var compensator

1 INTRODUCTION

Real and reactive powers on a transmission line in an integrated network are governed by the line impedance, voltage magnitudes, the angle difference at the line ends, and the role the line is playing in maintaining network stability under dynamic contingencies. Power transfer in most integrated transmission systems is constrained by transient stability, voltage stability, and/or power stability. Reactive power (VAR) compensation or control is an essential part in a power system to minimize power transmission losses, to maximize power transmission capability, and to maintain the supply voltage. It is increasingly becoming one of the most economic and effective solutions to both traditional and new problems in power transmissions systems. It is a well-established practice to use reactive power compensation to control the magnitude of the voltage at a particular bus bar in any electric power system. In the past, synchronous condensers, mechanically switched capacitors and inductors, and saturated reactors have been applied to control the system voltage in this manner [1, 2].

Since the late 1960s, thyristor controlled reactor (TCR) devices together with fixed capacitor FC or thyristor switched capacitor (TSC) have been used to inject or absorb reactive power [3, 4].

Series compensation is the control of the equivalent line impedance of a transmission line. The introduction of external components (either capacitive or inductive) is used to change the apparent reactance of the line. The controllable series compensator such as the thyristor controlled series compensation (TCSC) has been developed to change the apparent impedance of a line by either inductive or capacitive compensation, facilitating active power transfer control. The thyristors control the conduction period of the reactor to vary the overall effective impedance of the circuit. The TCSC suffers from the disadvantages that it generates low order harmonic components into the power system. TCSC's are usually connected in series to conventional line series capacitors. They may consist of one or several identical modules. Each module has a small thyristor controlled reactor in parallel to the segment series capacitor. Although the TCSC is primarily used for regulating the power flow through varying its effective reactance inserted in series with the transmission line, it may also be used for voltage stabilization. In this case, the output reads the terminal voltage within a tight band. Recently, voltage source converters using GTO thyristor have been developed to operate as static VAR compensators [5–7]. These converters are known as ASVC. Such converters may resemble the operation of synchronous condensers but in a static manner. For these devices, a converter transformer is always needed to complement the function of the power electronic switches to perform system VAR compensation and may also be used to connect the device to the high voltage bus. The converter supplies reactive power to the network by increasing the synthesized inverter output voltage. Similarly, the ASVC absorbs VARs from the network by reducing the output voltage below the network voltage, *ie*, no large power components such as capacitor banks or reactors are used. Only a small capacitor is employed to provide the required reference voltage level to the inverter. In contrast to the TCR/FC or TCR/TSC schemes bulky and expensive passive elements are not required. The possibility of PWM voltage source converters with a high switching frequency for reactive power compensation has also been reported [8, 9]. However, the high switching frequency operation of GTO is not available. Recently, in order to apply large-scale reactive power compensation, new SVC systems with a low switching frequency PWM operation have been reported [10–12]. The conventional GTO inverters have a limitation of their dc link voltage about 2 kV. Hence, the series connections of the existing GTO thyristors have been essential in realizing high voltage about 4 kV. So there have been great interests in the multilevel level inverter topology, which can overcome the series connection problems.

Recently, the multilevel pulse width modulation converter topology has drawn tremendous interest in the power industry since it can easily provide the high power required for high power applications for such uses as static

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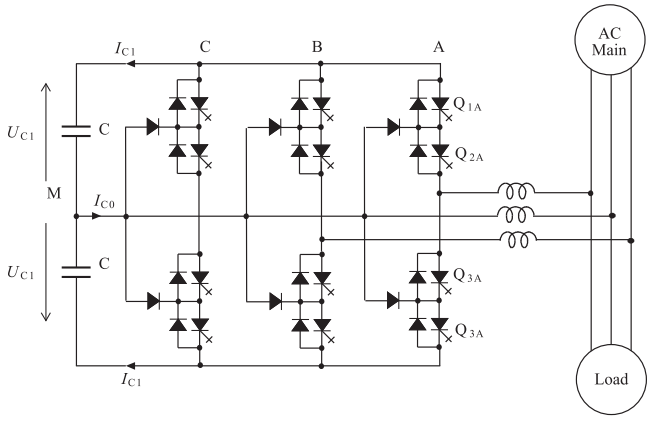

Fig. 1. Power circuit of the ASVC.

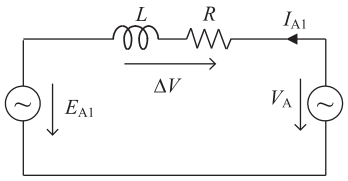

Fig. 2. Per-phase fundamental equivalent circuit.

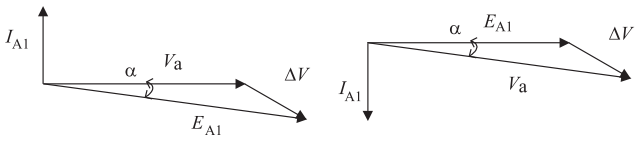

Fig. 3. Phasor diagram for leading and lagging mode.

VAR compensation, active power filters, and the control of large motors by high power adjustable frequency drives.

The most popular structure proposed as a transformerless voltage source inverter is the diode clamped converter based on the neutral point clamped (NPC) converter proposed by Nabae [13]. It has the advantages that the blocking voltage of each switching device is one half of dc link voltage and the harmonics contents output voltages are far less than those of a two-level inverter at the same switching frequency. Each alternative has its technical and economical advantages, limitations, and drawbacks, and it is the scope of this paper to present the modelling and analysis of this new type of inverter used for static VAR compensation.

The main purposes of the paper are not only to illustrate the model of the ASVC using N.P.C inverter, but also to describe the closed loop reactive power controller design. Finally, the P-spice implementation of ASVC model is included as well as some simulation results under various transient conditions of the proposed ASVC model and its control.

2 OPERATING PRINCIPLE

The static VAR compensator (ASVC) which uses a three-level converter of the voltage source type is shown in Fig. 1. The main circuit consists of a bridge inverter made up of twelve power GTO's with antiparallel diodes, which is connected to the three-phase supply through a reactor X of small value. Two capacitors are connected to the dc side of the converter. The structure of one leg of the inverter itself is made up of four pairs of diode-GTO forming a switch and two diodes allowing to have the zero level point of the inverter output voltage.

The operation principles of the system can be explained by considering the per-phase fundamental equivalent circuit of the ASVC system as shown in Fig. 2. In this figure, E_{a1} is the ac mains voltage source. I_{a1} and V_a are the fundamentals components of current and output voltage of the inverter supply respectively. The ASVC is connected to the AC mains through a reactor L and a resistor R representing the total loss in the inverter. As shown in Fig. 3, by controlling the phase angle α of the inverter output voltage, the dc capacitor voltage U_c can be changed. Thus, the amplitude of the fundamental component E_{a1} can be controlled.

3 MATHEMATICAL MODEL OF THE ASVC [14]

Figure 4 shows a simplified equivalent circuit of the ASVC. Using matrix form, the mathematical model is given by:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_a - e_a \\ v_b - e_b \\ v_c - e_c \end{bmatrix} \quad (1)$$

The model of the inverter output voltage is given by

$$\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \left\{ \begin{bmatrix} S_{1A}S_{2A} \\ S_{1B}S_{2B} \\ S_{1C}S_{2C} \end{bmatrix} U_{c1} - \begin{bmatrix} S_{3A}S_{4A} \\ S_{3B}S_{4B} \\ S_{3C}S_{4C} \end{bmatrix} U_{c2} \right\}. \quad (2)$$

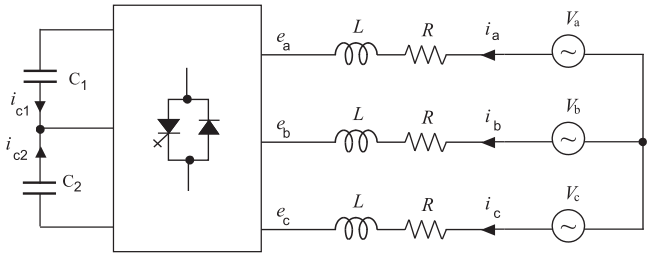

Fig. 4. Equivalent circuit of the ASVC

With:

S_{ki} : The switching function, is either 1 or 0 corresponding to on and off states of the switch Q_{ki} respectively.

K : Names of arms (A, B ,C).

i : number of switches of one arm ($i = 1, 2, 3, 4$)

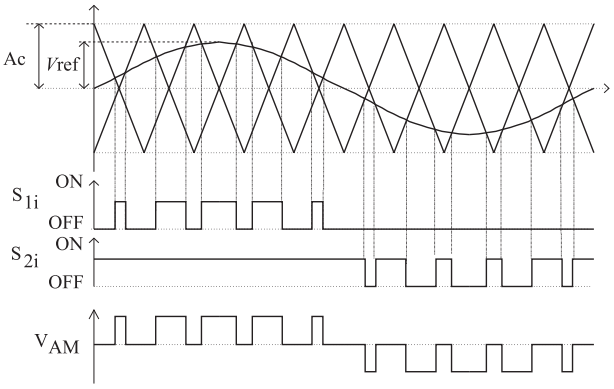

Fig. 5. Three-level PWM

The DC side currents are given by

$$\begin{aligned} I_{C1} &= S_{1A}S_{2A}i_A + S_{1B}S_{2B}i_B + S_{1C}S_{2C}i_C \\ I_{C2} &= S_{3A}S_{4A}i_A + S_{3B}S_{4B}i_B + S_{3C}S_{4C}i_C \end{aligned} \tag{3}$$

$$I_{C0} = I_{C1} + I_{C2} \tag{4}$$

and the DC side capacitor voltages are given by

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} U_{C1} \\ U_{C2} \end{bmatrix} = \frac{1}{C}\begin{bmatrix} I_{C1} \\ I_{C2} \end{bmatrix}. \tag{5}$$

The dynamic model of the power circuit of an ASVC in the abc reference frame is given by equations (1) to (5).

3.1 DQ Frame

Park's transformation matrix (6) is used to develop the time-invariant form in a two-axis (d-q-o) rotating reference frame under the following assumptions:

- all switches are ideal,
- the source voltages are balanced,
- the total losses in the inverter are represented by lumped resistor R,
- the total harmonic contents caused by switching action are negligible.

$$P = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\omega t+\alpha) & \cos\left(\omega t - \frac{2\pi}{3} + \alpha\right) & \cos\left(\omega t + \frac{2\pi}{3} + \alpha\right) \\ \sin(\omega t+\alpha) & \sin\left(\omega t - \frac{2\pi}{3} + \alpha\right) & \sin\left(\omega t + \frac{2\pi}{3} + \alpha\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \tag{6}$$

Thus we write equation (7)

$$\begin{aligned} U_{c1} &= U_{c2} = U_c \\ I_{c1} &= I_{c2} = I_c \end{aligned} \tag{7}$$

The AC mains voltage is defined by (8)

$$V_{ABC} = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \sqrt{\frac{2}{3}}V_L \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 2\pi/3) \\ \sin(\omega t + 2\pi/3) \end{bmatrix} \tag{8}$$

where V_L is the rms line voltage.

Equation (9) gives the inverter voltage.

$$E_{ABC} = \begin{bmatrix} e_A \\ e_B \\ e_c \end{bmatrix} = FU_c \tag{9}$$

F is the commutation function defined by equation (10)

$$F = \sqrt{\frac{2}{3}}D \begin{bmatrix} \sin(\omega t+\alpha) \\ \sin(\omega t - 2\pi/3 + \alpha) \\ \sin(\omega t + 2\pi/3 + \alpha) \end{bmatrix} \tag{10}$$

$$IM = \sqrt{2/3}D \tag{11}$$

D is the modulation index in the Park axis. The voltage supply equation in the dq frame is given by (12)

$$V_{qd0} = PV_{ABC} = V_L \begin{bmatrix} -\sin\alpha \\ \cos\alpha \\ 0 \end{bmatrix} \tag{12}$$

and for the inverter voltage we obtain

$$E_{qd0} = PE_{ABC} = \begin{bmatrix} 0 \\ D \\ 0 \end{bmatrix} U_C \tag{13}$$

Equation (1) transformed in dq frame gives equation (15)

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} R/L & -\omega \\ \omega & R/L \end{bmatrix}\begin{bmatrix} i_q \\ i_d \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_q - e_q \\ v_d - e_d \end{bmatrix}. \tag{14}$$

Substituting equations (12) and (13) in (14) we get

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} R/L & -\omega \\ \omega & R/L \end{bmatrix}\begin{bmatrix} i_q \\ i_d \end{bmatrix} + \frac{1}{L}\begin{bmatrix} -V_L\sin\alpha \\ V_L\cos\alpha - DU_C \end{bmatrix}. \tag{15}$$

For the DC side of the inverter we may get the following equations. The DC current is given by

$$I_{c1} + I_{c2} = 2I_c = Fi_{abc} \tag{16}$$

and

$$i_{abc} = P^{-1}i_{qdo} = P^{\top}i_{qdo} \tag{17}$$

$$2I_c = F^{\top}P^{-\top}i_{qdo} = \begin{bmatrix} 0 & D & 0 \end{bmatrix}\begin{bmatrix} i_q \\ i_d \\ i_o \end{bmatrix} = Di_d. \tag{18}$$

The capacitors voltages are given by:

$$\frac{\mathrm{d}U_C}{\mathrm{d}t} = \frac{i_C}{C} \tag{19}$$

combining equations (19) and (20) we get (21)

$$\frac{\mathrm{d}U_C}{\mathrm{d}t} = \frac{Di_d}{2C} \tag{20}$$

and the reactive power delivered by ASVC is given by the relation (21) in the DQ Frame:

$$Q_c = V_q i_d - V_d i_q. \tag{21}$$

Combining all equations we obtain

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_q \\ i_d \\ U_c \end{bmatrix} = \begin{bmatrix} -R/L & -\omega & 0 \\ \omega & -R/L & -D/L \\ 0 & D/2C & 0 \end{bmatrix}\begin{bmatrix} i_q \\ i_d \\ U_c \end{bmatrix} + \frac{1}{L}\begin{bmatrix} -V_L\sin\alpha \\ V_L\cos\alpha \\ 0 \end{bmatrix}. \tag{22}$$

In equation (22) the control parameter α is defined in the form of $\sin\alpha$ and $\cos\alpha$. Thus the system is nonlinear. In the next section we establish a linear model.

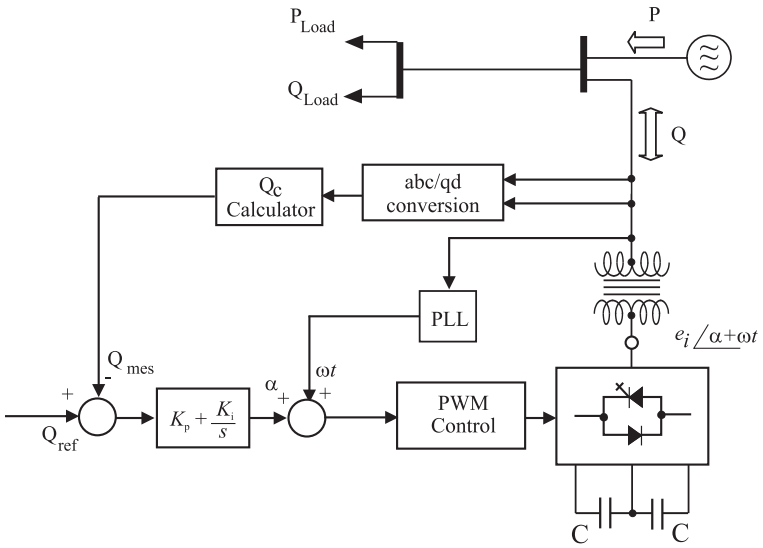

Fig. 6. Main circuit and control block diagram.

3.2 Linear model

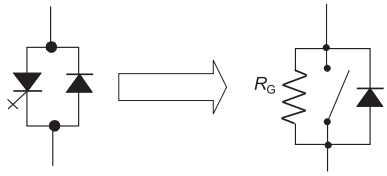

Fig. 7. Simplified Pspice model of a switch and its antiparallel diodes.

To achieve an easier design of the control, equations (22) must be linearized under the following assumptions.

- Disturbance $\Delta\alpha$ is small.
- The second-order terms are dropped.
- The quiescent operating αo is near zero.

The annotation Δ is introduced to indicate disturbed values.

Equations (23) to (27) are substituted in equation (22)

$$i_q = i_{qo} + \Delta i_q \tag{23}$$

$$i_d = i_{do} + \Delta i_d \tag{24}$$

$$U_C = U_{CO} + \Delta U_C \tag{25}$$

$$\alpha = \alpha_O + \Delta\alpha \tag{26}$$

$$Q_c = Q_{co} + \Delta Q_c \tag{27}$$

we obtain equation (28) in the state space.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\Delta i_{qo}\\ \Delta i_{do}\\ \Delta U_{co}\end{bmatrix} = \begin{bmatrix}R/L & -\omega & 0\\ \omega & R/L & D/L\\ 0 & D/2C & 0\end{bmatrix}\begin{bmatrix}\Delta i_{qo}\\ \Delta i_{do}\\ \Delta U_{co}\end{bmatrix} + \frac{1}{L}\begin{bmatrix}V_L\\ 0\\ 0\end{bmatrix}\Delta\alpha \tag{28}$$

$$\Delta Q_c = [\,-V_L \quad 0 \quad 0\,]\begin{bmatrix}\Delta i_{qo}\\ \Delta i_{do}\\ \Delta U_{co}\end{bmatrix}$$

3.3 Regulator synthesis

From equation (28) we calculate the transfer function of the system equation (29).

$$G(s) = \frac{\Delta Q_C(s)}{\Delta\alpha(s)} = \frac{A(s)}{B(s)}\,,$$

$$A(s) = \frac{V_L^2}{L}\left[s^2 + \frac{R}{L}s + \frac{D^2}{2LC}\right], \tag{29}$$

$$B(s) = s^3 + \frac{2R}{L}s^2 + \left\{\left[\frac{R}{L}\right]^2 + \frac{D^2}{2LC} + \omega^2\right\}s + \frac{D^2R}{2L^2C}\,.$$

The ASVC control scheme is illustrated in the block diagram of Fig. 5. First, a conventional PI controller is used to study the dynamic behaviour of the system [15].

3.4 PWM three-level control strategy

Figure 6 shows the triangular-sinusoidal control used in this work [16]. We used the following signals.

- The reference signals V_{ref},
- The Triangular carrier V_A,

and the gates signals, V_{AM} phase A voltage to middle point of capacitors. The switching signals patterns are generated in this manner:

FOR k =A, B ,C DO
  If (vref (k) > 0) and (vref (k) ≥ Vc)
    Then $Sk1 = 1,\ Sk2 = 1,\ Sk3 = 0,\ Sk4 = 0.$
  Elseif (vref (k) ?0) and (vref (k) ? VA)
    Then $Sk1 = 0,\ Sk2 = 0,\ Sk3 = 1,\ Sk4 = 1.$
  Else $Sk1 = 0,\ Sk2 = 1,\ Sk3 = 1,\ Sk4 = 0$
End DO

4 P–SPICE MODELLING

We have chosen to model the GTO in a simplified form, resistor with a big value if the GTO is OFF and a small value if GTO is ON. This pinciple is illustrated in Fig. 7 [17]. Figure 8 shows the PWM generating method of gate signals, and Fig. 9 shows this circuit transformed under P-spice.

The schemes of Figs 1 and 9 are used to establish a P-spice program (using Microsim Evaluation Version 6.0) of the power circuit and control circuit, respectively.

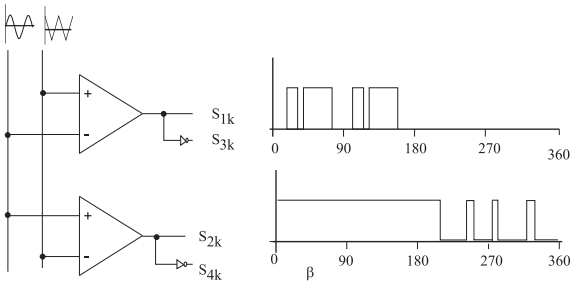

Fig. 8. PWM generator circuit.

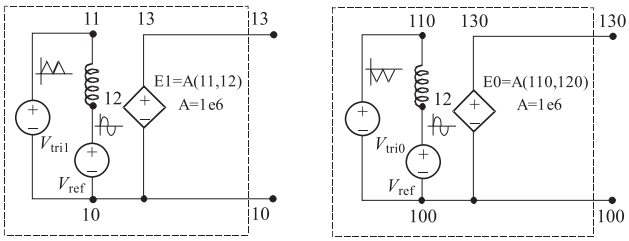

Fig. 9. Scheme circuit of PWM generator under Pspice.

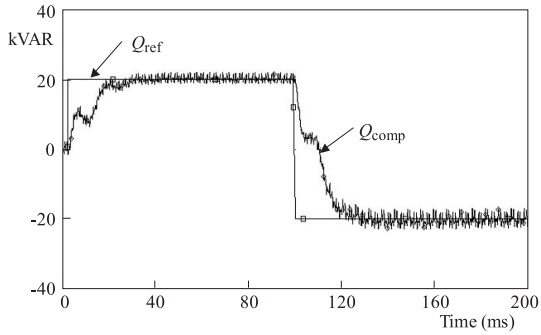

Fig. 10. Simulated reactive power response.

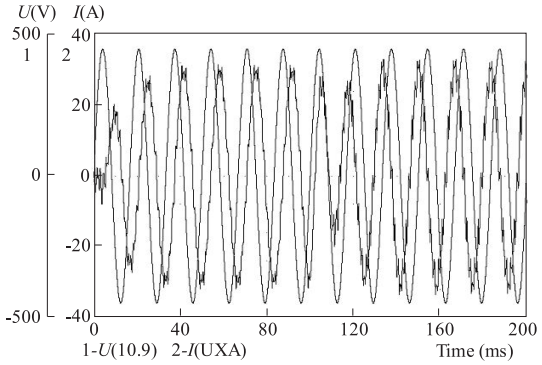

Fig. 11. Simulated current and voltage waveforms.

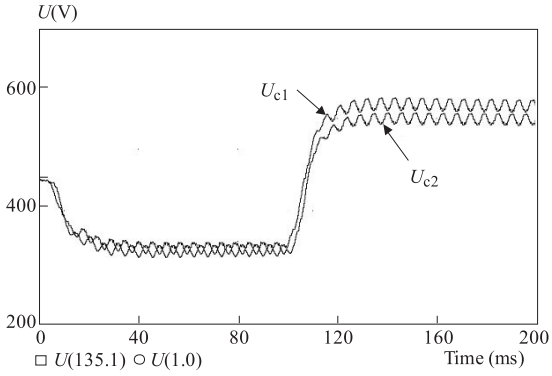

Fig. 12. Simulated inverter DC Bus voltage.

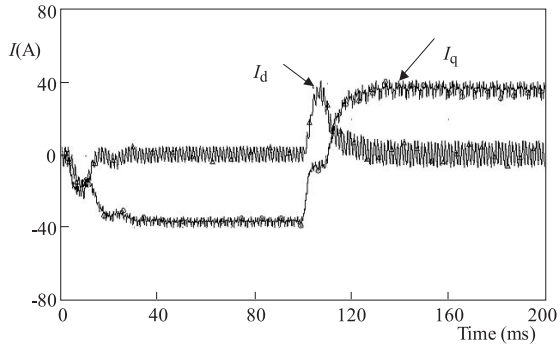

Fig. 13. Simulated inverter current in dq frame.

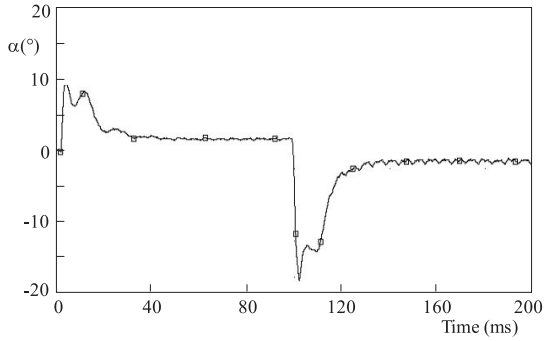

Fig. 14. Variation of the control angle α $(^\circ)$.

5 SIMULATION RESULTS

To check the validity of the model described above a set of simulation tests have been carried out to analyse the system under steady state and transient conditions using P-spice. Computer simulation is carried out using the system parameters given by [17]: $f = 60$ Hz, $W = 2\pi f$, $V_L = 550$ V, $R = 0.4\,\Omega$, $L = 10$ mH, $C = 1000\,\mu$F, MI (Modulation Index)=1.2.

Based on the linear model described above and using root locus technique the parameters of the controller are found to be [15]. $K_p = 10^{-5}$, $K_i = 1.7 \times 10^{-4}$. The amplitude of the reference was adjusted to cause the system to swing from lagging mode to leading mode.

Figure 10 shows the simulated reactive power delivered by ASVC due to a reference change from 20 kVAR lagging to 20 kVAR leading. Figure 11 shows the simulated current and voltage waveforms to step reference of reactive power. The DC side response to the same change is depicted on Fig. 12 we notice a fluctuation of voltages U_{c1} and U_{c2} around an average value. The ASVC currents in the dq frame are represented in Fig. 13. Figure 14 shows the waveform of the control parameter α delivered by the regulator PI.

6 CONCLUSION

A study and mathematical modelling of the dynamic performance analysis of an Advanced Static Var Compensator (ASVC) using three-level voltage source inverter has been presented in this paper. The dynamic behaviour of the system was analysed using P-spice through a set of simulation tests which have lead to the design of an inexpensive controller for reactive power applications. From the results of the simulations and the mathematical modelling developed in this paper, we have directed our future research work to add time domain voltage source model of arc furnace. This may lead to design a faster and robust control to reduce VAR caused by the rapid variation in the arc furnace current.

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