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EFFICIENCY EVALUATION OF VARIOUS TEST STRATEGIES ON A MIXED–SIGNAL CIRCUIT

Juraj Brenkuš [*] — **Viera Stopjaková** [*]
Ronny Vanhooren [**] — **Anton Chichkov** [**]

In this paper, an analysis comparing the efficiency of different test strategies on a moderate complexity mixed- signal circuit is presented. Selected test strategies from the groups of functional, structural and parametric approaches were applied for the circuit test while considering bridging faults introduced into the circuit layout. The faults were extracted from the layout of the circuit. Fault simulation results are shown, where fault coverage, efficiency and quality of the respective test methods have been evaluated. Results show that the parametric and structural approaches are offering higher test quality (fault coverage, multiple and unique detections, test time) than the functional approach. In addition, the functional approach requires a rather complicated test setup. A short discussion on the possible benefits of a DfT deployment is also given.

K e y w o r d s: analog test; mixed-signal test; fault simulations; bridging faults

1 INTRODUCTION

Effective test procedures are the necessary part of any high-quality manufacturing process. Errors in manufacturing can result in the production of defective units, which need to be discarded. The primary goal of testing is to determine whether the units produced by the manufacturing process are defect-free and will function as desired. The second important goal is to generate information that could possibly improve process yield and help reduce overall production costs [1]. A perfect test process should detect all defective units and pass all acceptable units.

In the case of digital integrated circuits (ICs), there are many well known and industrially established efficient test techniques. These are mostly based on the widely accepted stuck-at fault model [2–10]. Also the test generation and the test vector set preparation process have a substantial Computer Aided Design and Computer Aided Test (CAD/CAT) support.

Analog circuits are somehow more difficult to test. This difficulty arises from the absence of a widely accepted fault model, broad variety of building blocks and unique specifications. In mixed-signal ICs, where analog circuits are integrated together with digital ones, testing is even more difficult because of the limited access to both analog and digital blocks. Analog test is mainly based on checking the circuit's functional specifications what results to long, and thus, expensive test. Such a test approach is not affording a way to define a general test methodology applicable to all analog building blocks.

Encouraged by the success of the structural and fault-driven test methods of digital ICs, the researchers have tried to deploy these techniques to analog test as well. Some Built-in Self-Test (BIST) schemes have been proposed and successfully applied [11–17]. These were mostly aiming on-chip test pattern generation and evaluation, core isolation and accessibility enhancement. On the other hand, such a solution requires chip area overhead, can degrade performance, and increase noise in the circuit. As a consequence, these solutions are not widely accepted among analog designers. Structural and parametric test methods gained more acceptance in the industry. From these test methods, thermal testing [18], the oscillation-based test [19–24], and the IDDT [25–28] gained more attention in the latest years.

The growth in interest has been motivated by advances in integrated circuit (IC) manufacturing technology and by economic factors (overall production costs). ICs with digital, analog and mixed-signal circuits on the same substrate have become rather common recently. The applications of such ICs include wireless communication, networking, multimedia, process-control and real-time control systems. In many cases, integrated systems consist of digital cores surrounded by peripheral analog circuitry, such as filters and data converters. The analog and mixed-signal components serve as interfaces between digital processing circuitry and the real-world analog signals. The analog components usually occupy a much smaller silicon area than their digital counterparts.

As discussed above, analog and mixed-signal circuits will not necessarily occupy a large fraction of the silicon area in ICs. However, without an effective CAD support, the analog and mixed-signal components will consume test resources and force test costs completely out of proportion to their size. Conversely, without adequate test, the analog and mixed-signal components may lead to unacceptable product failure and yield losses. Hence, there is a strong economic motivation to advance analog and mixed-signal IC test.

[*] Slovak University of Technology, Department of Microelectronics, Ilkovičova 3, 812 19 Bratislava, Slovakia, juraj.brenkus@stuba.sk
[**] ON Semiconductor, Test Methodology Team, Westerring 15, Oudenaarde B-9700, Belgium, ronny.vanhooren@onsemi.com

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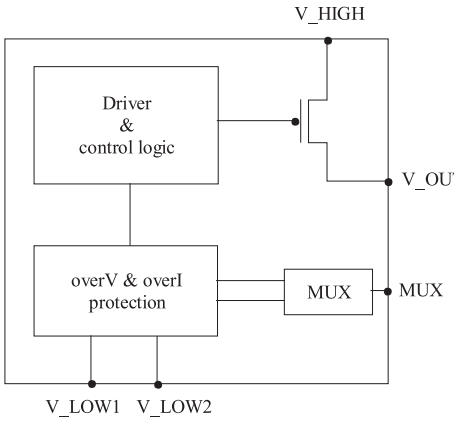

Fig. 1. Block diagram of the CUT.

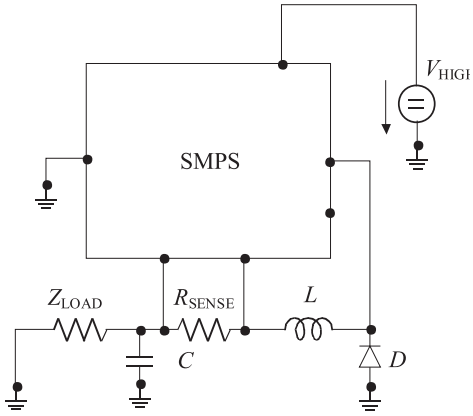

Fig. 2. Configuration used for the functional test application and evaluation.

2 MOTIVATION AND GOALS

As can be seen, although the analog part of a complex mixed-signal circuit might not necessarily constitute a large part of the system, it can significantly influence the overall test cost. Thus, it is inevitable to have a high quality, effective test procedure for the production environment. There is a wide variety of analog/mixed-signal test approaches available, like oscillation test method, current monitoring, BIST, and many others. Those methods can be characterized as functional, structural or parametric. However, none of them is, generally, applicable to all analog/mixed-signal circuits, since all the test methods have some, more or less severe, limitations. In most of the real-world test solutions, more than one type of test are used, *eg* a structural test is supported by some parametric test(s). Usually, up to a certain point, the more different tests are applied, the more information can be obtained about the circuit under test (CUT). Then, the amount of test to be used is determined by the quality and reliability required by the customer. To build up an effective test procedure, one should know which faults is a specific test able to detect, and how (time) expensive and robust this test is.

To obtain these data, it is necessary to conduct a study based on fault simulations and supported by the experience of test engineers and designers. Normally, such an approach is not affordable, so the fault simulations, since they are time-expensive, are excluded and the test procedure is then based on the experience of the designers and test engineers. With such an approach one can just guess the fault coverage (FC) of the selected test.

All this led us to the idea of comparing the efficiency of some test strategies obtained by fault simulations on a mixed-signal circuit. Instead of a standard set of benchmark circuits with complexity of several tens of nodes [29] we decided to use a moderate complexity mixed-signal circuit with 1300 nodes as the experimental CUT. Our intention was to evaluate the fault coverage, efficiency and added value brought by some selected tests from the groups of available functional, structural and parametric test approaches.

3 EXPERIMENT DESCRIPTION

3.1 The test vehicle

The CUT selected for this experiment was a Switched Mode Power Supply (SMPS) with a complexity of 1300 nodes. This circuit was designed for a high-voltage 0.35 μm CMOS process. The block diagram of this circuit is shown in Figure 1. The analog part, consisting of the over-voltage and over-current protection circuits and the power switch with the driver represents 85 % of the overall design. The rest is taken by the control logic.

However, since the selected circuit under test represents only a fraction of a more complex mixed-signal system (5 % of the overall chip area), it was not possible to fully isolate it for the test purposes, and thus, make it fully stand-alone and independent circuitry during test. The accessibility of the circuit was ensured by five pins (GND excluded). From these pins, one was exclusively dedicated to test mode (MUX) where the output of the over-voltage or over-current protection could be observed.

3.2 Fault list extraction

The starting point for the necessary fault simulations was the fault list extraction from the circuit layout. Faults considered and targeted in this experiment were bridging faults on the metallization layers, since they are the most common for the respective technology node. This is due to the fact that the metallization, as for the majority of CMOS processes, is aluminum-based. Bridging faults can be divided into several classes based on the location of the physical defect, *eg* between parallel metal lines, corners of two metal lines, vias, etc. In our case, only the bridges occurring between two parallel metal lines were considered, since they constitute the biggest bridging fault class.

In order to extract the fault list, parasitic devices (representing the bridging fault model) were introduced into the layout with the desired length, and the overlapping areas between the introduced parasitic devices and the

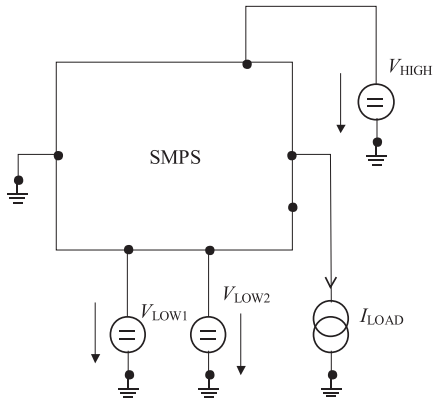

Fig. 3. Test setup for the switch R_{ON} measurement.

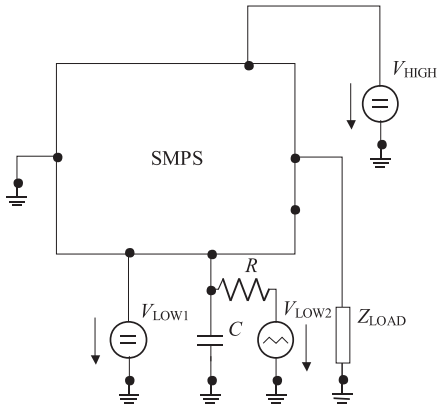

Fig. 4. Test setup for the switching point measurement.

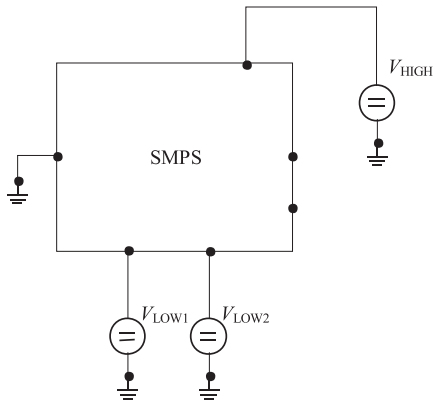

Fig. 5. Test setup for I_{DDQ} measurement.

metallization were examined. Thus, the size of the overlapping area has also created a weight, based on which the bridging faults were ordered in the fault list. Two different dimensions (lengths) of the physical defect were considered: 0.8 μm and 1.6 μm. The bottom limit for the defect width was set to 0.7 μm, thus creating quite exhaustive fault list.

3.3 Test methods considered

The primary goal of the experiment was to evaluate the fault coverage, efficiency and the benefits of various test techniques. Since there are a broad variety of tests available, we decided to pick only one representative from each of the groups of functional, structural and parametric test approaches.

The functional test approach was based on recommended operating and functional conditions according to the circuit data sheet. The circuit functional test setup is shown in Figure 2, and it represents the normal operational mode of the device under test.

The evaluated parameter was the average value of V_{LOW} voltage measured for two different loading conditions. The structural test consisted of a set of measurements that were targeting certain building blocks of the CUT. The first measured parameter was the on-resistance of the power PMOS device (see Figure 3). During this test, a certain current was drawn through the switch, and the resulting voltage drop across the device was measured.

The second structural test was targeting the switching point of the over-current protection circuit. During this test the voltage difference between the inputs V_LOW1 and V_LOW2 at which the over-current protection switches off the circuit was measured (see Figure 4). Then, from the known value of the sensing resistor RSENSE (see Figure 1) we can calculate the threshold current using Ohm's law. During the third structural test, two parameters were measured. Firstly, the switching point of the over-voltage comparator was measured, secondly, the delay from the input of the comparator to the V_{OUT} node was measured. From these two parameters, the V_{LOW} voltage for normal operational conditions was calculated.

As the representative of the parametric test approach, I_{DDQ} testing was selected, applied and evaluated. This test method represents a simple quiescent current consumption measurement. Since the CUT uses three different power supply voltages (V_{HIGH}, V_{LOW1} and V_{LOW2}), the intention was to separately measure the consumption from each (see Figure 5). However, one of the supply paths, namely V_{LOW1}, could not be satisfactory isolated from the rest of the chip because of a common supply pin with the rest of the chip and no DfT present in the circuit. Since the rest of the chip represented a huge 'background noise', we excluded this supply path from our measurements. This test was performed for three different operational conditions of the CUT:

i over-voltage protection is inactive, over-current protection is inactive;

ii over-voltage protection is active, over-current protection is inactive;

iii over-voltage protection is inactive, over-current protection is active;

Fault simulations for all of the test approaches mentioned above were performed for four different values of the V_{HIGH} supply voltage, varying from 12 V to 72 V. The decision criteria, distinguishing between a fault-free and a defective circuit, for the functional as well as for

the structural test approaches were taken from the circuit specifications. For the parametric approach, the decision criteria were determined by the corner analysis of the fault-free circuit where the process fluctuations were taken into account. Based on the results of these simulations the decision criteria for the quiescent current evaluation were set. Taken into account that none of the supply currents showed variation from its nominal value greater than $\pm 26\,\%$ for any of the corners, we decided to set the decision criteria to $\pm 50\,\%$ of the nominal value for each of the supply currents. The simulations were conducted in CADENCE design environment using SpectreS simulator.

3.4 Fault simulations

Our primary focus was on bridging faults, since this fault group is the major yield killer for this particular circuit under test. The fault model for the defect used in the fault simulations was based on Failure Analysis (FA) data. From these data we have seen that if an undesired bridging fault occurred, it was typically a low-ohmic one with a bridging resistance value in the range from $100\,\Omega$ to $500\,\Omega$. Based on this knowledge, we decided to model the bridging faults as a simple resistor with the resistance value of $1\,\mathrm{k}\Omega$. In the experiment, only one fault at-a-time was considered and injected into the circuit, and then fault simulations for all the test approaches were performed. Results were gathered, processed, and the analyzed parameter values were calculated. Consequently, these values were compared to the decision criteria. To each measurement a PASS/FAIL signature was assigned.

4 EVALUATION RESULTS

4.1 Fault Coverage

Fault coverage (FC) is one of the most important parameters describing the quality of a particular test (mostly its efficiency). It puts the group of faults detected by the test and the group of all the considered (possible) faults into a ratio. The mathematical representation is as follows

$$FC = \frac{FD}{FD + FN} \times 100 \tag{1}$$

where FC is the fault coverage in percents, FD refers to the group of detected faults, and FN represents the group of non-detected faults.

Thus, the fault coverage was the first qualitative feature of the considered test methods to be evaluated in this experiment.

The fault coverage values obtained for the respective tests are shown in Table 1. As can be seen from this table, the approach offering the best fault coverage is the parametric test, while the structural approach is offering nearly the same FC. The functional approach seems to be the less efficient in detecting considered faults. More detailed visualization of these results is observable in Figure 6, where the well known Venn diagram, obtained for our experiment, can be found. As can be seen from this diagram, $34.47\,\%$ of the considered faults were not detected by any of the approaches taken into account. Furthermore, the highest fault coverage (FC) of $56.81\,\%$ ($40.78 + 9.71 + 5.83 + 0.49$) was achieved by the parametric (I_{DDQ}) approach, while offering $5.83\,\%$ of unique detections, *ie* detections of faults that were not detected by any other of the considered approaches. On the other hand, the lowest fault coverage of $45.63\,\%$ was achieved by the traditional functional test.

4.2 Test efficiency

Another important parameter describing a particular test is the time needed to execute such a test. The less time it takes to run the test, the cheaper the test is (from the tester usage time point of view). Now, let us compare the considered tests taking into account the test time factor. Since the parametric test is the fastest one, we decided to use the time of this test method as the reference and call it 1 time unit ($1\,\mathrm{t.u.}$). Results of this comparing evaluation are shown in Table 1 too. One can see that from the test time point of view, again the functional test seems to be the less efficient. To come up with a little bit more exact evaluation of the time efficiency of different tests, the fault coverage of the tests has been also taken into account. In that way, we get a parameter that is describing detections per test time (DTT), which can be expressed by the following equation

$$DTT = \frac{FC}{TT}\,, \tag{2}$$

where FC is the fault coverage, and TT is the time necessary to execute the test. For the comparison between different approaches, we used the above mentioned time units instead of the time, and set the DTT of the parametric test as the reference value, *ie* we divided the equation by the FC of the parametric test, thus obtaining a relative DTT. The resulting values are shown in Table 1. Since the differences in the FCs are not substantial, the calculated values of DTT are mainly determined by the test time.

4.3 Quality of the test

For each of the approaches we have also evaluated unique detections (UD) and multiple detections (MD). These detections are creating a measure on the quality and necessity of the given test. If a particular fault is targeted by more than one test, the probability of its detection is higher. This gives a higher quality mark to the given test approach.

Obtained unique detections and multiple detections for each of the test approaches assumed in this experiment are also shown in Table 1. A fault was assumed to be detected multiple times, if at least two different measurements were detecting the given fault. As can be seen from this table, the functional test for this circuit is

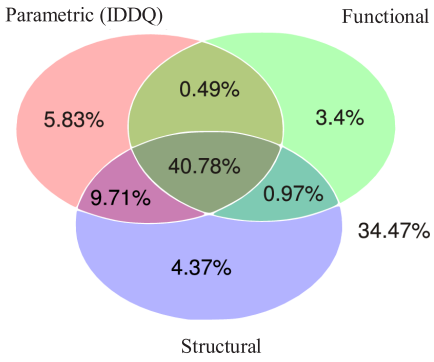

Fig. 6. Fault coverage of particular test approaches.

Table 1. Summarized results for particular approaches

	FC [%]	MD [%]	UD [%]	Time [t.u.]	DTT_rel
Functional	45.63	0	3.4	400	0.002
Structural	55.83	28.15	4.37	40	0.025
Parametric	56.8	28.15	5.83	1	1

Table 2. Additional possible detections

FC [%]	Bridging resistance [Ω]			
	$1k$	500	200	100
Functional	0	0.49 %	1.46 %	2.43 %
Structural	0	0.49 %	1.46 %	2.43 %
I_{DDQ}	0	0	0.97 %	1.94 %
I_{DDQ} + DfT	11.65 %	11.65 %	11.65 %	11.65 %

not offering any multiple detections, since it contains one measurement only.

Accuracy and repeatability are also determining the quality of a test. However, these measures were not evaluated in this experiment, since they cannot be evaluated by simulations only. These factors are closely related to the robustness of the measurement method and some setup related issues (like complexity and stability). From the three approaches taken into account in this experiment, the most complicated measurement setup needed was for the functional approach, while the structural and the parametric approaches were characterized by rather simple setup and fast measurements.

4.4 Further investigations

After the detailed analysis of the obtained results, we decided to perform further evaluations. Our intention was to investigate two issues:

1. What would be the additional fault coverage offered by IDDQ testing if we would be able to disconnect the load (the rest of the chip)?
2. Could non-detected faults become detectable if a lower value of bridging resistance is considered?

Answers to those questions can be given by results obtained from the further simulations. Obtained results are summarized in Table 2, where other possible FC values can be observed.

As can be seen from Table 2, by the possibility of isolation of all the supply paths (I_{DDQ} + DfT), the fault coverage of the parametric approach could be enhanced by more than 11 %, thus yielding a fault coverage of more than 68 % (56.8 % + 11.65 %). This represents an overhead of more than 20 % in coverage over the functional test. In addition, the parametric test is much faster than the functional one (≈ 100 times), and also have a higher quality ranking in means of multiple detections (see Table 1).

Table 2 also shows the results for the second problem, whether the bridges would become detectable with a lower values of bridging resistance used in the respective fault model. The simulations were conducted for resistance values of 500, 200 and 100 ohms. The results prove our prediction that some faults could become detectable under such conditions. Anyhow, those additional possible detections are representing only a fraction of all the considered faults.

4.5 DfT improvement

As can be seen from the simulation results shown above, fault coverage, and thus, efficiency of the evaluated methods could be improved by introducing some DfT solutions into the tested circuitry. More precisely, by the isolation of V_LOW1 power supply path from the rest of the chip, the fault coverage could be enhanced by more than 11% up to 68 %. Such a fault coverage is achievable when the parametric (I_{DDQ}) approach is deployed (see Table 2). The block diagram of the respective DfT solution, providing such functionality, is depicted in Figure 7.

This DfT change provides separated supply paths drawn from the V_LOW1 input for the SMPS block and for the rest of the chip. However, it is not a very efficient solution from the chip area point of view, since it requires at least $100 \times 100\,\mu$m of silicon area for each PAD. On the other hand, taking into account the dimensions of the chip and the fact that some of the package pins are not connected, it is a rather feasible and convenient solution. In normal operation mode, the PADs are externally connected together, while for test purposes the external connection is removed.

Another possible DfT modification would be the power down mode, separated for the SMPS and the rest of the chip (see Figure 8). This solution would enable testing of the SMPS while the rest of the circuitry is not active, thus, eliminating the 'background noise' created by this circuitry. In such a way, the parametric test could be precisely performed also for the V_LOW1 supply path. Moreover, the proposed solution is not demanding noticeable silicon area overhead, while providing basically the same testability improvement as the previous solution, thus test becoming more efficient. On the other hand, it requires an additional selection bit 'SEL', determining what part of the chip is going to be controlled by the

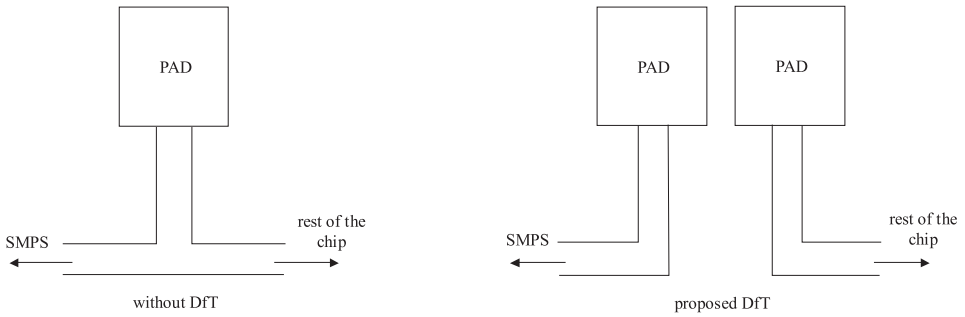

Fig. 7. Power supply distribution DfT.

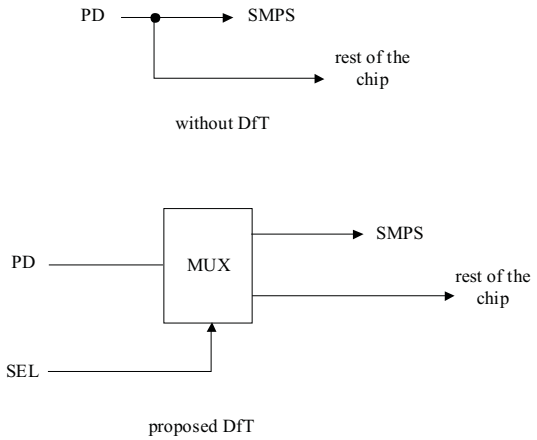

Fig. 8. DfT solution proposed for power down mode.

power down signal (PD). Anyhow, this solution is not as efficient as the first one, since it just allows to put the rest of the chip into the power down mode while the first solution disconnects it, thus, eliminating also the leakage current of the rest of the chip from the supply path.

5 CONCLUSION

The aim of the presented experiment was to analyze and evaluate the efficiency of some basic test strategies on a moderate complexity mixed-signal integrated circuit. Test method representatives from the groups of functional, structural and parametric approaches have been included within the experimental analysis. The most probable and frequent bridging faults, determined by the fault list extracted from the circuit layout, were considered and modeled. Then, the fault coverage, efficiency and the quality of these tests were evaluated and compared. As shown above, the fault coverage of all the tests is comparable, since no substantial differences have been reported. As soon as the time necessary to execute the test is taken into account, the differences between the tests are much more remarkable, since the functional approach requires approximately 400 times longer test time than the parametric strategy, while still offering even a lower fault coverage.

In the next step, the quality of the selected test techniques in terms of multiple detections was evaluated. As the evaluation shows, only the structural and the parametric tests are offering some multiple detections. From all these results, one could conclude that the most beneficial test approach for the selected CUT is the parametric one. It offers the highest fault coverage and good test quality, with a short test application time needed. The only disadvantage, compared to the functional and structural approaches, is the decision criteria that are not taken directly from the circuit specifications, but determined indirectly by the corner analysis of the fault-free circuit. This could be a serious limitation in some applications, where a very sensitive or hard to measure parameter has to meet the specifications. In such cases, dedicated setups and measurements are introduced to target this specific parameter.

Furthermore, in order to enhance the test methods efficiency, two DfT solutions have been proposed. Both are targeting the V_LOW1 supply path additional possible detections by removing the 'background noise' introduced by the on-chip circuitry (SMPS excluded). One of the proposed DfT solutions is providing an isolation mechanism, while the second one is putting the non-tested part of the chip into the power-down mode.

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Juraj Brenkuš received the MS degree in Electronics from Slovak University of Technology in Bratislava, Slovakia, in 2000. Since September 2000 he has been PhD student at Microelectronics Department of Slovak University of Technology. He is the author or co-author of more than 10 papers presented at international conferences. His main research interests are IC design and test, on-chip testing and test development automation.

Viera Stopjaková received the MS degree and PhD degree in Electronics from Slovak University of Technology in Bratislava, Slovakia, in 1992 and 1997, respectively. Since September 2009 she has been professor at Microelectronics Department of Slovak University of Technology, where she has been involved in several domestic and EU research projects. She is the author or co-author of more than 90 papers published in journals or presented at international conferences. Her main research interests are IC design and test, on-chip testing, biomedical electronics and neural networks.

Ronny Vanhooren. Biography not available.

Anton Chichkov graduated in 1990 in VLSI design at the Technical University of Sofia, Bulgaria. In 1998 he received the PhD in Electronics and Computer Science from the Technical University of Lisbon. He has worked as test engineering and test methodology manager in Alcatel Microelectronics, AMI Semiconductor and ON Semiconductor. He has earned several publications in high speed ASICs design, ASIC emulation techniques, HW/SW co-design, industrial test methods and test development automation. Holds patent on automatic test program generation methods and tools.