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COMMUNICATIONS

ION IMPLANTED OHMIC CONTACTS TO AlGaN/GaN STRUCTURES

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Implantation of silicon ions was used for the ohmic contact resistance improvement in AlGaN/GaN and GaN epitaxial layers on sapphire. $^{28}\ Si^{+}$ ions with a dose $2 \times 10^{15}\,\mathrm{cm}^{-2}$ and energy 80 keV were selectively implanted using a photoresist mask. Implanted samples were RTP annealed in temperatures up to 1250 °C in nitrogen ambient using unprotected surface method and proximity geometry method with a dummy GaN/sapphire wafer as the cover. Post-annealed sample surface was studied by SEM, AFM and EDS methods. High density of 1 μm size defects on unprotected surface samples was observed. The proximity method resulted in good surface quality without defects. Ohmic contact Ti/Al/Ni/Au multilayer was electron beam evaporated and RTP annealed at 850 °C. The ohmic contacts fabricated in the Si implanted regions revealed the specific contact resistance of $1.5 \times 10^{-5}\Omega\mathrm{cm}^2$, in comparison to $8 \times 10^{-5}\Omega\mathrm{cm}^2$ that means fivefold improvement of the ohmic contact resistance was obtained due to ion implantation processing.

K e y w o r d s: ion implantation, heterostructure, AlGaN/GaN, ohmic contacts

1 INTRODUCTION

Low resistivity of ohmic contacts in device structures are essential for proper functioning of the devices, particularly in high frequency or high power applications. In AlGaN/GaN HFETs an efficient method undertaken in this direction is Si ion implantation into source/drain sub-contact regions [1].

In a number of reports [2–4] the parameters of Si implantation process into GaN layers are specified and could be grouped in the following ranges: ion energy 30–100 keV, ion dose 1×10^{15}–$5 \times 10^{15}\mathrm{cm}^{-2}$, RTP annealing temperatures 1100–1400 °C, annealing time 30 s –5 min, N_2 or N_2/H_2 ambient. During thermal processing different methods of GaN surface protection from decomposition are used: proximity geometry (face-to-face aligned GaN layers), capping with a protective (SiO_2, AlN, SiN_x) layer, quartz ampoule with Al vapor encapsulation or nitrogen overpressure in the reactor.

In this work, we investigate post-implant processing of GaN and AlGaN/GaN layers implanted with Si ions and evaluate the resulting resistance of the Ti/Al/Ni/Au ohmic contacts. Special attention was put to the observed GaN surface degradation during the high temperature treatment.

2 EXPERIMENT

The investigated samples were structures of GaN layers undoped and Si-doped ($n = 10^{17}\mathrm{cm}^{-3}$) both epitaxially grown and GaN/AlGaN/GaN (5 nm/30 nm/500 nm) heterostructures used for fabrication of HFET devices grown on sapphire substrates by low pressure metal-organic chemical vapor deposition. Since processing of a HFET device structure requires several masks and mask alignment procedure, alignment marks were developed using ohmic contact metalization and were deposited on the samples before the ion implantation process took place. The samples were implanted with $^{28}\mathrm{Si}^{+}$ ions with a dose $2 \times 10^{15}\mathrm{cm}^{-2}$ and energy 80 keV at room temperature. Such implantation conditions resulted in the peak concentration about $2 \times 10^{20}\mathrm{cm}^{-3}$ at the mean projected range of 50 nm. Implantation was carried on directly to the structure, without surface passivation, using a 2 μm thick photoresist mask. Post-implant annealing was performed in a halogen lamp RTP fitted with a graphite susceptor using N_2 gas as ambient. The temperature was controlled by a thermocouple embedded in the susceptor. Initially samples were annealed with unprotected surface but due to the observed formation of defects, proximity geometry (face-to-face), with a dummy GaN/sapphire sample as a cover, was applied. After thermal processing was done, investigations of the sample surface were performed using SEM, EDS and AFM instruments. Then, the ohmic contacts metalization (Ti/Al/Ni/Au) was e-beam evaporated and annealed in 850 °C by RTP. Evaluation of the specific contact resistance was performed using CTLM technique.

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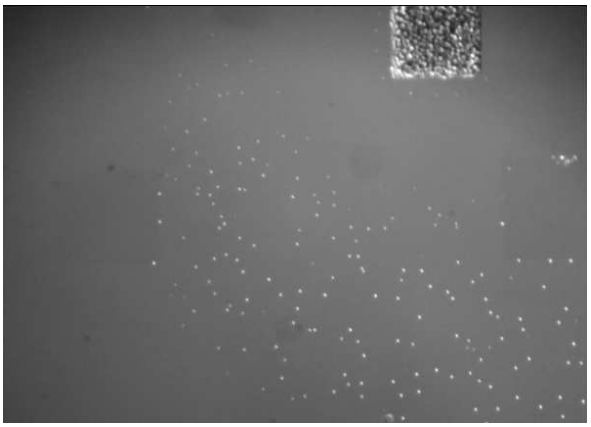

Fig. 1. Ion implanted GaN sample annealed at 1050 °C, 15 s; without a cover

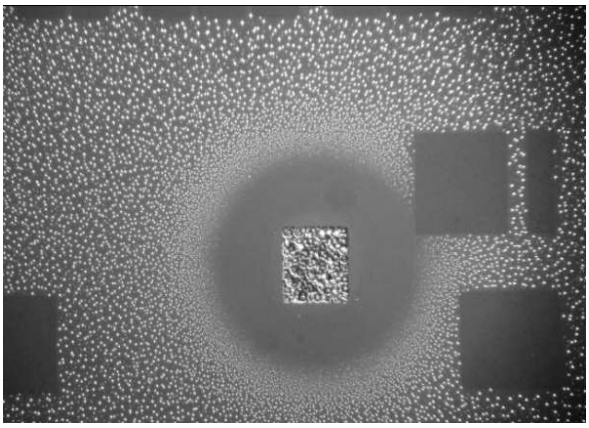

Fig. 2. Ion implanted GaN sample annealed at 1050 °C, 15 s +1100 °C, 10 s; high defect density in the non-implanted regions

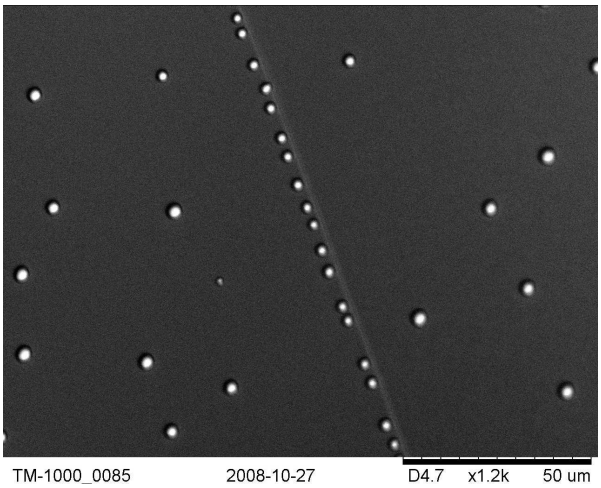

Fig. 3. SEM microphotograph showing defects distributed along a line dislocation after annealing at 1100 °C, 15 s

3 RESULTS

First, preliminary annealing processes were performed for the implanted and non-implanted GaN samples. RTP annealing in nitrogen ambient without protected sample surface resulted in formation of the surface defects with their density increasing with the annealing temperature (compare Fig. 1 and Fig. 2). The defects started to form in the non-implanted regions after processing at 1050 °C, just after short annealing time of 15 s (Fig. 1). Samples with the doped and undoped GaN layers were defected in the same degree. Fig. 2 presents a sample annealed sequentially at 1050 °C, 15 s and at 1100 °C, 10 s, which resulted in much higher density of defects. An interested feature is a lack of defects in the implanted regions (dark rectangles). Another interesting finding is that there are no visible defects around metalization (an alignment mark). It can be speculated that metal contact prevents formation of the defects by locally decreasing temperature during the annealing or it saturates possible crystal stress in its vicinity.

A SEM microphotograph presented in Fig. 3 indicates that in 1100 °C defects decorated line dislocations already existing in the sample. Energy dispersive spectroscopy (EDS) tool available in the SEM was applied to study the nature of the defects. Unfortunately, the analysis revealed just Ga in non-implanted and Ga with traces of Si in the implanted regions of the GaN layer. There was no change of EDS signal in the defect region, probably due to small area of a single defect. As it was evaluated by AFM study (Fig. 4) a typical shape of the defect was a dome with its height of $1 - 1.3\,\mu$m and its base diameter of 1–3 μm. We believe that this kind of defects arises due to gallium agglomeration after nitrogen atoms escaped from the sample.

To avoid defect formation, further annealing processes were performed using proximity geometry that is a dummy sapphire substrate with the GaN layer was used as a cover. It was found that such arrangement protected the annealed sample from creation of defects in the annealing temperatures as high as 1250 °C, but instead, high density of defects was generated in the cover itself. In Fig. 5 a GaN sample surface after annealing at 1200 °C is shown.

The upper part (photo in Fig. 5) was shadowed with the dummy sample during annealing and it revealed smooth, un-defected surface. The lower part shown, annealed without cover, revealed a high density of defects. Gallium precipitation was noticed in the surface of a dummy GaN layer. Presumably the cover has gained higher temperature then the implanted sample underneath during heat radiation from the halogen lamps.

The proximity method was used to anneal ion implanted damage in the source/drain regions of GaN/AlGaN/GaN/sapphire heterostructure developed for HFET device fabrication. The annealed samples were patterned using lift-off photolithography to obtain ohmic contact metalization in the implanted regions. Ti/Al/Ni/Au multilayer was electron beam evaporated and RTP annealed at 850 °C. A non-implanted, uniformly Si doped ($n = 1 \times 10^{17}\mathrm{cm}^{-3}$) GaN sample was also processed to obtain ohmic contacts for comparison purposes. The contacts on GaN sample after annealing at 850 °C for

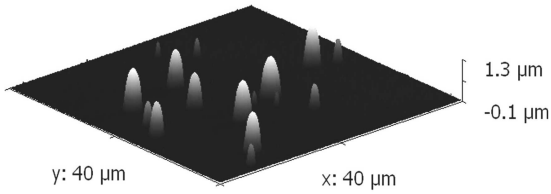

Fig. 4. An AFM area scan picture of the defects in the sample annealed at 1100 °C, 15 s.

Fig. 5. Ion implanted sample annealed at 1200 °C, 45 s, partially covered (upper part in the photo with no defects).

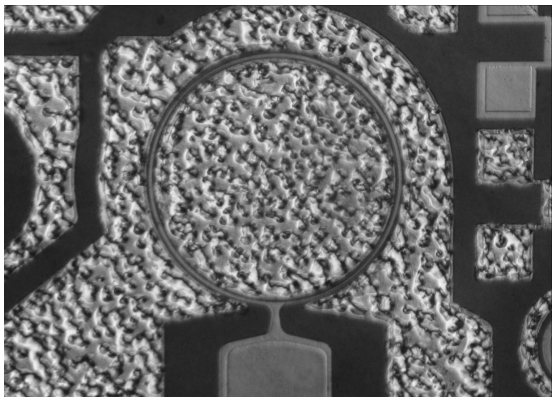

Fig. 6. Structure of a circular geometry HFET device with the processed ohmic contacts and a Schottky gate.

30 s revealed a linear I–V characteristic, while contacts on the heterostructure were strongly nonlinear. Subsequent alloying at 850 °C for additional 45 s resulted in linear I–V characteristics of heterostructure contacts, and no change in GaN sample contact linearity. To improve bonding quality, the contacts were covered with another metalization of Ti/Au layer. A part of the processed structure is shown in Fig. 6. The specific contact resistance in both samples was evaluated using circular transmission line method (CTLM). The ohmic contact resistance of $1.5 \times 10^{-5}\Omega\text{cm}^2$ for the Si ion implanted GaN/AlGaN/GaN heterostructure sample was obtained, while for the unimplanted GaN sample the contact resistance of $8 \times 10^{-5}\Omega\text{cm}^2$ was obtained.

4 CONCLUSIONS

Silicon ion implanted n^+ regions for ohmic contact were formed in GaN and AlGaN/GaN layers. Post implantation annealing by RTP was investigated using two methods. Annealing with unprotected sample surface resulted in many defects. The proximity geometry method with a dummy GaN/sapphire wafer used as a cover resulted in good surface quality, without visible defects, up to the annealing temperature of 1250 °C. The ohmic contacts fabricated in the implanted regions revealed the specific contact resistance of $1.5 \times 10^{-5}\Omega\text{cm}^2$ that means fivefold improvement of the standard ohmic contact resistance obtained without ion implantation.

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