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COMMUNICATIONS

STUDY OF PtSi/TiW vs PtSi/Ti–TiN CONTACT STRUCTURES

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The contact structure in integrated circuits (IC) needs to have good ohmic properties with low contact resistance and it needs to be thermodynamically stable to prevent contact degradation. Usually, a structure with a PtSi-TiW-AlCu metallization or a TiSi2- TiN-AlCu metallization in the IC fabrication is used. In this paper, the electrical properties of two contact structures are investigated. On different metallization sandwiches, the function of silicide and barrier layer will be described. The PtSi silicide layer will be used with TiW and Ti-TiN barrier types and the contact properties will be characterized on single contacts and on power MOS transistors. Generally, the TiW barrier process is very dirty because the particles creating. From this point of view, the equipment mean time to cleaning (MTTC) is also derived. Therefore, a TiN barrier implementation will be attractive for manufacturing. The TiN barrier will be tested on a power transistor product which was previously developed with a TiW barrier.

K e y w o r d s: PtSi, TiW, TiN, Ti-TiN, silicide, diffusion barrier, Schottky contact, power transistor

1 INTRODUCTION

The contact structures are important parts of the transistors or the diodes. Important property of the ohmic contact is low contact resistance, because the current losses or signal time delays. First, the silicide layer (PtSi, $TiSi_2$, Wsi_2, $MoSi_2$, Ni_2Si) is created onto silicon. In this work the platinum silicide was used. The platinum-silicide was implemented because they excellent electrical characteristics, due to the mechanism by which the silicide is formed [1]. During the growth process, the original contaminants from the Pt-Si interface are swept to the surface of the newly formed silicide, and the PtSi-Si interface is buried beneath the original Si surface. As a result, an absolutely clean and intimate silicide-silicon contact is formed. The PtSi has also other characteristics. The formation of the PtSi layer occurs in a lateral, as well as a vertical direction. This effect reduces the gate length and it is unwanted. Second, a barrier layer is implemented between silicide contact and AlCu metallization. The barrier is necessary because Si solubility in AlCu layer. This is starting mechanism for junction spiking. Most common barrier materials are W, TaN, TiW, TiWN, TiN, TiON ... In this paper, TiW and TiN barrier layers are used.

Titanium tungsten was among the first material to be employed as a diffusion barrier a typically used with PtSi layer which is in direct contact with heavy doped Si regions. While tungsten is by itself a fairly good diffusion barrier, the Ti is added for several reasons. First, Ti improves the adhesion of the tungsten to SiO_2. Second, it protects the tungsten from corrosion by forming a thin layer of titanium oxide on the surface, making the tungsten an even better diffusion barrier [2]. Finally, the maximum temperature that the contact can withstand is increased to 500 °C.

Titanium nitride is an attractive material as a contact diffusion barrier in silicon manufacturing, because it behaves as an impermeable barrier to silicon and because the activation energy for the diffusion of other impurities is high [3]. TiN is also chemically and thermodynamically very stable. The TiN specific contact resistivity to Si is somewhat higher than that of Ti or PtSi, and as result, it is ordinary not used to make direct contact to Si. Instead it, contact structure consisting of TiN-Ti-Si or TiN-$TiSi_2$-Si was most commonly been used. Such contact structures exhibit very low specific contact resistivity to Si and remarkably high thermal stability, with the ability to withstand temperatures up to 550 °C without contact failure. Finally, the AlCu interconnect layer is deposited on the barrier layer.

Because high current operation the power transistors in IC should be most sensitive parts for barrier stability testing. The power metal oxide semiconductor field effect transistor (MOSFET) is based on the original MOS transistor scheme with poly-silicon gate; in this work tested.

2 SEMICONDUCTOR — METAL CONTACT

Two types of the metal-semiconductor contacts are used in the ICs fabrication of the semiconductor devices. They are the Schottky and the ohmic contacts. Therefore, the diffusion barrier layer change will be characterized by them. A Schottky contact exhibits asymmetrical current voltage (I–V) characteristics due to a potential barrier

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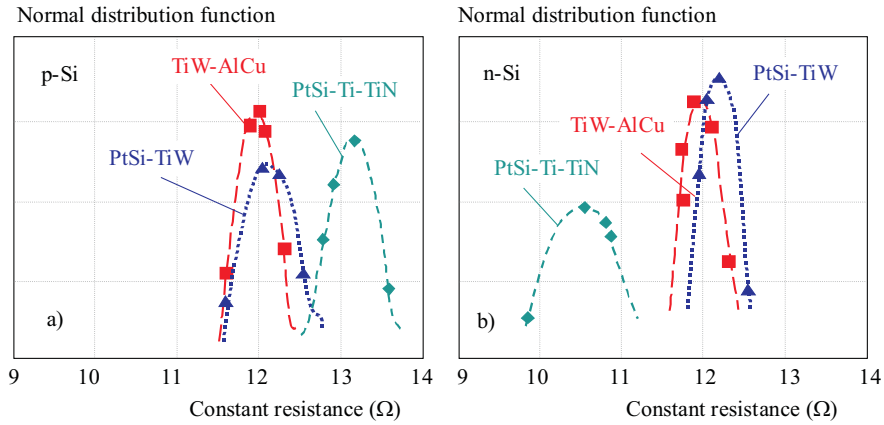

Fig. 1. Metal-Si contact resistance vs. the barrier type; a) for p-Si type; b) for n-Si type

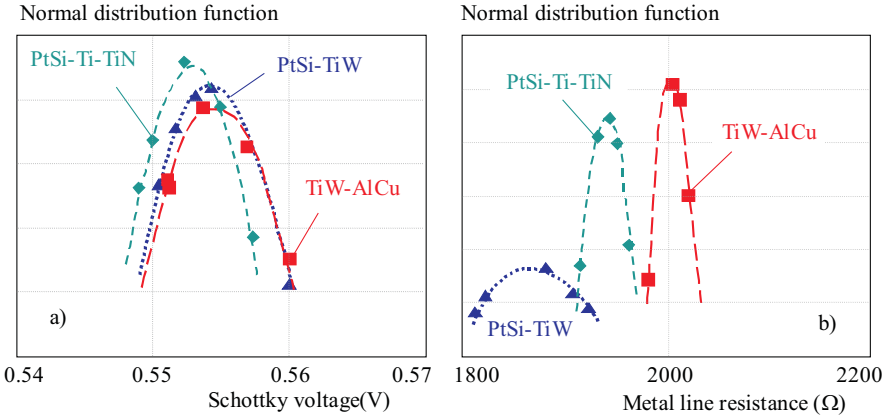

Fig. 2. a) The Schottky forward voltage vs. the barrier type; b) The metal line resistance vs. different barrier use

created between metal and semiconductor. The ohmic contact (created on high doped semiconductor), on the other hand, shows a linear I–V characteristic regardless of the polarity of the external bias voltage. A Schottky diode is formed by an appropriate metal deposition on a low doped semiconductor of either type. The metal has a work function W_M, what represents the distance between Fermi level and vacuum level. An electron having energy higher than the vacuum level can move freely in space. The potential Schottky barrier height (Φ_B) is defined for the n-Si and the p-Si by different way. For n-Si is given by $q\Phi_B = W_M X_s$, for p-Si is given by $q\Phi_B = X_s + E_g W_M$, where X_s is an electron affinity and E_g is a valence band [4].

3 DIFFUSION BARRIER PROPERTIES

The concept of the barrier layers use in metallization systems is to keep separately two materials. The barrier layer should form low resistance contacts with both materials silicide and AlCu. The resistivity of the barrier layer itself is usually not too significant because of its small thickness compared to that of the materials which are separated. The reactions in and between solids involve diffusion in the solids or across the interfaces. The movement of atoms necessarily requires a driving force, which can be thermal, chemical, electrical or mechanical in origin. In this work, the diffusion barrier thermodynamic properties will be tested by power NMOS transistor. The basic difference of power transistor is in transistor dimensions. The transistor dimensions are designed to be able work with higher voltage and current without to run out of maximum temperature limits [5]. The leakage current in this work tested, is defined as maximum allowed current through drain — substrate diode reverse biased. The channel is closed (accumulated), the source and substrate are connected to ground and the drain to bias. The PN diode reverse biased is created. The most important characteristics of power MOS transistor is the R_{ON} resistance (the resistance in switch-on state of transistor). R_{ON} is made up of several components. $R_{DS(on)} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml}$, where R_{source} is a source diffusion resistance, R_{ch} is a channel resistance, R_A is an accumulation resistance, R_J is a JFET resistance of the region between the two body regions, R_D is a drift region resistance, R_{sub} is a substrate resistance and R_{wcml} is a sum of bond wire resistance, contact resistance between the source and drain metallization and the silicon, metallization. The R_{wcml}

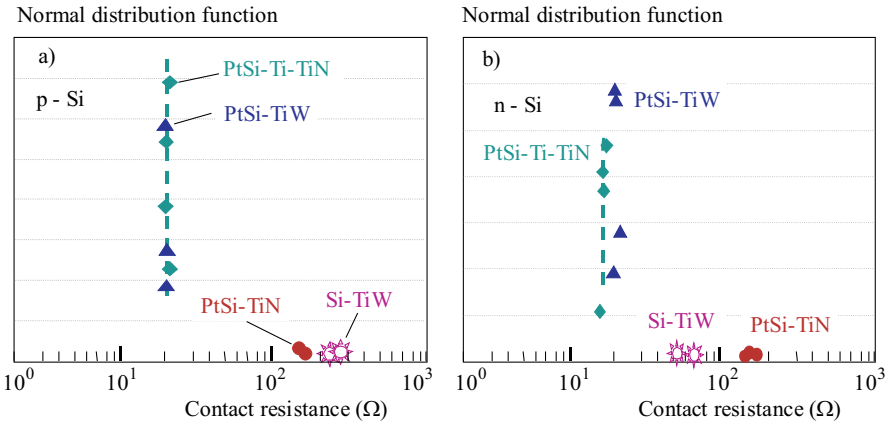

Fig. 3. Metal-Si contact resistance *vs* the barrier type; a) for p-Si type; b) for n-Si type

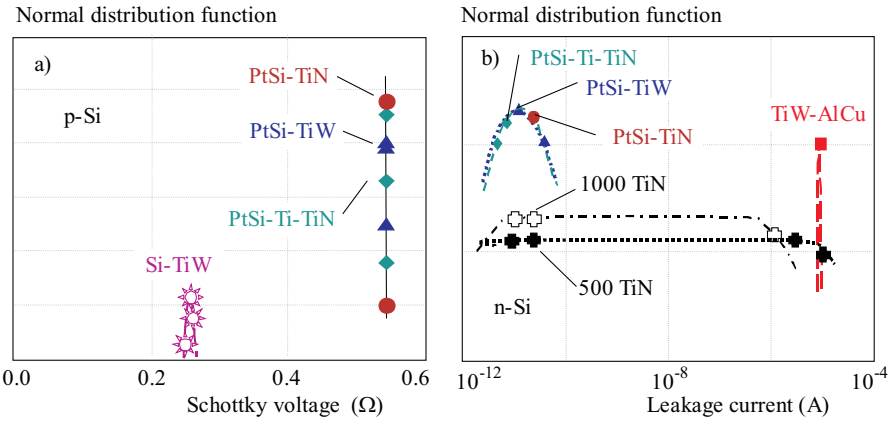

Fig. 4. a) The Schottky forward voltage vs. the barrier type; b) NMOS transistor $I_{leakage}$ *vs* barrier type

can be normally negligible in high voltage applications but can become significant in low voltage applications.

4 EXPERIMENTAL

The measurement was made on ON Semiconductor Piestany power MOSFET transistor product NCP1582. The TiW barrier was deposited on the varian#3290 equipment; from single target (90% W, 10% Ti). The Ti-TiN barrier was deposited on the MRC Eclipse Mark4 equipment; from single Ti target in Ar-N_2 ambient. The electrical characteristics were measured on five test structures on 6 inches wafers. The metal line resistance parameter (serial metal strap resistance), the contact resistance parameter and the Schottky voltage parameter were tested. The n-Si and p-Si square contact size is $\sim 2\,\mu$m. The Schottky square contact size is $\sim 17\,\mu$m. The metal line is made with snake structure on $\sim 240\,\mu$m$\times \sim 1060\,\mu$m area (line width is $\sim 1.1\,\mu$m). The power transistor gate oxide thickness is 35 nm. The gate dimensions are $2.2\,\mu$m $\times$ $215\,\mu$m (length $\times$ width). The structure is built with 160 gates electrodes net with $4\,\mu$m gap between them, where the drain-source region is implanted (with B or As). In charts, the normal sum distribution function calculated from the mean value and the standard deviation of the measured samples are compared. The ICs structure was tested with and without PtSi silicide, with pre-metallization cleaning before barrier deposition, with TiW, TiW in situ deposited with AlCu, TiN and Ti-TiN barriers.

First, the TiW and Ti-TiN barrier change is investigated (Fig. 1). The TiW barrier was tested also with AlCu layer deposited in situ and with airbreak between them. The n-Si contact resistance is shifted down in comparison with p-Si contact resistance. The electrical parameters are adjusted with the barrier work function.

The Ti under layer has a lower work function compare to TiW layer which correlates with electrical measurement results. The Schottky diode (build onto n-Si) forward voltage is changed also because the barrier work function changes (Fig. 2a). The metal line resistance is shifted up for the Ti-TiN layer. It is defined with the barrier-AlCu interface [6]. The $TiAl_3$ intermetallic compound is created on the interface and from this reason the metal line resistance is increased (Fig. 2b). It was also confirmed with layer sheet resistance measurement on wafers test structures. The TiW barrier deposited in situ with AlCu layer option has the highest metal line resistance (Fig. 2b). The difference to the airbreak, when

the barrier layer is exposed to the air and the layer surface is oxidized, is that an intermetallic forming with bimetallic compound WaI_{12}, which is created at annealing temperatures higher than 450 °C at the interface without the TiW oxidized surface. The tungsten oxide layer (WO_3) is consumed in the oxidation-reduction reaction with the AlCu if the TiW surface is oxidized. The reaction product Al_2O_3 inhibits the intermetallic reaction. Then to form WaI_{12} layer, it is necessary to increase annealing temperature to 600 °C or to use longer annealing time [7].

Second, the Ti liner layer function deposited before TiN barrier and the pre-metal cleaning before TiW barrier deposition was tested (Fig. 3). With the use of TiN barrier, the resistance is higher for both silicon types. It is given by the reactive sputtering in the N_2 ambient.

The N_2 gas nitride the PtSi surface and this mechanism increase the contact resistance. The Schottky voltage is lower because TiN work function influence compare to the TiW and Ti-TiN barriers (Fig. 2a). The PtSi surface purity was tested with pre-metal plasma cleaning turn-off.

It has influence only on the ohmic contact. The Schottky contact is not influenced. The not removed SiO_2 layer on the PtSi surface significant influences the contact parameters.

Third, the PtSi silicide layer function was tested (Fig. 3). The TiW barrier layer onto the silicon area was directly deposited. The shift in contact resistances is made due to work function difference and also due to Si-TiW interface resistance. The p-Si contact resistance is 6× higher in comparison to n-Si. During the PtSi growth process, the original contaminants from the Pt-Si interface are swept to the surface of the newly formed silicide and the PtSi-Si interface is buried beneath the original Si surface. The result is an absolutely clean and intimate silicide-silicon contact. During the TiW deposition process, the Si surface is cleaned with the pre-metal plasma cleaning.

Fourth, the barrier thermodynamic stability was tested. The contact was characterized with the Si-TiW interface. The stability was tested with power NMOS transistor leakage current between drain and substrate. Only TiW barrier deposited in situ with AlCu layer has higher value of leakage current. Without air break, the AlCu penetrates easier through the barrier and degraded the contact. The AlCu acceptors atoms doped the n-type region. This mechanism degraded the n-type drain region [8]. With this way, the TiN barrier was tested also. The TiN barrier starts to degrade at thickness of 50 nm.

4 CONCLUSIONS

The silicon-metal, the silicide-barrier and the barrier-aluminium interface are investigated. The electrical parameters depend on the material work function, on the interdiffusion properties between two layers and on the interface purity. With the TiW barrier limitation on the MOS structure, the Ti-TiN barrier thermal stability was shown. The TiN barrier could be use only with Ti underlayer, which was tested also. This characterization suggests that the Ti-TiN barrier change could be attractive for manufacturing. With the change and process optimization could increase the equipment MTTC and the process could be more robust associated with leakage current through the contact structure. In this work, the contact sandwich multistructure also with each layer interaction was complex characterized. This characterization could help manufacturing to solve issues easily associated with contact parameters.

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