MULTIFUNCTION CURRENT DIFFERENCING CASCADED TRANSCONDUCTANCE AMPLIFIER (MCDCTA) AND ITS APPLICATION TO CURRENT-MODE MULTIPHASE SINUSOIDAL OSCILLATOR

Chunhua Wang — Hairong Lin

In this study, a new versatile active element, namely multifunction current differencing cascaded transconductance amplifier (MCDCTA), is proposed. This device which adopts a simple configuration enjoys the performances of low-voltage, low-input and high-output impedance, wide bandwidth etc. It simplifies the design of the current-mode analog signal processing circuit greatly, especially the design of high-order filter and oscillator circuits. Moreover, an example as a new current-mode multiphase sinusoidal oscillator (MSO) using MCDCTA is described in this paper. The proposed oscillator, which employs only one MCDCTA and minimum grounded passive elements, is easy to be realized. It can provide random \( n \) (\( n \) being odd or even) output current signals and these output currents are equally spaced in phase all at high output impedance terminals. Its oscillation condition and the oscillation frequency can be adjusted independently, linearly and electronically by controlling the bias currents of MCDCTA. The operation of the proposed oscillator has been testified through PSPICE simulation and experimental results.

**Key words:** current-mode circuit, multifunction current differencing cascaded transconductance amplifier (MCDCTA), multiphase sinusoidal oscillator (MSO), analog integrated circuit

1 INTRODUCTION

Active building blocks have a wide range of application in analog signal processing, especially the design of oscillator and filter circuits. As a result, a lot of active elements and their related applications have been introduced in current-mode signal processing circuits, for instance, operational transconductance amplifier (OTA) [1, 2], current amplifier (CA) [3], current feedback operational amplifier (CFOA) [4], second-generation current conveyor (CCII) [5–9], current differencing buffered amplifier (CDBA) [10, 11] etc. Unfortunately, these reported circuits suffer from one or more of the following drawbacks:

(a) Complex circuitry
(b) High power consumption
(c) Operation in voltage-mode
(d) High-input and low-output impedance
(e) Narrow bandwidth
(f) Lack of electronic controllability
(g) Needing element-matching conditions

To facilitate the implementation of current-mode analog signal processing circuit, D. Bioled presented the current differencing transconductance amplifier (CDTA) in 2003 [12]. This device is a synthesis of the well-known advantages of the CDBA and OTA. It is also really current-mode element whose input and output signals are all current form. Comparing some others active device, the outstanding features of this active element are larger dynamic range, high slew rate, electronic adjustability and low-input and high-output impedance etc. Meanwhile, from our investigations, CDTA element and its some modified devices have been widely used in analog signal processing circuit in recently years [13–31]. However, so far, all of the reported CDTAs have two unavoidable problems: first, the transconductance of the CDTA cannot linearly tunable by controlling external bias current in a large input current range. Second, the published CMOS-based CDTA circuits are subject to a limit of bandwidth. Moreover, the most reported active devices are mainly used for low-order circuit structures design. The design of higher order current-mode circuits need to employ a large number of active components. Undoubtedly, the use of multiple active elements will inevitably increase the complexity of the circuit, chip area and power in the analog circuit design. Hence, for the design techniques of stable and accurate circuits, single active element, rather than many elements, should be single suitable current-mode active device. The literatures [16, 20, 22] have explained this view well.

Recently, a current differencing cascaded transconductance amplifier (CDCTA) with \( n \) transconductances tuned electronically has been presented by Jun X [32]. CDCTA enjoys the features of simple structure, low input impedance and low power consumption etc. However, this active device which has some weakness in the structure and performance is not really perfect active building block. It is not convenient for the design of more different analog signal processing circuits, especially the circuits including negative feedback configurations. Hence, the purpose of this paper is to present a multifunction...
current differencing cascaded transconductance amplifier (MCDCTA) and its application on multiphase sinusoidal oscillator. This MCDCTA is not an extension of MCDTA which consists of two independent building blocks, Z-copy CDBA and OTA [27]. The presented MCDCTA is an independent and systematic active building block, which is different with some simple combination of CDBA and OTAs. It can improve the accuracy and flexibility of current-mode circuit design greatly. By cascading transconductance stages in series connection, this element with two current inputs (p and n terminals) and n + 1 transconductance stages can easily achieve n-order lossy integral operation (assuming that capacitors are connected to relational ports) and one current operation amplifier (assuming that a resistor is connected to relational port). Thus it simplifies the design of the current-mode multiphase sinusoidal oscillator circuit considerably. Up to now, the design of MSO circuit which uses a single active element has not yet been reported.

A comparison of the previously published MSOs using various active devices and the proposed oscillator designed in this study is summarized in Table 1. From Table 1, compared to previous works, it is noted that the proposed MSO greatly reduces the number of active elements (only one active element) and overcomes the aforementioned weakness of the already reported MSOs.

### Table 1. Comparison results for the proposed MSO and other reported MSOs

<table>
<thead>
<tr>
<th>Topology</th>
<th>Number of active elements</th>
<th>Number of resistors</th>
<th>Passive components grounded</th>
<th>Electronically high-output operation</th>
<th>Low-input impedance</th>
<th>No needing additional amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td><a href="OTA">2</a></td>
<td>n</td>
<td>n</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><a href="CA">3</a></td>
<td>n</td>
<td>0</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><a href="CFOA">4</a></td>
<td>n</td>
<td>2n</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><a href="CCII">9</a></td>
<td>2n</td>
<td>2n</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><a href="CDBA">11</a></td>
<td>2n</td>
<td>4n</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><a href="CDTA">16</a></td>
<td>n + 2</td>
<td>0</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><a href="CDTA">20</a></td>
<td>n</td>
<td>n</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Proposed (MCDCTA)</td>
<td>1</td>
<td>1</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

![Fig. 1](image.png)

**Fig. 1.** (a) — Symbol of the MCDCTA element (b) — Equivalent circuit of the MCDCTA element

2 REALIZATION OF MULTIFUNCTION CURRENT DIFFERENCING CASCADED TRANSCONDUCTANCE AMPLIFIER

The MCDCTA element symbol and its corresponding equivalent circuit are shown in Figs. 1(a) and (b), respectively. Ideally, the MCDCTA can be characterized by the following equations.

\[ V_p = V_n = 0, \quad I_z = I_p - I_n, \]

\[ I_{x1} = I_{x1z} = g_{m1}V_z, \]

\[ I_{xi} = I_{x1z} = g_{m0}V_{x(i-1)z}, \quad (i \geq 2). \]
Proposed MCDCTA-based MSO circuit employing grounded passive elements.

Fig. 2. Proposed MCDCTA-based MSO circuit employing grounded passive elements

$X_{i2}$ by a transconductance gain ($g_{m1}$). The voltage at the terminal $X_{i2}$ is transferred in the same way to a current at the terminal $X_{(i+1)2}$ by transconductance gain $g_{m(i+1)}$. The internal current mirror provides a copy of the current flowing out of the $X_{i2}$ terminal to the ±$X_i$ terminals.

In general, the active device can be obtained by using CMOS or BJT techniques. A novel possible CMOS-based low-voltage, wide frequency MCDCTA topology realization suitable for the monolithic integrated circuit (IC) implementation can be found elsewhere. The circuit contains two principal module: a low-input resistance current differencing unit and one power stages. The current differencing unit which have very low input impedance have been formed by transistors $M_1$ and $I_{m15}$ and some power stages. Since its input terminals have extremely low-input impedance and don’t have parasitic capacitance, which vastly extends circuit’s bandwidth. The transconductance circuits are achieved using transistors $M_{16}$-$M_{23}$, $M_{36}$-$M_{43}$ and bias current sources ($I_{Bi}$). In order to increase the circuit bandwidth and output resistances, some unity-gain negative current mirrors has been designed using NMOS transistors. All of the parts of the circuit share the same voltage source VDD and VSS. Additionally, all of the PMOS transistors is equivalent to the bias current sources. Since the standard 0.18 µm CMOS process parameters, the threshold voltages $V_{TN}$ and $V_{TP}$ of the NMOS and PMOS transistors are about 0.42 V and 0.49 V, respectively. As a result, the minimum supply voltage is about $[2(0.42V)+0.49V] = 1.33$ V or ±0.665 V. The transconductance stages can be added in the circuit and terminals $X_i$, $X_{i2}$ can be extended by negative current mirrors. It is also easy to know that the transconductance stages and the number of $X_{i2}$ and ±$X_i$ ports of the MCDCTA can be chosen a reasonably as actual needed. The input resistances of the terminals $p$ and $n$ can also be

$$r_p = \frac{g_{m5} + g_{m11}}{g_{m4}g_{m5} + g_{m11} + g_{m5}g_{m10}r_{o7}},$$

$$r_n = \frac{g_{m3} + g_{m9}}{g_{m2}g_{m3} + g_{m9} + g_{m3}g_{m8}r_{o6}},$$

where $r_{oa}$ is the drain-source resistance of the transistor $M_i$ seen at output terminal and $g_{mi}$ indicates the transconductance of the transistors $M_i$. We can notice that, the input resistance $r_p$ and $r_n$ are very low due to the feedback factors from transistors $M_5 \rightarrow M_{11} \rightarrow M_{10}$ and $M_3 \rightarrow M_9 \rightarrow M_8$, respectively. The output resistance looking into the $X_i$, ±$X_i$ terminals can be, respectively, expressed as (the equations in example z, $x_1$ and $x_{12}$ ports).

$$r_z = \frac{r_{oa}r_{o4}r_{o3}r_{o15}g_{m7}}{r_{oa}r_{o4}r_{o15}g_{m7} + r_{oa}},$$

$$r_{xz1} = \frac{r_{o3}r_{o26}r_{o64}g_{m26}}{r_{o3}r_{o26}r_{o64}g_{m26} + r_{o64}}.$$  

\section{3 PROPOSED MCDCTA-BASED CURRENT-MODE MULTIPHASE SINUSOIDAL OSCILLATOR}

The presented MCDCTA simplifies the design of conventional MSO circuit greatly. The realization of the proposed current-mode MSO structure using only one MCDCTA, one grounded resistor and $n$ grounded capacitors is shown in Fig. 2. The use of grounded passive components is suitable for an integration point of view and is helpful for easing the elimination of various parasitic capacitance effects [33]. From Fig. 2 and equations (1)-(3), by routine analysis, we can write

$$I_{x1} = g_{m1}I_{C1} \frac{1}{sC_1},$$

$$I_{x2} = g_{m2}I_{C2} \frac{1}{sC_2},$$

$$\vdots$$

$$I_{xn} = g_{mn}I_{Cn} \frac{1}{sC_n},$$

$$I_{x(n+1)} = g_{m(n+1)}I_{n+1}R, I_{C1} = I_2 - I_{x1}, I_{C2} = I_{x1} - I_{x2}, \vdots$$

$$I_{Cn} = I_{x(n-1)} - I_{xn}, I_R = I_{xn}.$$
We have
\[
I_{x1} = \frac{1}{1 + (sC_1/gm1)},
\]
\[
I_{x2} = \frac{1}{1 + (sC_2/gm2)},
\]
\[
\vdots
\]
\[
I_{xn} = \frac{1}{1 + (sC_n/gmn)}.
\]
By summing the above equations, we draw
\[
L(s) = -Rg_{m(n+1)} \prod_{i=1}^{n} \frac{1}{1 + (sC_i/gmi)}.
\]

Assuming that \( gmi = gn (1 \leq i \leq n) \) and \( C_i = C \) (\( 1 \leq i \leq n \)), the open loop gain \( L(s) \) of the designed circuit in Fig. 2 can be given by
\[
L(s) = -Rg_{m(n+1)} \left[ \frac{1}{1 + s(C/gm)} \right]^n
\]
where \( Rg_{m(n+1)} \) is the current amplifier gain, \( g_{m(n+1)} \) which is tunable by adjusting the bias current \( I_{B(n+1)} \) is the \((n+1)\)th transconductance. In order to keep sinusoidal oscillations at frequency \( \omega_0 = 2\pi f_0 \), the Barkhausen criteria must be met such that
\[
L(j\omega_0) = -Rg_{m(n+1)} \left[ \frac{1}{1 + j\omega_0(C/gm)} \right]^{(n)} = 1,
\]
that is
\[
\left[ 1 + j\omega_0 \frac{C}{gm} \right]^n + (Rg_{m(n+1)}) = 0.
\]
We have
\[
\Delta \varphi = \frac{\pi}{n} = \tan^{-1} \frac{\omega_0C}{gm}.
\]
Here, \( \Delta \varphi \) is the phase shift of the each transconductance stage. According to the provided MSO scheme and equation (13–15), there have \( n \) output currents \( I_{o1}, \) \( i = 1, 2, 3, \ldots, n \) and each shifted phase is \( 180^\circ /n \). The size and the phase of the system loop gain are written as below.
\[
|L(j\omega_0)| = 1
\]
and
\[
\angle [L(j\omega_0)] = 2k\pi, \quad k = 0, 1, 2, \ldots
\]
Combining the above equations (14)–(17), the oscillation condition (OC) and the oscillation frequency (OF) results are expressed respectively by
\[
OC: K = \left[ 1 + \left( \frac{\omega_0C}{gm} \right)^2 \right]^{(n/2)} = Rg_{m(n+1)}
\]
and
\[
OF: \omega_0 = \frac{gm}{C} \tan \frac{\pi}{n}.
\]
Through replacing \( \omega_0 \) into (18), the oscillation condition can be obtained as
\[
OC: \left[ 1 + \tan^2 \frac{\pi}{n} \right]^{(n/2)} = Rg_{m(n+1)} \geq 1.
\]
Equation (19) shows that the oscillation frequency \( \omega_0 \) of MSO can be electronically, linearly and independently controlled by transconductance \( gm \) without obstructing condition of oscillation. Moreover, it is easy to seen that, from (20), the oscillation condition (OC) of oscillator depends on the parameter \( Rg_{m(n+1)} \). And by employing an inverted version of the output current of the MCDCTA, the even-phase (2\( n = 6, 10, 14, \ldots \)) output currents (\( -I_{O1}, -I_{O2}, \ldots, -I_{On} \)) are also achieved from the same framework. Thus, the proposed circuit of Fig. 3 can be oscillated when \( n \) is odd or even number.

Here, it may be stated that the presented MSO can be realized without any constraints on the component values, and it exhibits both low-input and high-output impedance characteristics, which will be more convenient in terms of cascading and connecting to other networks. Comparing conventional MSO circuit, it also greatly reduces the number of active and passive elements and power consumption.

\section{4 NON–IDEAL ANALYSIS}

For a complete analysis of the proposed circuit, the following non-idealities of MCDCTA must be considered. Figure 3 shows the simplified equivalent topology that will be used to represent the behavior of the non-ideal MCDCTA. Additionally, for the analysis of non-ideal
components except for the parasitic resistance and parasitic non-ideal MCDCTA characteristics and its parasitic capacitance given through the following equations.

$$C \text{ and } Z$$

Fig. 4. Frequency characteristics of input terminal resistances: (a) — p terminal; (b) — n terminal

In the non-ideal case, the MCDCTA’s current and voltage nature can be given through the following equations.

$$I_z = \alpha_p I_p - \alpha_n I_n, \quad I_{xiz} = \gamma g_{m1} V_{x(i-1)z}, \quad I_{xi} = \beta_i I_{xiz},$$

$$\alpha_p = \frac{g_{m6}g_{m7}}{g_{m13}g_{m14}} \frac{g_{m5}g_{m10}^2\omega^{57}}{g_{m5} + g_{m11} + g_{m5}g_{m10}^2\omega^{57}},$$

$$\alpha_n = \frac{g_{m3}g_{m8}^2\omega^{56}}{g_{m3} + g_{m9} + g_{m3}g_{m8}^2\omega^{56}}$$

where \( \alpha_p (\alpha_p = 1 - \varepsilon_p, |\varepsilon_p| \ll 1) \) and \( \alpha_n (\alpha_n = 1 - \varepsilon_n, |\varepsilon_n| \ll 1) \) indicate the parasitic current transfer error from p and n to z terminal. \( \gamma (\gamma = 1 - \varepsilon_c, |\varepsilon_c| \ll 1) \) denotes the parasitic transconducance tracking error from \( X_{sz} \) to \( X_{i(z+1)} \) terminal. \( \beta_i (\beta_i = 1 - \varepsilon_d, |\varepsilon_d| \ll 1) \) is the parasitic current transfer error from \( X_{iz} \) to \( X_i \) terminal. It is clearly seen that there are parasitic resistance \( r_p \), \( r_n \) (ideally equal to zero) at terminals p and n, and parasitic resistance \( r_{xiz}, r_{xi} \) (ideally equal to infinity) and parasitic capacitance \( C_{xiz}, C_{xi} \) (ideally equal to zero) from the high-impedance terminals \( z, X_{iz} \) and \( X_i \) of the MCDCTA to the ground (assuming \( C'_i = C + C_{xiz}, (1 \leq i \leq n), C'_{(n+1)i} = C_{x(n+1)z} \)).

\( Z'_i \) is an non-ideal impedance connected at the terminal \( z \) and \( X_{iz} \). Hence, taking into account all the above non-ideal MCDCTA characteristics and its parasitic components except for the parasitic resistance and parasitic capacitance at terminals \( X_i \), we can rewrite the modified current transfer functions of Fig. 2 as

$$I_{x1z} = \gamma_1 g_{m1} V_z = \gamma_1 g_{m1} (-\alpha_p I_{x(n+1)} - \beta_1 I_{x1z}) Z'_1,$$

$$I_{x2z} = \gamma_2 g_{m2} V_{x1z} = \gamma_2 g_{m2} (I_{x1z} - \beta_2 I_{x2z}) Z'_2,$$

$$\vdots$$

$$I_{xnz} = \gamma_n g_{mn} V_{x(n-1)z} = \gamma_n g_{mn} (I_{x(n-1)z} - \beta_n I_{xnz}) Z'_n,$$

$$I_{x(n+1)z} = \gamma(n+1) g_{m(n+1)} V_{xnz} = \gamma(n+1) g_{m(n+1)} I_{xnz} Z'_{(n+1)}.\quad (24)$$

The parameters \( Z'_i \) and \( Z'_{(n+1)} \) of (24) are seen to be

$$Z'_i = \frac{1}{1/r_{xiz} + sC'_i} (1 \leq i \leq n),$$

$$Z'_{(n+1)} = \frac{1}{sC'_{(n+1)} + 1/r_{x(n+1)z} + 1/R}.$$ One gets

$$L(s) = -\frac{\gamma(n+1) g_{m(n+1)}}{\alpha_p} \prod_{i=1}^{n} \frac{1}{\beta_i} \frac{1}{1 + ((1/r_{x1z}) + sC'_1)/\gamma_1 g_{m1} \alpha_p \beta_1} \times \frac{1}{sC'_{(n+1)} + 1/r_{x(n+1)z} + 1/R} \times \prod_{i=2}^{n} \frac{1}{1 + ((1/r_{xiz}) + sC'_i)/\gamma_i g_{mi} \beta_i}.\quad (26)$$

Since the value of \( r_{xiz} \) is in the order of \( \mu \Omega \), thus for an external resistor of value \( R \ll r_{xiz} \) connected at this terminal, \( R \parallel r_{x(n+1)z} \approx R \). Similarly, the value of \( C_{xiz} \) is about zero, so \( C'_i = C, \; (1 \leq i \leq n), \; C'_{(n+1)i} = 0 \). Assuming \( r_{x1z} = r_{x2z} = \cdots = r_{x(n+1)z} = r_{xz}, \; \beta_1 = \beta_2 = \cdots = \beta_n = \beta, \; \gamma_1 = \gamma_2 = \cdots = \gamma(n+1) = \gamma \). Re-analysis of the proposed MSO circuit in Fig. 2 employing (26) with \( r_{xz} \gg 1/sC, \; R \ll 1/sC'_{(n+1)z} \) the modified oscillation condition and oscillation frequency can be rewritten by the following equations.

$$L(s) \approx -R g_{m(n+1)} \frac{\gamma}{\alpha_p \beta^n} \left( \frac{1}{1 + (sC/\gamma g_{mn})^n} \right),\quad (27)$$

OC: \( R g_{m(n+1)} \frac{\gamma}{\beta^n \alpha_p} \approx \left[ 1 + \tan^2 \frac{\pi}{n} \right]^{(n/2)} \)\]

OF: \( \omega_0 \approx \frac{\gamma g_{mn}}{C} \tan \frac{\pi}{n}.\quad (29)\]

From the above equations, it is easy to show that the oscillation condition is mainly affected by the current transfer errors \( (\alpha_p, \beta) \) and transconductance tracking error \( (\gamma) \) of the MCDCTA in non-ideal case. But the influence of these errors can be easily corrected through adjusting the
value of $R g_{m(n+1)}$. Additionally, it is evident that $\omega_0$ is slightly changed from the ideal case by the factor of $\gamma \beta$. To offset this effect, it still can be tuned by the $g_{mn}$-value.

According to equation (29), the active and passive sensitivities of the oscillator in non-ideal case are deduced as

$$S_{\alpha_p}^{\omega_0} = S_{\alpha_n}^{\omega_0} = 0, \quad S_{\gamma_\beta}^{\omega_0} = S_{\beta}^{\omega_0} = S_{g_m}^{\omega_0} = -S_{C_\beta}^{\omega_0} < 1. \quad (30)$$

It is noteworthy from (30) that the absolute magnitude values of all $\omega_0$ sensitivities are about equal to 0 or 1. It is easy to see that parasitics has been alleviated through this cascaded structure considerably.

### 5 SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the performances of the proposed circuits, the CMOS-based MCDCTA circuit (two transconductance stages) was simulated with the parameters of the TSMC 0.18 $\mu$m transistor model in PSPICE circuit simulation program. The supply voltages used are $V_{DD} = -V_{SS} = 1.0 \, V$, and the bias currents $I_p$ and $I_{B1}$ are selected as 30 $\mu$A and 50 $\mu$A respectively. The dimensions of the CMOS transistors are listed in Table 2.

### Table 2. Dimensions of the CMOS transistors

<table>
<thead>
<tr>
<th>COMS TRANSISTORS W(um)/L(um)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M19,M24-M39,M44-M55</td>
<td>24/1</td>
</tr>
<tr>
<td>M20-M21,M40-M41</td>
<td>10/0.6</td>
</tr>
<tr>
<td>M22-M23,M42-M43</td>
<td>10/1</td>
</tr>
<tr>
<td>M56-M57,M62-M67,M70-M75</td>
<td>36/0.6</td>
</tr>
<tr>
<td>M58-M59</td>
<td>81/0.6</td>
</tr>
<tr>
<td>M60-M61,M68-M69</td>
<td>63/0.6</td>
</tr>
</tbody>
</table>

### Table 3. Simulated performances of the proposed MCDCTA

<table>
<thead>
<tr>
<th>Design parameters</th>
<th>Simulation results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 0.18 um</td>
</tr>
<tr>
<td>The supply voltages</td>
<td>$V_{DD} = -V_{SS} = 1.0 , V$</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>1.12 mW ($I_p = I_n = 0 , A$)</td>
</tr>
<tr>
<td>$-3 , \text{dB bandwidth}$</td>
<td>410 MHz ($I_z/I_p$), 413 MHz ($I_{x1}/I_n$), 402 MHz ($I_{x2}/I_p$), 401 MHz ($I_{x2}/I_n$), 402 MHz ($I_{x2}/I_p$), 408 MHz ($I_{x2}/I_n$)</td>
</tr>
<tr>
<td>Transconductance linear range</td>
<td>0.12 mV $\cdot$ 1.0 mS</td>
</tr>
<tr>
<td>Input bias current range</td>
<td>$-200 , \mu$A to 200 $\mu$A</td>
</tr>
<tr>
<td>$r_{p, r_{x1}, r_{x2}, r_{x12}}$</td>
<td>5.2531 $\Omega$, 6.2418 $\Omega$, 512.0536 $\Omega$</td>
</tr>
<tr>
<td>$\alpha_p, \alpha_n$</td>
<td>0.9816, 0.9815</td>
</tr>
</tbody>
</table>

The input impedance of the $p$ and $n$ terminals are given in Fig. 4(a) and (b), respectively. We can see that MCDCTA’s input impedances compared with CDTA [12] are about zero. The output impedance at $Z$, $X_i$ and $X_{iz}$ terminals was found in Fig. 5(a) and (b), respectively. It is noted that the output impedance value at the output terminals is enough to drive the load of our application. The change of $Z$ terminal current according to $p$ terminal current of the MCDCTA CMOS realization is obtained in Fig. 6, when $I_{B1} = 50 \, \mu$A. So it is clearly seen that it is linear in $-80 \, \mu$A $< I_p < 80 \, \mu$A and can be tuned. The $-3 \, \text{dB}$ cutoff frequencies of the current gains $I_{x2}/I_p$, $I_{x1}/I_n$, $I_{x12}/I_p$, $I_{x12}/I_n$ and $I_{x2}/I_n$ are approximately 410 MHz, 413 MHz, 402 MHz, 401 MHz, 402 MHz and 408 MHz, as shown in Figs. 7 and 8. The measured frequency response of transconductance is shown in Fig. 9, when the bias current is 50 $\mu$A. We can see that the transconductance of the proposed MCDCTA has a large bandwidth, which makes it suitable...
for high frequency operations. The performance characteristics of the CMDCTA CMOS configuration are seen in Table 3.

To confirm the performance of the presented current-mode MSO system in Fig. 2, a six-phase MSO \((n = 3)\) has been devised by using the proposed circuit. The proposed MSO oscillator is also simulated with PSPICE circuit simulation program. The values of the bias currents are shown in Table 4.

<table>
<thead>
<tr>
<th>Topology</th>
<th>The supply voltage</th>
<th>Measured highest load impedance (Z_L)</th>
<th>Operating frequency (f)</th>
<th>Deviation of oscillation frequency (f_o)</th>
<th>THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>±10 V</td>
<td>Dozens of 50pF</td>
<td>100 MHz</td>
<td>±10 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>[3]</td>
<td>±1.5 V</td>
<td>Hundreds of 0.22µF</td>
<td>100 MHz</td>
<td>±20 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>[4]</td>
<td>±10 V</td>
<td>Hundreds of 0.22µF</td>
<td>100 MHz</td>
<td>±10 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>[9]</td>
<td>±10 V</td>
<td>Dozens of 275pF</td>
<td>100 MHz</td>
<td>±20 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>[11]</td>
<td>±12 V</td>
<td>Hundreds of 1 nF</td>
<td>100 MHz</td>
<td>±10 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>[16]</td>
<td>±3 V</td>
<td>Hundreds of 1 nF</td>
<td>100 MHz</td>
<td>±20 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>[20]</td>
<td>±3 V</td>
<td>Hundreds of 1 nF</td>
<td>100 MHz</td>
<td>±20 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>[22]</td>
<td>±2.5 V</td>
<td>Hundreds of 1 nF</td>
<td>100 MHz</td>
<td>±20 %</td>
<td>0.84 %</td>
</tr>
<tr>
<td>Proposed</td>
<td>±1.0 V</td>
<td>Dozens of 5.3µF</td>
<td>100 MHz</td>
<td>±10 %</td>
<td>0.84 %</td>
</tr>
</tbody>
</table>

Comparison simulation results of the proposed multiphase sinusoidal oscillator to other designs are given in Table 4.

![Fig. 7. Frequency responses at z output terminal](image7.png)

![Fig. 9. Transconductance value relative to bias current \(I_B\)](image9.png)

![Fig. 8. Frequency responses at \(X_1\) and \(X_{12}\) output terminals](image8.png)

Figure 7 shows the adjustability of the oscillation frequency by \(I_B\). The deviation of the simulated oscillation frequency values is consistent with the calculated values. Although there is a deviation between the theoretical values and the simulation values in high bias current value region, decreasing this error can be offset through simply tuning the value of external capacitor \(R = 17.5 \text{ KΩ}\) are used. The output waveforms and frequency spectrum obtained from the proposed MSO topology of Fig. 2 are, respectively, shown in Figs. 10 and 11. The simulated value of oscillation frequency is 14.67 MHz, which is close agreement with the calculated value of 14.80 MHz. The deviation for oscillation frequency is 0.86%. The error is mainly due to parasitic impedances appearing at \(X_{12}\) and \(X_i\) terminals. From the simulation results, it is noted that the phase difference of \(I_{o2}, I_{o3}, -I_{o1}\) and \(-I_{o2}\) and \(-I_{o3}\) comparing with \(I_{o1}\) were, respectively, measured as 58°, 119°, 181°, 240° and 298°. Apparently, they are very close to the theoretical predicted values. The total harmonic distortion (THD) in the output waveforms \(I_{o1}, I_{o2}, I_{o3}\) were about to 0.841%. It is also found that the six-phase sinusoidal oscillator circuit power consumption is approximately 6.35 mW.

Figure 12 shows the adjustability of the oscillation frequency by \(I_B\) without affecting the oscillation condition, when \(I_0 = 30 \mu\text{A}, I_{B4} = 80 \mu\text{A}, C = 5.3 \text{ pF}\) and \(R = 17.5 \text{ KΩ}\). Obviously, in a wide frequency range, the simulated oscillation frequency values are consistent with the calculated values. Although there is a deviation between the theoretical values and the simulation values in high bias current value region, decreasing this error can be offset through simply tuning the value of external capacit
80
40
0
-40
-80
9.5 9.6 9.7 9.8 9.9
Time (μs)
0 10 20 30 40 50
f (MHz)
40
20
10
0
I_o1
I_o2
I_o3
Fig. 10. Simulated results of the proposed current-mode MSO of Fig. 3: (a) — I_o1, I_o2, I_o3, (b) — −I_o1, −I_o2, −I_o3

80
40
0
-40
-80
9.5 9.6 9.7 9.8 9.9
Time (μs)
0 10 20 30 40 50
f (MHz)
40
20
10
0
I_o1
I_o2
I_o3
Fig. 11. Simulated spectrums of I_o1, I_o2, I_o3

80
40
0
-40
-80
9.5 9.6 9.7 9.8 9.9
Time (μs)
0 10 20 30 40 50
f (MHz)
40
20
10
0
R = 24.6 kΩ, C = 1 nF, I_B = 125 μA, I_B3 = 215 μA.

The derived results are summarized in Table 4. From Table 1 and Table 4, we can see that the proposed circuit has better performance than that of the reported circuits in terms of the circuit complexity, the supply voltage, bandwidth and accuracy etc. It is also seen that the total harmonic distortion (THD) is very low relative to other reported MSO. Since its active device further alleviates parasitics and can avoid the influence of input impedance on the bandwidth of circuit, the presented MSO in this work enjoys comparatively high frequency.

To verify the workability of the proposed MSO, a current-mode four-phase oscillator according to the presented configuration is verified by experimentally tested. The MCDCTA active element was performed through using commercially available ICs, ie, AD844s (CCIIs) and CA3080Es (OTAs) in experiment. The DC supply voltages were taken as ±12 V. In experiments, working resistor, capacitor and bias current values were confirmed as follows:

R = 24.6 kΩ, C = 1 nF, I_B = 125 μA, I_B3 = 215 μA.

The oscillation frequencies obtained by experiments is about 217.39 KHz, which is deviated from the calculated value (216.18 KHz) by 0.56 %.

6 CONCLUSION

In this paper, a new active component, MCDCTA and its application to realization current mode multiphase sinusoidal oscillator have been presented. The proposed element which enjoys simple configuration, low-input and high-output impedance, wide bandwidth and versatility can be operated at low power supply voltage. The presented MSO which only adopts a single active component (MCDCTA) and few grounded passive elements decrease the number of elements, chip area and power consumption consumedly. Moreover, its parameters can be determined by varying the bias current of MCDCTA. The performances of the presented circuits have been proven by the simulation and experimental results. Based on these advantages, this novel active element and its application circuits are very appropriate to implement in IC fabrication fields; Instrumentation and measurement systems, RF transmitter/receiver, wireless communication devices etc. It is also expected to be useful for the designed active component in analog signal processing besides the oscillator circuits.

Acknowledgment

The authors would like to thank the reviewers for valuable comments and helpful suggestions. This work is supported by the National Natural Science Foundation of China (No. 61274020) and the natural science foundation of Hunan Province (No. 14JJ7026) and the Open Fund Project of Key Laboratory in Hunan Universities (No. 13K015).
REFERENCES


Received 21 April 2014

Chunhua Wang was born in Yongzhou, China, in 1963. He received the BC degree from Hengyang Teacher’s College, Hengyang, China, in 1983, the MS degree from Physics Department, Zheng Zhou University, Zheng Zhou, China, in 1994, and the PhD degree from School of Electronic Information and Control Engineering, Beijing University of Technology, Beijing, China, in 2003. He has been a professor of School of Computer and Communication, Hunan University, Changsha, China from 2004. His interests include analog integrated circuit design, RFIC design and wireless communication.

Hairong Lin was born in Changsha, China, in 1988. He received the BC degree from Huihua College, Huihua, China. He is currently studying in Hunan University for master degree. His research areas are mainly in analog integrated circuits, RFIC design and analog signal processing.