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Journal of ELECTRICAL ENGINEERING, VOL. 66, NO. 5, 2015, 241–249

MULTIFUNCTION CURRENT DIFFERENCING CASCADED TRANSCONDUCTANCE AMPLIFIER (MCDCTA) AND ITS APPLICATION TO CURRENT–MODE MULTIPHASE SINUSOIDAL OSCILLATOR

Chunhua Wang — Hairong Lin *

In this study, a new versatile active element, namely multifunction current differencing cascaded transconductance amplifier (MCDCTA), is proposed. This device which adopts a simple configuration enjoys the performances of low-voltage, low-input and high-output impedance, wide bandwidth etc. It simplifies the design of the current-mode analog signal processing circuit greatly, especially the design of high-order filter and oscillator circuits. Moreover, an example as a new current-mode multiphase sinusoidal oscillator (MSO) using MCDCTA is described in this paper. The proposed oscillator, which employs only one MCDCTA and minimum grounded passive elements, is easy to be realized. It can provide random n (n being odd or even) output current signals and these output currents are equally spaced in phase all at high output impedance terminals. Its oscillation condition and the oscillation frequency can be adjusted independently, linearly and electronically by controlling the bias currents of MCDCTA. The operation of the proposed oscillator has been testified through PSPICE simulation and experimental results.

K e y w o r d s: current-mode circuit, multifunction current differencing cascaded transconductance amplifier (MCDCTA), multiphase sinusoidal oscillator (MSO), analog integrated circuit

1 INTRODUCTION

Active building blocks have a wide range of application in analog signal processing, especially the design of oscillator and filter circuits. As a result, a lot of active elements and their related applications have been introduced in current-mode signal processing circuits, for instance, operational transconductance amplifier (OTA) [1, 2], current amplifier (CA) [3], current feedback operational amplifier (CFOA) [4], second-generation current conveyor (CCII) [5–9], current differencing buffered amplifier (CDBA) [10, 11] *etc.* Unfortunately, these reported circuits suffer from one or more of the following drawbacks:

(a) Complex circuitry
(b) High power consumption
(c) Operation in voltage-mode
(d) High-input and low-output impedance
(e) Narrow bandwidth
(f) Lack of electronic controllability
(g) Needing element-matching conditions

To facilitate the implementation of current-mode analog signal processing circuit, D. Bioled presented the current differencing transconductance amplifier (CDTA) in 2003 [12]. This device is a synthesis of the well-known advantages of the CDBA and OTA. It is also really current-mode element whose input and output signals are all current form. Comparing some others active device, the outstanding features of this active element are larger dynamic range, high slew rate, electronic adjustability and low-input and high-output impedance *etc.* Meanwhile, from our investigations, CDTA element and its some modified devices have been widely used in analog signal processing circuit in recently years [13–31]. However, so far, all of the reported CDTAs have two unavoidable problems: first, the transconductance of the CDTA cannot linearly tunable by controlling external bias current in a large input current range. Second, the published CMOS-based CDTA circuits are subject to a limit of bandwidth. Moreover, the most reported active devices are mainly used for low-order circuit structures design. The design of higher order current-mode circuits need to employ a large number of active components. Undoubtedly, the use of multiple active elements will inevitably increase the complexity of the circuit, chip area and power in the analog circuit design. Hence, for the design techniques of stable and accurate circuits, single active element, rather than many elements, should be single suitable current-mode active device. The literatures [16, 20, 22] have explained this view well.

Recently, a current differencing cascaded transconductance amplifier (CDCTA) with n transconductances tuned electronically has been presented by Jun X [32]. CDCTA enjoys the features of simple structure, low input impedance and low power consumption etc. However, this active device which has some weakness in the structure and performance is not really perfect active building block. It is not convenient for the design of more different analog signal processing circuits, especially the circuits including negative feedback configurations. Hence, the purpose of this paper is to present a multifunction

* College of Information Science and Engineering, Hunan University, Changsha 410082, P. R. China, wch1227164@hnu.edu.cn, hr12306@163.com

DOI: 10.2478/jee-2015-0040, Print ISSN 1335-3632, On-line ISSN 1339-309X

Table 1. Comparison results for the proposed MSO and other reported MSOs

Topology	Number of active elements	Passive: Number of resistors	Passive: components grounded	Electronically operation	Low-input and high-output impedance	No needing additional amplifier
[2](OTA)	n	n	No	Yes	No	Yes
[3](CA)	n	0	Yes	Yes	No	Yes
[4](CFOA)	n	$2n$	No	No	No	Yes
[9](CCII)	$2n$	$2n$	No	No	No	Yes
[11](CDBA)	$2n$	$4n$	No	No	Yes	Yes
[16](CDTA)	$n+2$	0	Yes	Yes	Yes	No
[20](CDTA)	$2(n+1)$	0	No	Yes	No	No
[22](CDTA)	n	n	No	No	No	Yes
Proposed (MCDCTA)	1	1	Yes	Yes	Yes	Yes

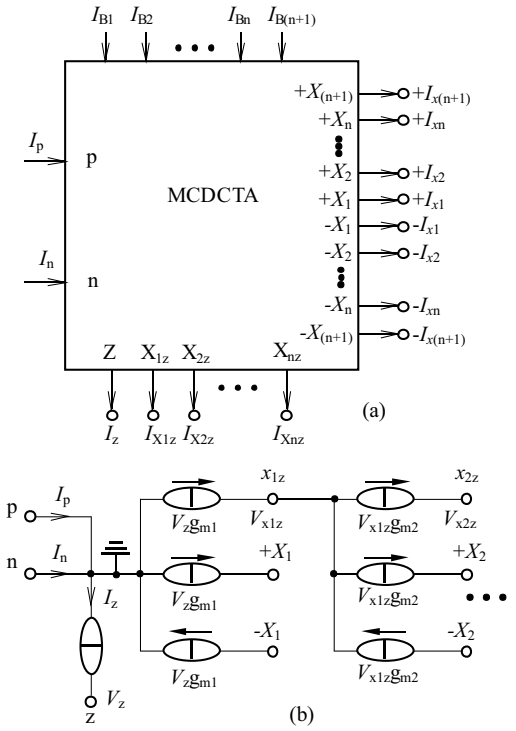

Fig. 1. (a) — Symbol of the MCDCTA element (b) — Equivalent circuit of the MCDCTA element

current differencing cascaded transconductance amplifier (MCDCTA) and its application on multiphase sinusoidal oscillator. This MCDCTA is not an extension of MCDTA which consists of two independent building blocks, Z-Copy CDTA and OTA [27]. The presented MCDCTA is a independent and systematic active building block, which is different with some simple combination of CDBA and OTAs. It can improve the accuracy and flexibility of current-mode circuit design greatly. By cascading transconductance stages in series connection, this element with two current inputs (p and n terminals) and $n+1$ transconductance stages can easily achieve n-order lossy integral operation (assuming that capacitors are connected to relational ports) and one current operation amplifier (assuming that a resistor is connected to relational port). Thus it simplifies the design of the current-mode multiphase sinusoidal oscillator circuit considerably. Up to now, the design of MSO circuit which uses a single active element has not yet been reported.

A comparison of the previously published MSOs using various active devices and the proposed oscillator designed in this study is summarized in Tab. 1. From Tab. 1, compared to previous works, it is noted that the proposed MSO greatly reduces the number of active elements (only one active element) and overcomes the aforementioned weakness of the already reported MSOs.

2 REALIZATION OF MULTIFUNCTION CURRENT DIFFERENCING CASCADED TRANSCONDUCTANCE AMPLIFIER

The MCDCTA element symbol and its corresponding equivalent circuit are shown in Figs. 1(a) and (b), respectively. Ideally, the MCDCTA can be characterized by the following equations.

$$V_p = V_n = 0\,,\; I_z = I_p - I_n\,, \tag{1}$$

$$I_{x1} = I_{x1z} = g_{m1} V_z\,, \tag{2}$$

$$I_{xi} = I_{xiz} = g_{mi} V_{x(i-1)z}\,,\; (i \geq 2)\,. \tag{3}$$

Where p and n are low-impedance current input terminals, Z, X_{iz} and $\pm X_i$ are high-impedance current output terminals, g_{mi} which can controllable electronically and independently through an auxiliary port current I_{Bi} is the transconductance gain of the ith transconductance stage, and V_z and V_{xiz} is voltage drop at the terminal Z and X_{iz} (assuming that an external impedance is connected to corresponding ports). The proposed device provides current I_{xi} in both directions, but they are equal in magnitude. On the basis of above expressions and equivalent circuit of Fig. 1(b), the current flowing out of the terminal Z (I_z) is a difference between the input current terminals p and n ($I_p - I_n$). The voltage drop at the terminal z is transferred to a current at the terminal

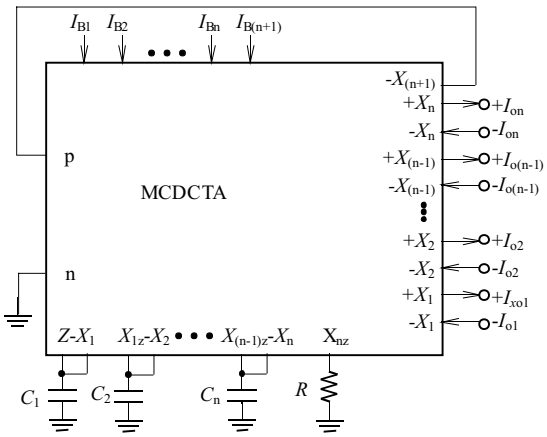

Fig. 2. Proposed MCDCTA-based MSO circuit employing grounded passive elements

X_{1z} by a transconductance gain (g_{m1}). The voltage at the terminal X_{iz} is transferred in the same way to a current at the terminal $X_{(i+1)z}$ by transconductance gain $g_{m(i+1)}$. The internal current mirror provides a copy of the current flowing out of the X_{iz} terminal to the $\pm X_i$ terminals.

In general, the active device can be obtained by using CMOS or BJT techniques. A novel possible CMOS-based low-voltage, wide frequency MCDCTA topology realization suitable for the monolithic integrated circuit (IC) implementation can be found elsewhere. The circuit contains two principal module: a low-input resistance current differencing unit and $n+1$ transconductance stages. The current differencing unit which have very low input impedance have been formed by transistors $M_1 - M_{15}$ and some power circuits. Since its current input terminals have exceedingly low-input impedance and don't have parasitic capacitance, which vastly extends circuit's bandwidth. The transconductance circuits are achieved using transistors $M_{16}-M_{23}$, $M_{36}-M_{43}$ and bias current sources (I_{Bi}). In order to increase the circuit bandwidth and output resistances, some unity-gain negative current mirrors has been designed using NMOS transistors. All of the parts of the circuit share the same voltage source VDD and VSS. Additionally, all of the PMOS transistors is equivalent to the bias current sources. Since the standard 0.18 um CMOS process parameters, the threshold voltages V_{TN} and V_{TP} of the NMOS and PMOS transistors are about 0.42 V and 0.49 V, respectively. As a result, the minimum supply voltage is about $\left[2\left(0.42\,\mathrm{V}\right)+0.49\,\mathrm{V}\right] = 1.33$ V or ± 0.665 V. The transconductance stages can be added in the circuit and terminals X_i, X_{iz} can be extended by negative current mirrors. It is also easy to know that the transconductance stages and the number of X_{iz} and $\pm X_i$ ports of the CMDCTA can be chosen a reasonably as actual needed. The input resistances of the terminals p and n can also be

$$r_p = \frac{1}{g_{m4}} \frac{g_{m5} + g_{m11}}{g_{m5} + g_{m11} + g_{m5} g_{m10} r_{o57}}\,, \tag{4}$$

$$r_n = \frac{1}{g_{m2}} \frac{g_{m3} + g_{m9}}{g_{m3} + g_{m9} + g_{m3} g_{m8} r_{o56}} \tag{5}$$

where r_{oi} is the drain-source resistance of the transistor M_i seen at output terminal and g_{mi} indicates the transconductance of the transistors M_i. We can notice that, the input resistance r_p and r_n are very low due to the feedback factors from transistors $M_5 \to M_{11} \to M_{10}$ and $M_3 \to M_9 \to M_8$, respectively. The output resistance looking into the z, $\pm x_i$ and x_{iz} terminals can be, respectively, expressed as (the equations in example z, x_1 and x_{1z} ports).

$$r_z = \frac{r_{o7} r_{o14} r_{o59} r_{o15} g_{m7}}{r_{o7} r_{o14} r_{o15} g_{M7} + r_{o59}}\,, \tag{6}$$

$$r_{x1z} \cong r_{x1} = \frac{r_{o30} r_{o26} r_{o64} g_{m26}}{r_{o30} r_{o26} g_{m26} + r_{o64}}\,. \tag{7}$$

3 PROPOSED MCDCTA–BASED CURRENT–MODE MULTIPHASE SINUSOIDAL OSCILLATOR

The presented MCDCTA simplifies the design of conventional MSO circuit greatly. The realization of the proposed current-mode MSO structure using only one MCDCTA, one grounded resistor and n grounded capacitors is shown in Fig. 2. The use of grounded passive components is suitable for an integration point of view and is helpful for easing the elimination of various parasitic capacitance effects [33]. From Fig. 2 and equations (1)-(3), by routine analysis, we can write

$$\begin{aligned} I_{x1} &= g_{m1} I_{C_1} \frac{1}{sC_1}\,, \\ I_{x2} &= g_{m2} I_{C_2} \frac{1}{sC_2}\,, \\ &\vdots \\ I_{xn} &= g_{mn} I_{C_n} \frac{1}{sC_n}\,, \\ I_{x(n+1)} &= g_{m(n+1)} I_R R\,. \end{aligned} \tag{8}$$

$$\begin{aligned} I_{C_1} &= I_z - I_{x_1}\,, \\ I_{C_2} &= I_{x_1} - I_{x_2}\,, \\ &\vdots \\ I_{C_n} &= I_{x_{(n-1)}} - I_{x_n}\,, \\ I_R &= I_{x_n}\,. \end{aligned} \tag{9}$$

$$\begin{aligned}
\frac{I_{x1}}{I_{x(n+1)}} &= -\frac{1}{1+(sC_1/g_{m1})}\,,\\
\frac{I_{x2}}{I_{x1}} &= \frac{1}{1+(sC_2/g_{m2})}\,,\\
&\vdots\\
\frac{I_{xn}}{I_{x(n-1)}} &= \frac{1}{1+(sC_n/g_{mn})}\,,\\
\frac{I_{x(n+1)}}{I_{xn}} &= Rg_{m(n+1)}\,.
\end{aligned} \tag{10}$$

By summing the above equations, we draw

$$L(s) = -Rg_{m(n+1)} \prod_{i=1}^{n} \frac{1}{1+(sC_i/g_{mi})}\,. \tag{11}$$

Assuming that $g_{mi} = g_m\,(1 \le i \le n)$ and $C_i = C$ $(1 \le in)$, the open loop gain $L(s)$ of the designed circuit in Fig. 2 can be given by

$$L(s) = -Rg_{m(n+1)}\Big[\frac{1}{1+s(C/g_m)}\Big]^n \tag{12}$$

where $Rg_{m(n+1)}$ is the current amplifier gain, $g_{m(n+1)}$ which is tunable by adjusting the bias current $I_{B(n+1)}$ is the $(n+1)$th transconductance. In order to keep sinusoidal oscillations at frequency $\omega_0 = 2\pi f_0$, the Barkhausen criteria must be met such that

$$L(j\omega_0) = -\frac{Rg_{m(n+1)}}{\big[1+j\omega_0(C/g_m)\big]^n} = 1\,, \tag{13}$$

that is

$$\Big[1+j\omega_0\frac{C}{g_m}\Big]^n + \big(Rg_{m(n+1)}\big) = 0\,. \tag{14}$$

We have

$$\Delta\varphi = \frac{\pi}{n} = \tan^{-1}\frac{\omega_0 C}{g_m}\,. \tag{15}$$

Here, $\Delta\varphi$ is the phase shift of the each transconductance stage. According to the provided MSO scheme and equation (13–15), there have n output currents I_{oi}, $(i = 1, 2, 3, \ldots, n)$ and each shifted phase is $180°/n$. The size and the phase of the system loop gain are written as below.

$$|(j\omega_0)| = 1 \tag{16}$$

and

$$\angle\,[L(j\omega_0)] = 2k\pi\,, \quad k = 0, 1, 2, \ldots \tag{17}$$

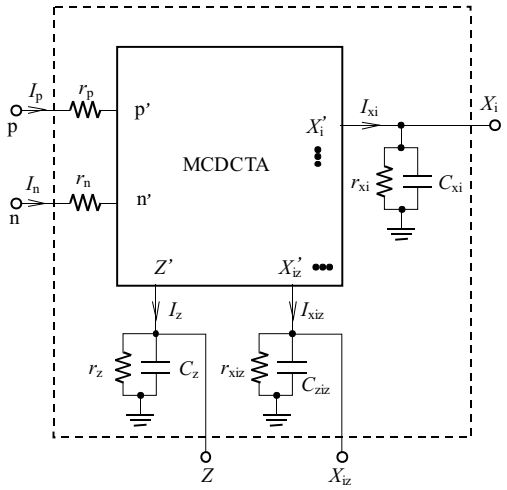

Fig. 3. Simplified equivalent circuit of the non-ideal MCDCTA

Combining the above equations (14)–(17), the oscillation condition (OC) and the oscillation frequency (OF) results are expressed respectively by

$$\text{OC: } K = \Big[1+\Big(\frac{\omega_0 C}{g_m}\Big)^2\Big]^{(n/2)} = Rg_{m(n+1)} \tag{18}$$

and

$$\text{OF: } \omega_0 = \frac{g_m}{C}\tan\frac{\pi}{n}\,. \tag{19}$$

Through replacing ω_0 into (18), the oscillation condition can be obtained as

$$\text{OC: } \Big[1+\tan^2\frac{\pi}{n}\Big]^{(n/2)} = Rg_{m(n+1)} \ge 1\,. \tag{20}$$

Equation (19) shows that the oscillation frequency ω_0 of MSO can be electronically, linearly and independently controlled by transconductance g_m without obstructing condition of oscillation. Moreover, it is easy to seen that, from (20), the oscillation condition (OC) of oscillator depends on the parameter $Rg_{m(n+1)}$. And by employing an inverted version of the output current of the MCDCTA, the even-phase $(2n = 6, 10, 14, \ldots)$ output currents $(-I_{O1}, -I_{O2}, \ldots, -I_{On})$ are also achieved from the same framework. Thus, the proposed circuit of Fig. 3 can be oscillated when n is odd or even number.

Here, it may be stated that the presented MSO can be realized without any constraints on the component values, and it exhibits both low-input and high-output impedance characteristics, which will be more convenient in terms of cascading and connecting to other networks. Comparing conventional MSO circuit, it also greatly reduces the number of active and passive elements and power consumption.

4 NON–IDEAL ANALYSIS

For a complete analysis of the proposed circuit, the following non-idealities of MCDCTA must be considered. Figure 3 shows the simplified equivalent topology that will be used to represent the behavior of the non-ideal MCDCTA. Additionally, for the analysis of non-ideal

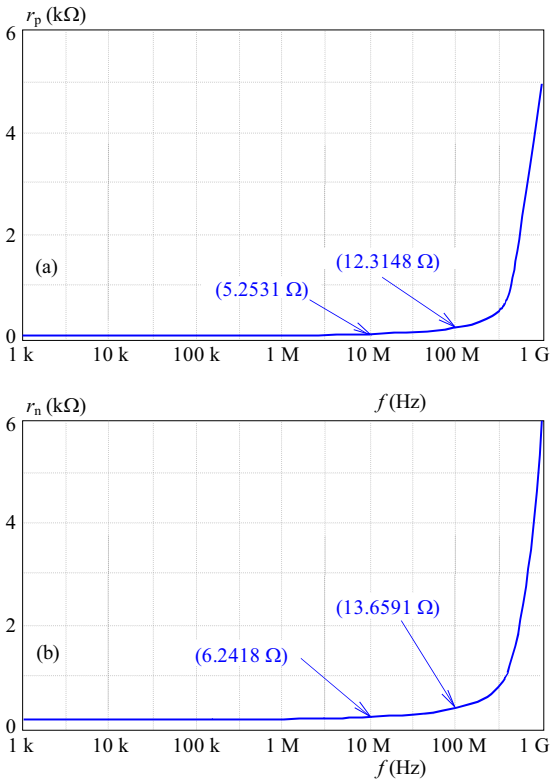

Fig. 4. Frequency characteristics of input terminal resistances: (a) — p terminal; (b) — n terminal

case, the MCDCTA's current and voltage nature can be given through the following equations.

$$I_z = \alpha_p I_p - \alpha_n I_n\,,\ I_{xiz} = \gamma_i g_{mi} V_{x(i-1)z}\,,\ I_{xi} = \beta_i I_{xiz}\,, \tag{21}$$

$$\alpha_p = \frac{g_{m6}g_{m7}}{g_{m13}g_{m14}}\,\frac{g_{m5}g_{m10}r_{o57}}{g_{m5}+g_{m11}+g_{m5}g_{m10}r_{o57}}\,, \tag{22}$$

$$\alpha_n = \frac{g_{m3}g_{m8}r_{o56}}{g_{m3}+g_{m9}+g_{m3}g_{m8}r_{o56}} \tag{23}$$

where $\alpha_p\big(\alpha_p = 1-\varepsilon_p, |\varepsilon_p| \ll 1\big)$ and $\alpha_n\big(\alpha_n = 1-\varepsilon_n, |\varepsilon_n| \ll 1\big)$ indicate the parasitic current transfer error from p and n to z terminal. $\gamma_i\big(\gamma_i = 1-\varepsilon_c, |\varepsilon_c| \ll 1\big)$ denotes the parasitic transconductance tracking error from X_{iz} to $X_{(i+1)z}$ terminal. $\beta_i\big(\beta_i = 1-\varepsilon_d, |\varepsilon_d| \ll 1\big)$ is the parasitic current transfer error from X_{iz} to X_i terminal. It is clearly seen that there are parasitic resistance r_p, r_n (ideally equal to zero) at terminals p and n, and parasitic resistance r_{xiz}, r_{xi} (ideally equal to infinity) and parasitic capacitance C_{xiz}, C_{xi} (ideally equal to zero) from the high-impedance terminals z, X_{iz} and X_i of the MCDCTA to the ground (assuming $C_i' = C + C_{xiz}, (1 \le i \le n), C_{(n+1)}' = C_{x(n+1)z}$). Z_i' is an non-ideal impedance connected at the terminal z and X_{iz}. Hence, taking into account all the above non-ideal MCDCTA characteristics and its parasitic components except for the parasitic resistance and parasitic capacitance at terminals X_i, we can rewrite the modified current transfer functions of Fig. 2 as

$$\begin{aligned}
I_{x1z} &= \gamma_1 g_{m1} V_z = \gamma_1 g_{m1}(-\alpha_p I_{x(n+1)} - \beta_1 I_{x1z}) Z_1'\,,\\
I_{x2z} &= \gamma_2 g_{m2} V_{x1z} = \gamma_2 g_{m2}(I_{x1z} - \beta_2 I_{x2z}) Z_2'\,,\\
&\vdots\\
I_{xnz} &= \gamma_n g_{mn} V_{x(n-1)z}\\
&= \gamma_n g_{mn}(I_{x(n-1)z} - \beta_n I_{xnz}) Z_n'\,,\\
I_{x(n+1)z} &= \gamma_{(n+1)} g_{m(n+1)} V_{xnz}\\
&= \gamma_{(n+1)} g_{m(n+1)} I_{xnz} Z_{(n+1)}'\,.
\end{aligned} \tag{24}$$

The parameters Z_i' and $Z_{(n+1)}'$ of (24) are seen to be

$$\begin{aligned}
Z_i' &= \frac{1}{1/r_{xiz} + sC_i'} \quad (1 \le i \le n)\,,\\
Z_{(n+1)}' &= \frac{1}{sC_{(n+1)}' + 1/r_{x(n+1)z} + 1/R}\,.
\end{aligned} \tag{25}$$

One gets

$$\begin{aligned}
L(s) = -\gamma_{(n+1)} g_{m(n+1)} &\frac{1}{\alpha_p \prod_{i=1}^{n} \beta_i}\\
&\times \frac{1}{1 + \big((1/r_{x1z}) + sC_1'\big)/\big(\gamma_1 g_{m1}\alpha_p\beta_1\big)}\\
&\times \frac{1}{sC_{(n+1)}' + \big(1/r_{x(n+1)z}\big) + 1/R}\\
&\times \prod_{i=2}^{n} \frac{1}{1 + \big((1/r_{xiz}) + sC_i'\big)/\big(\gamma_i g_{mi}\beta_i\big)}\,.
\end{aligned} \tag{26}$$

Since the value of r_{xiz} is in the order of $M\Omega$, thus for an external resistor of value $R \ll r_{xiz}$ connected at this terminal, $R \,||\, r_{x(n+1)z} \cong R$. Similarly, the value of C_{xiz} is about zero, so $C_i' = C$, $(1 \le i \le n)$, $C_{(n+1)}' = 0$. Assuming $r_{x1z} = r_{x2z} = \cdots = r_{x(n+1)z} = r_{xz}$, $\beta_1 = \beta_2 = \cdots = \beta_n = \beta$, $\gamma_1 = \gamma_2 = \cdots = \gamma_{(n+1)} = \gamma$. Re-analysis of the proposed MSO circuit in Fig. 2 employing (26) with $r_{xz} \gg 1/sC$, $R \ll 1/sC_{x(n+1)z}$ the modified oscillation condition and oscillation frequency can be rewritten by the following equations.

$$L(s) \cong -R g_{m(n+1)} \frac{\gamma}{\alpha_p \beta^n} \Big(\frac{1}{1 + \big(sC/\gamma\beta g_m\big)}\Big)^n, \tag{27}$$

$$\text{OC:}\ \ R g_{m(n+1)} \frac{\gamma}{\beta^n \alpha_p} \cong \Big[1 + \tan^2 \frac{\pi}{n}\Big]^{(n/2)} \tag{28}$$

$$\text{OF:}\ \ \omega_0 \cong \frac{\gamma\beta g_m}{C} \tan \frac{\pi}{n}\,. \tag{29}$$

From the above equations, it is easy to show that the oscillation condition is mainly affected by the current transfer errors (α_p, β) and transconductance tracking error (γ) of the MCDCTA in non-ideal case. But the influence of these errors can be easily corrected through adjusting the

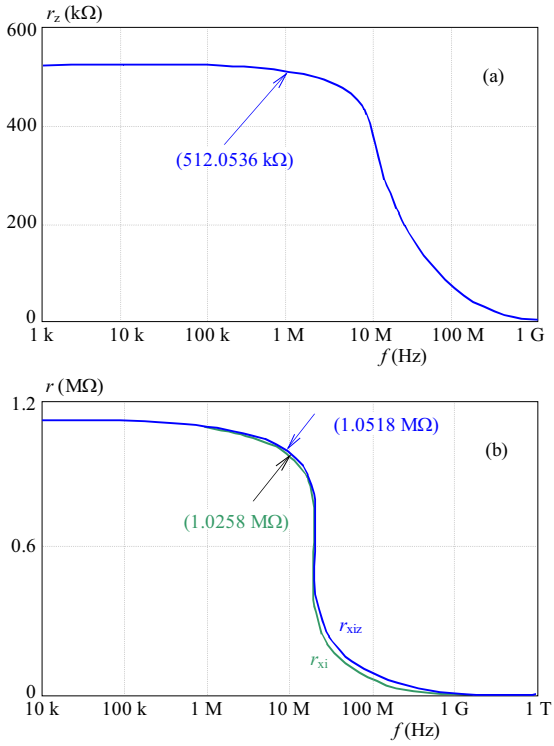

Fig. 5. Frequency characteristics of output terminal resistances: (a) — z terminal; (b) — X_i and X_{iz} terminals

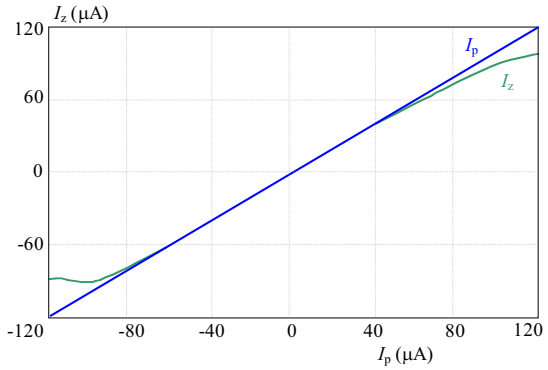

Fig. 6. The change of z terminal current according to the p terminal current

value of $Rg_{m(n+1)}$. Additionally, it is evident that ω_0 is slightly changed from the ideal case by the factor of $\gamma\beta$. To offset this effect, it still can be tuned by the g_m-value.

According to equation (29), the active and passive sensitivities of the oscillator in non-ideal case are deduced as

$$S_{\alpha_p}^{\omega_0} = S_{\alpha_n}^{\omega_0} = 0\,, \quad S_{\gamma_i}^{\omega_0} = S_{\beta_i}^{\omega_0} = S_{g_m}^{\omega_0} = -S_C^{\omega_0} < 1\,. \quad (30)$$

It is noteworthy from (30) that the absolute magnitude values of all ω_0 sensitivities are about equal to 0 or 1. It is easy to see that parasitics has been alleviated through this cascaded structure considerably.

5 SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the performances of the proposed circuits, the CMOS-based MCDCTA circuit (two transconductance stages) was simulated with the parameters of the TSMC 0.18 μA transistor model in PSPICE circuit simulation program. The supply voltages used are VDD = −VSS = 1.0 V, and the bias currents I_o and I_{Bi} are selected as 30 μA and 50 μA respectively. The dimensions of the CMOS transistors are listed in Table. 2 (partial).

Table 2. Dimensions of the CMOS transistors

COMS TRANSISTORS	W(um)/L(um)
M1-M19,M24-M39,M44-M55	24/1
M20-M21,M40-M41	10/0.6
M22-M23,M42-M43,	10/1
M56-M57, M62-M67,M70-M75	36/0.6
M58-M59	81/0.6
M60-M61,M68-M69	63/0.6

Table 3. Simulated performances of the proposed MCDCTA

Design parameters	Simulation results
Technology	TSMC 0.18 um
The supply voltages	+VDD = −VSS = 1.0 V
Power dissipation	1.12mW ($I_p = I_n = 0$ A)
−3 dB bandwidth	410 MHz(I_z/I_p),413 MHz(I_z/I_n)
	402 MHz(I_{xi}/I_p),401 MHz (I_{xi}/I_n)
	402 MHz(I_{xiz}/I_p),408 MHz (I_{xiz}/I_n)
Transconductance linear range	0.12 mS–1.0 mS
Input bias current range	−200 μA to 200 μA
$r_p, r_n, r_z, r_{xi}, r_{xiz}$	5.2531 Ω, 6.2418 Ω, 512.0536 KΩ
	1.0258 MΩ, 1.0518 MΩ
α_p, α_n	0.9816, 0.9815

The input impedance of the p and n terminals are given in Fig. 4(a) and (b), respectively. We can seen that MCDCTA's input impedances compared with CDTA [12] are about zero. The output impedance at Z, X_i and X_{iz} terminals was found in Fig. 5(a) and (b), respectively. It is noted that the output impedance value at the output terminals is enough to drive the load of our application. The change of Z terminal current according to p terminal current of the MCDCTA CMOS realization is obtained in Fig. 6, when $I_{Bi} = 50\,\mu$A. So it is clearly seen that it is linear in -80 uA $< I_p <$ 80 uA and can be tuned. The −3 dB cutoff frequencies of the current gains $I_z/I_p, I_z/I_n, I_{xi}/I_p, I_{xi}/I_n, I_{xiz}/I_p$ and I_{xiz}/I_n are approximately 410 MHz, 413 MHz, 402 MHz, 401 MHz, 402 MHz and 408 MHz, as shown in Figs. 7 and 8. The measured frequency response of transconductance is shown in Fig. 9, when the bias current is 50 μA. We can seen that the transconductance of the proposed MCDCTA has a large bandwidth, which makes it suitable

Table 4. Comparison simulation results of the proposed multiphase sinusoidal oscillator to other designs

Topology	The supply voltage	Measured highest operating frequency	C_{Load}	Deviation of OF	THD
[2]	±10 V	Dozens of	0.22 uF	> 10 %	–
[3]	±1.5 V	Hundreds of	100 pF	12.51 %	1.98 %
[4]	±10 V	Hundreds of	138 pF	6.00 %	–
[9]	±10 V	Dozens of	275 pF	4.22 %	–
[11]	±12 V	Hundreds of	1 nF	3.74 %	–
[16]	±3 V	Hundreds of	1 nF	6.00 %	1.300 %
[20]	±3 V	Hundreds of	1 nF	1.60 %	1.400 %
[22]	±2.5 V	Hundreds of	100 pF	1.25 %	1.032 %
Proposed	±1.0 V	Dozens of	5.3 pF	0.86 %	0.841 %

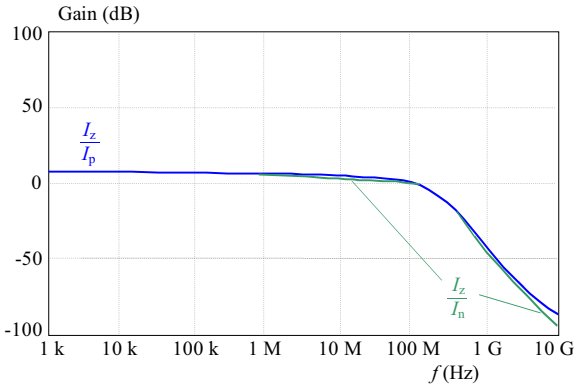

Fig. 7. Frequency responses at z output terminal

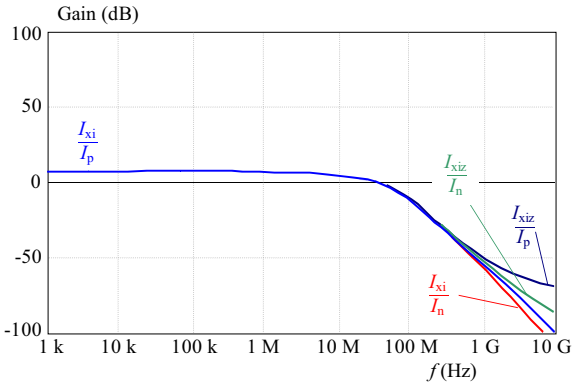

Fig. 8. Frequency responses at X_i and X_{iz} output terminals

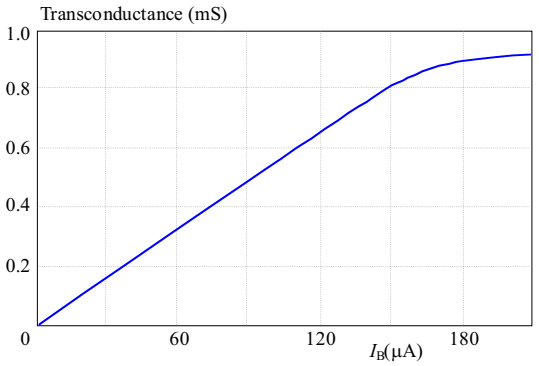

Fig. 9. Transconductance value relative to bias current (I_B)

for high frequency operations. The performance characteristics of the CMDCTA CMOS configuration are seen in Table 3.

To confirm the performance of the presented current-mode MSO system in Fig. 2, a six-phase MSO ($n = 3$) has been devised by using the proposed circuit. The proposed MSO oscillator is also simulated with PSPICE circuit simulation program. The values of the bias currents are $I_0 = 30\,\mu$A, $I_B = I_{B1} = I_{B2} = I_{B3} = 50\,\mu$A ($g_m \approx 0.32$ mS), $I_{B4} = 80\,\mu$A.

In order to avoid the parasitic effects, the external capacitors $C = C_1 = C_2 = C_3 = 5.3$ pF and resistor $R = 17.5\,\text{K}\Omega$ are used. The output waveforms and frequency spectrum obtained from the proposed MSO topology of Fig. 2 are, respectively, shown in Figs. 10 and 11. The simulated value of oscillation frequency is 14.67 MHz, which is close agreement with the calculated value of 14.80 MHz. The deviation for oscillation frequency is 0.86 %. The error is mainly due to parasitic impedances appearing at X_{iz} and X_i terminals. From the simulation results, it is noted that the phase difference of I_{o2}, I_{o3}, $-I_{o1}$, $-I_{o2}$ and $-I_{o3}$ comparing with I_{o1} were, respectively, measured as 58°, 119°, 181°, 240° and 298°. Apparently, they are very close to the theoretical predicted values. The total harmonic distortion (THD) in the output waveforms I_{o1}, I_{o2}, I_{o3} were about to 0.841 %. It is also found that the six-phase sinusoidal oscillator circuit power consumption is approximately 6.35 mW.

Figure 12 shows the adjustability of the oscillation frequency by I_B without affecting the oscillation condition, when $I_0 = 30\,\mu$A, $I_{B4} = 80\,\mu$A, $C = 5.3$ pF and $R = 17.5\,\text{K}\Omega$. Obviously, in a wide frequency range, the simulated oscillation frequency values are consistent with the calculated values. Although there is a deviation between the theoretical values and the simulation values in high bias current value region, decreasing this error can be offset through simply tuning the value of external ca-

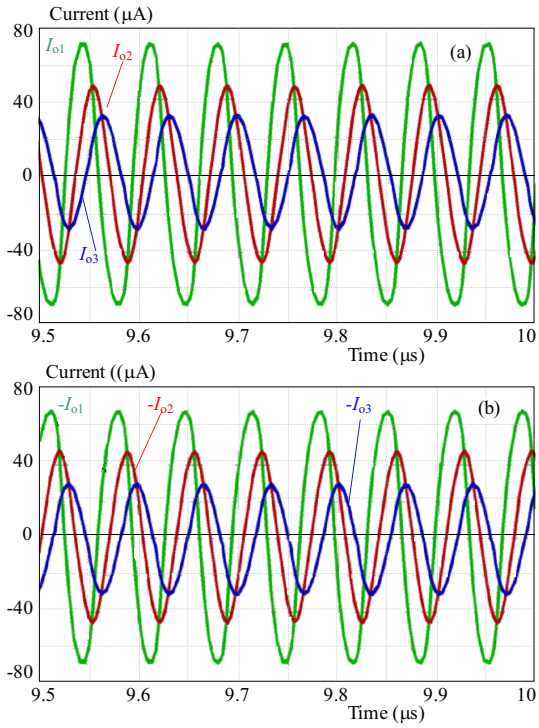

Fig. 10. Simulated results of the proposed current-mode MSO of Fig. 3: (a) — I_{O1}, I_{O2}, I_{O3}, (b) — $-I_{O1}$, $-I_{O2}$, $-I_{O3}$

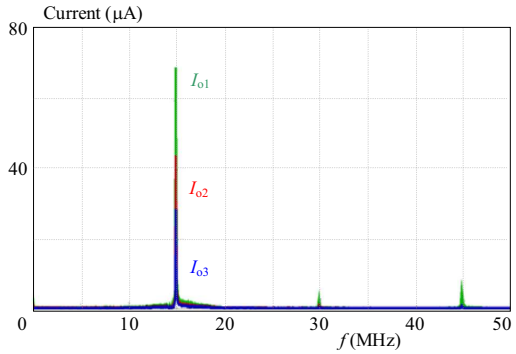

Fig. 11. Simulated spectrums of I_{O1}, I_{O2}, I_{O3}

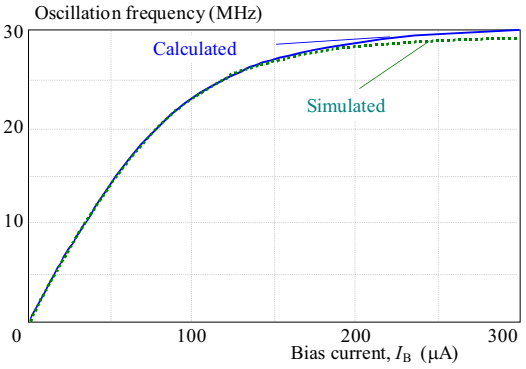

Fig. 12. The related curve of the oscillation frequency (f_0) and the bias currents I_B

pacitor. It is noted that the results of circuit simulations are in agreement with theory.

The simulation results of the proposed circuit in Fig. 3 have been compared with those reported in Table 1. The derived results are summarized in Table 4. From Table 1 and Table 4, we can see that the proposed circuit has better performance than that of the reported circuits in terms of the circuit complexity, the supply voltage, bandwidth and accuracy *etc.* It is also seen that the total harmonic distortion (THD) is very low relative to other reported MSO. Since its active device further alleviates parasitics and can avoid the influence of input impedance on the bandwidth of circuit, the presented MSO in this work enjoys comparatively high frequency.

To verify the workability of the proposed MSO, a current-mode four-phase oscillator according to the presented configuration is verified by experimentally tested. The MCDCTA active element was performed through using commercially available ICs, *ie*, AD844s (CCIIs) and CA3080Es (OTAs) in experiment. The DC supple voltages were taken as ±12 V. In experiments, working resistor, capacitor and bias current values were confirmed as follows:

$$R = 24.6\,\mathrm{k\Omega}\,,\ C = 1\,\mathrm{nF},\ I_B = 125\,\mathrm{uA},\ I_{B3} = 215\,\mathrm{uA}.$$

The oscillation frequencies obtained by experiments is about 217.39 KHz, which is deviated from the calculated value (216.18 KHz) by 0.56 %.

6 CONCLUSION

In this paper, a new active component, MCDCTA and its application to realization current mode multiphase sinusoidal oscillator have been presented. The proposed element which enjoys simple configuration, low-input and high-output impedance, wide bandwidth and versatility can be operated at low power supply voltage. The presented MSO which only adopts a single active component (MCDCTA) and few grounded passive elements decrease the number of elements, chip area and power consumption consumedly. Moreover, its parameters can be determined by varying the bias current of MCDCTA. The performances of the presented circuits have been proven by the simulation and experimental results. Based on these advantages, this novel active element and its application circuits are very appropriate to implement in IC fabrication fields: Instrumentation and measurement systems, RF transmitter/receiver, wireless communication devices *etc.* It is also expected to be useful for the designed active component in analog signal processing besides the oscillator circuits.

Acknowledgment

The authors would like to thank the reviewers for valuable comments and helpful suggestions. This work is supported by the National Natural Science Foundation of China (No. 61274020) and the natural science foundation of Hunan Province (No. 14JJ7026) and the Open Fund Project of Key Laboratory in Hunan Universities (No. 13K015).

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Received 21 April 2014

Chunhua Wang was born in Yongzhou, China, in 1963. He received the BC degree from Hengyang Teacher's College, Hengyang, China, in 1983, the MS degree from Physics Department, Zheng Zhou University, Zheng Zhou, China, in 1994, and the PhD degree from School of Electronic Information and Control Engineering, Beijing University of Technology, Beijing, China, in 2003. He has been a professor of School of Computer and Communication, Hunan University, Changsha, China from 2004. His interests include analog integrated circuit design, RFIC design and wireless communication.

Hairong Lin was born in Changsha, China, in 1988. He received the BC degree from Huaihua College, Huaihua, China. He is currently studying in Hunan University for master degree. His research areas are mainly in analog integrated circuits, RFIC design and analog signal processing.