DE GRUYTER OPEN

Journal of ELECTRICAL ENGINEERING, VOL. 66, NO. 5, 2015, 250–256

DESIGN OF A 5–BIT FULLY PARALLEL ANALOG TO DIGITAL CONVERTER USING COMMON GATE DIFFERRENTIAL MOS PAIR–BASED COMPARATOR

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This paper presents a novel comparator structure based on the common gate differential MOS pair. The proposed comparator has been applied to fully parallel analog to digital converter (A/D converter). Furthermore, this article presents 5 bit fully parallel A/D Converter design using the cadence IC5141 design platform and NCSU(North Carolina State University) design kit with $0.18\,\mu$m CMOS technology library. The proposed fully parallel A/D converter consist of resistor array block, comparator block, 1-n decoder block and programmable logic array. The 1-n decoder block includes latch block and thermometer code circuit that is implemented using transmission gate based multiplexer circuit. Thus, sampling frequency and analog bandwidth are increased. The INL and DNL of the proposed fully parallel A/D converter are $(0/+0.63)$ LSB and $(-0.26/+0.31)$ LSB at a sampling frequency of 5 GS/s with an input signal of 50 MHz, respectively. The proposed fully parallel A/D Converter consumes 340 mW from 1.8 V supply.

K e y w o r d s: fully parallel A/D converter, common gate differential MOS pair, transmission gate based multiplexer circuit, high speed A/D converter

1 INTRODUCTION

Nowadays, Analog to Digital Converters are widely used in mobile phones, cameras, optical and wireless communications systems and all of the systems that need digital knowledge. Because of increasing usage of digital signal processing, wireless communication systems and broadband systems, the demands for low resolution and high speed fully parallel A/D Converters are increasing [1–4].

The fully parallel A/D Converter is known as the fastest type of A/D Converters structure among the designers. Due to the fact that all the comparators operate in parallel, conversion of digital data obtain the result in one clock period and the fully parallel A/D Converter structure has a simple block diagram, it is the most popular converter. This architecture have been proposed as a solution for sampling rate of multi GS/s and resolution of 4-6 bits [5, 6]. Although fully parallel A/D Converter has a low resolution, there are some disadvantages according to the other types of A/D Converter structure. Some of them are high power consumption and large chip area. Especially, due to increasing resolution of fully parallel A/D Converter, input capacitance of this system, chip area and power consumption become larger [7–11].

The block diagram of the fully parallel A/D Converter architecture is shown in Fig. 1. The comparator is a circuit that compares the applied analog input voltage to input of comparator with quantization voltage that is obtained by resistance array.

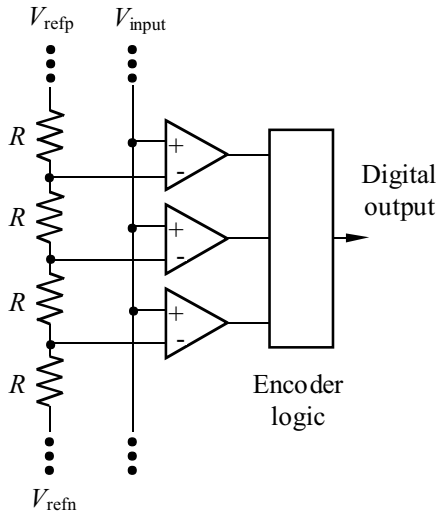

Fig. 1. The block diagram of the fully parallel A/D Converter architecture

At this transition point, according to whether analog input signal is higher or smaller than quantization voltage, analog input signal converts to digital code. This conversion of input signal is completed only one cycle of the sampling clock signal.

As we know, the design of comparator circuit for fully parallel A/D Converter architecture is one of the most important components that affect all the system [12–14].

Effective chip area, input impedance, analog input voltage range and power consumption of comparator are very important for this system that obtained with each other parallel connection of comparator [13]. Therefore, many different comparator circuits in the literature have been widely used. Some comparator structure which don't

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DOI: 10.2478/jee-2015-0041, Print ISSN 1335-3632, On-line ISSN 1339-309X

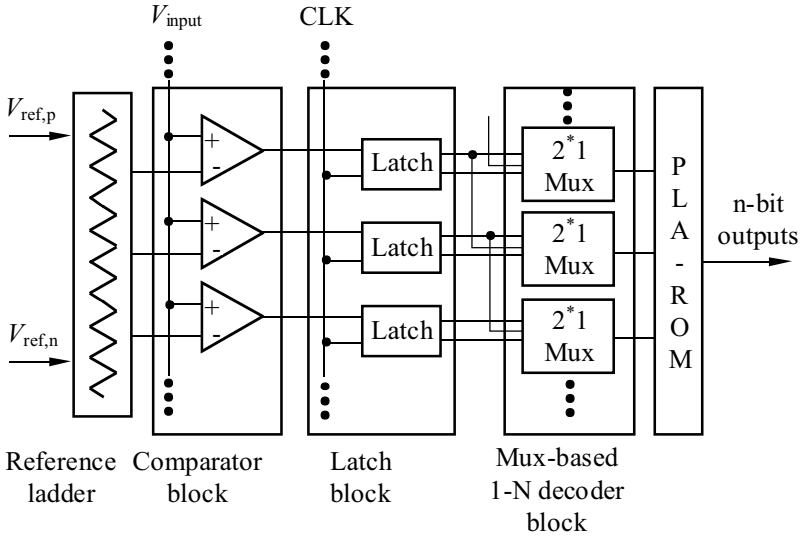

Fig. 2. The block diagram of the proposed fully parallel A/D Converter

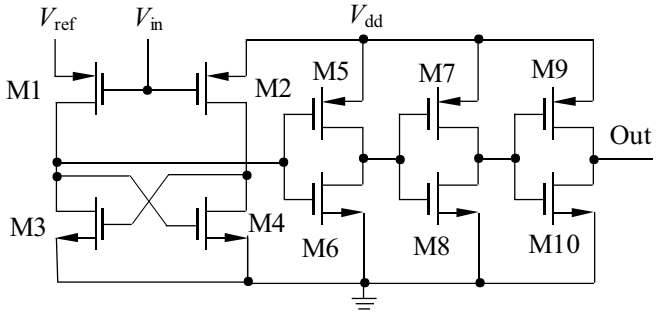

Fig. 3. Schematic of the proposed comparator circuit

require resistance array for quantization voltage have been proposed for low power consumption [15]. Auto-zeroing technique comparator structure has been proposed to reduce the offset voltage [16–18]. Latched comparator structure is used to solve kickback noise problem [14, 19].

The aim of this paper is to offer a novel comparator structure for fully parallel A/D Converter. The used structure as comparator is consist of Common Gate Differential MOS Pair (CGDMP) and two-cross coupled MOSFETs. The digital block of proposed fully parallel A/D Converter includes latch circuits, multiplexer based $1-n$ decoder and programmable logic array (pla-rom).

This article is organized as follows: The architecture of the proposed fully parallel A/D Converter is introduced in Part 2. Part 3 shows the post simulation results. Finally, conclusion is shown Part 4.

2 FULLY PARALLEL A/D CONVERTER STRUCTURE AND DESIGN BLOCKS

Figure 2 shows the block diagram of the proposed fully parallel A/D Converter. It consists of resistance array block, comparator block, latch block, multiplexer based 1-n decoder block and programmable logic array. In this study, it has two main features. These are CGDMP based comparator block and 2*1 multiplexer based 1-n decoder block.

2.1 The Proposed Comparator Structure

In this study, the schematic of proposed comparator structure is shown in Fig. 3. The circuit consists of Common-Gate Differential MOS Pair (CGDMP) that includes two PMOS transistor, two cross-coupled NMOS transistor, push-pull inverter circuit and digital buffer circuit.

There are two modes of operation for two cross-coupled NMOS transistor. In the first mode, positive feedback isn't active. In this mode, M3 and M4 drain voltage is obtained by applied input signal. In the second mode, according to the drain voltage of M3 and M4, outputs of two cross-coupled NMOS transistor are produced. One of these outputs is high and the other is low [20].

In the proposed comparator circuit, if analog input (Vin) is higher than reference voltage (Vref), M1 MOSFET is in the cutoff region. At the same time, as long as the analog input (Vin) is lower than the supply voltage (Vdd), gate voltage of M3 MOSFET is produced by the drain current of M2. However, because of having no voltage on drain of M3, M3 remains on the cutoff region. Therefore, drain voltage of M3 is logic-0 input. Logic-0 input is converted to logic-1 by the inverter circuit (M5-M6 pair). If analog input is lower than reference voltage, M1 MOSFET begins to operate. Thus, the drain and gate voltage of M3 are obtained. The obtained drain voltage of M3 will be logic-1 level. Logic-1 input is converted to logic-0 by the inverter circuit (M5-M6 pair). This comparison process will be completed. The last stage of comparator is a basic digital buffer circuit (M7,M8,M9,M10). The transistor aspect ratios (W(Width)/L(Length)) of MOS devices used in the digital buffer circuit must be large enough to obtain the best output digital voltage. Fig. 4 shows the DC analysis result of the comparator circuit.

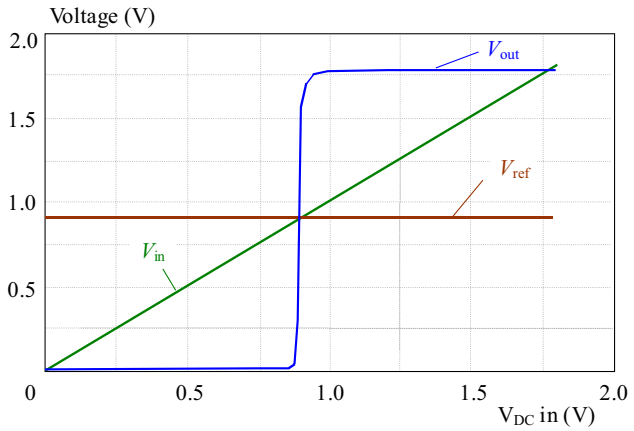

Fig. 4. The DC analysis result of the comparator

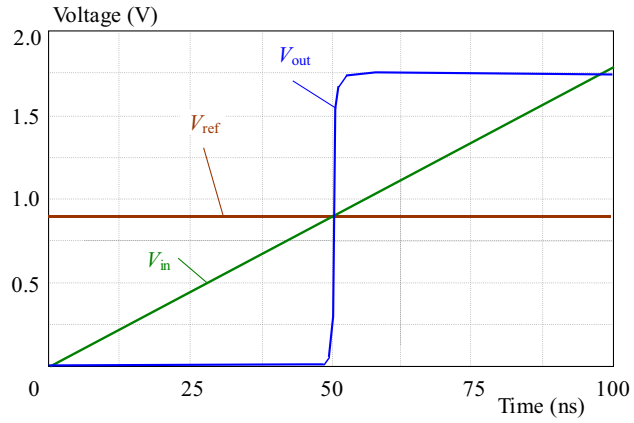

Fig. 5. Comparator output for $f_{\text{in}} = 10$ MHz

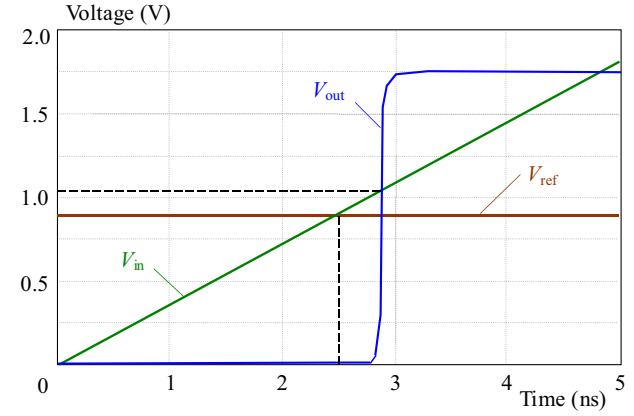

Fig. 6. The delay time of comparator for $f_{\text{in}} = 200$ MHz

Figure 5 shows comparator output for a 10 MHz input frequency. The simulated delay time of the comparator circuit is, 383 ps for a 200 MHz input frequency, shown in Fig. 6. Figure 7 shows bandwidth for proposed comparator circuit. According to the AC simulation, the bandwidth of proposed comparator is 340 MHz.

2.2 The Encoder Logic Block

The encoder logic block consists of dynamic latch circuit, 1-n code decoder and programmable logic array (pla-rom). Figure 8 shows the used dynamic latch circuit for the proposed fully parallel A/D Converter. According to the state of used clock signal, the latch circuit either transmits input voltage logic level to the output or holds the last output logic level. Thus, the control between the analog and digital parts of the fully parallel A/D Converter is obtained [12].

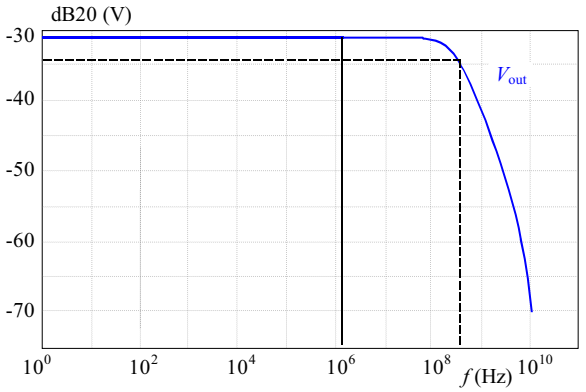

Fig. 7. The bandwidth of proposed comparator circuit

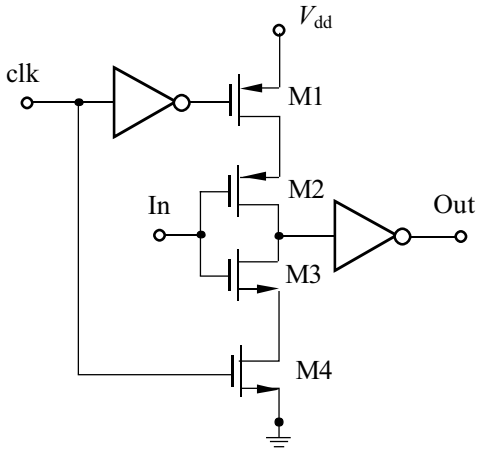

Fig. 8. The dynamic latch circuit

Thermometer code circuits are using to determine the border of logic level "1" and logic level "0" array. Transmission gate based multiplexer circuit as a thermometer code circuit is used in this proposed fully parallel A/D Converter.

In this structure, the inputs and control signal of multiplexer circuit should be selected carefully to obtain the necessary digital output.

Multiplexer based thermometer code circuit has less layout area and number of the critical path [21]. The number of multiplexer circuits required for "n" bit fully parallel A/D Converter is $2^n - 1$ for this structure. Figure 9 shows the used transmission gate based multiplexer circuit and the block diagram of $1 - n$ code decoder.

The pla-rom is using to convert $1 - n$ code to a binary code. This structure uses PMOS transistors working in a linear region as much as the number of bits(n), and $2^n - 1$ number of NMOS transistor array that is like binary

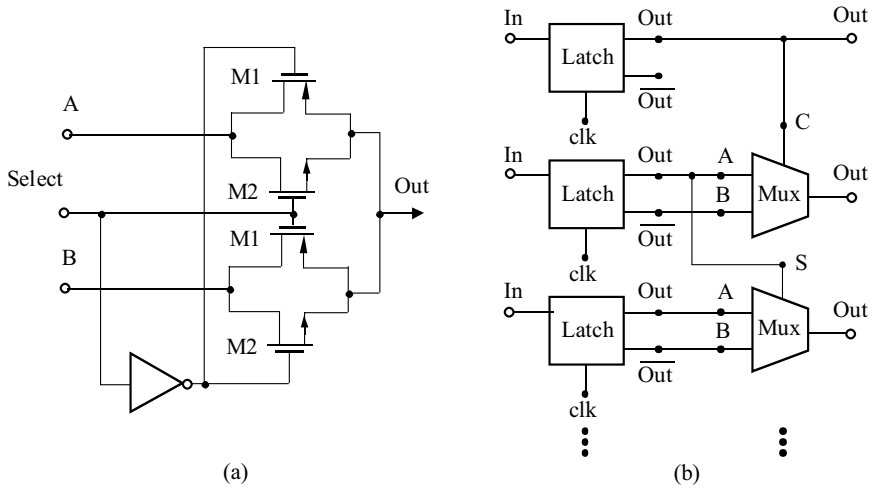

Fig. 9. (a) — Transmission gate based multiplexer circuit, (b) — The connection of between Latch and Multiplexer circuits

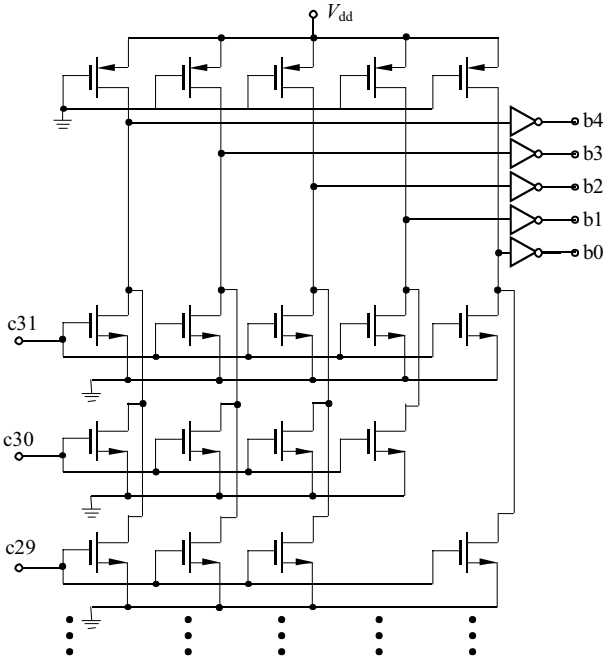

Fig. 10. The part of pla-rom structure

code sequence. The best advantage of this structure is fully parallel. One of the disadvantage of this structure is bubble error. Figure 10 shows the part of pla-rom.

3 POST–LAYOUT SIMULATION RESULTS

All the simulation results were obtained by using Cadence IC5141 design platform and NCSU (North Carolina State University) design kit with 0.18 μm CMOS technology library. The performance of the proposed fully parallel A/D Converter was evaluated with post-layout. A ramp-shaped analog input signal of between +0.3 V and 1.55 V is applied to the proposed fully parallel A/D Converter. The supply voltage is 1.8 V. Figure 11(a) shows the DC analysis results and Fig. 11(b) shows the corresponding linearity plots for DC results. The corresponding linearity plots (Differential Nonlinearity (DNL) and Integral Nonlinearity (INL)) are obtained by using a Matlab platform, as used in [22]. According to DNL and INL curves, DNL values range from −0.15 LSB to +0.25 LSB while INL values are −0.12 LSB and +0.5 LSB. Both are lower than 1 LSB.

For the output signal of the input frequency for 50 MHz and the digital clock frequency for 5 GS/s is shown Fig. 12(a). According to the transient simulation results, DNL and INL plots are obtained and shown Fig. 12(b).

The obtained DNL and INL values are lower 1LSB. INL minimum and maximum values are 0LSB and +0.63LSB, DNL values are −0.26LSB and +0.31LSB. Furthermore, the digital clock frequency is kept constant and analog input frequency is changed between 1 MHz and 200 MHz. DNL and INL values obtained by using this simulation. Figure 13 shows the worst-case linearity error values with respect to range values that is sum of the INL and DNL maximum and minimum values.

The obtained digital output waveforms for ramp-shaped analog signal for $f_{\text{in}} = 50$ MHz and $f_{\text{clk}} = 5$ GS/s is applied to an ideal 5 bit digital-to-analog converter (D/A Converter). The reconstructed output signal is shown Fig. 14. Figure 15 shows the reconstructed output signal for sinusoidal analog input for $f_{\text{in}} = 50$ MHz and $f_{\text{clk}} = 5$ GS/s.

4 CONCLUSIONS

In this paper, a novel comparator circuit, which consists of Common-Gate Differential MOS Pair(CGDMP) that includes two PMOS transistor, two cross-coupled NMOS transistor, push-pull inverter circuit and digital buffer circuit, is presented. The proposed comparator structure is used to 5-bit 5GS/s fully parallel A/D Converter. As a result of post-layout for DC simulations, INL is $(+0.5/-0.12)$LSB, and DNL is $(+0.25/-0.15)$LSB. For the operating at 5 GS/s with 200 MHz input signal frequency, INL is $(+1.05/-0.58)$LSB, and DNL is $(+0.7/-0.1)$LSB. The proposed comparator circuit

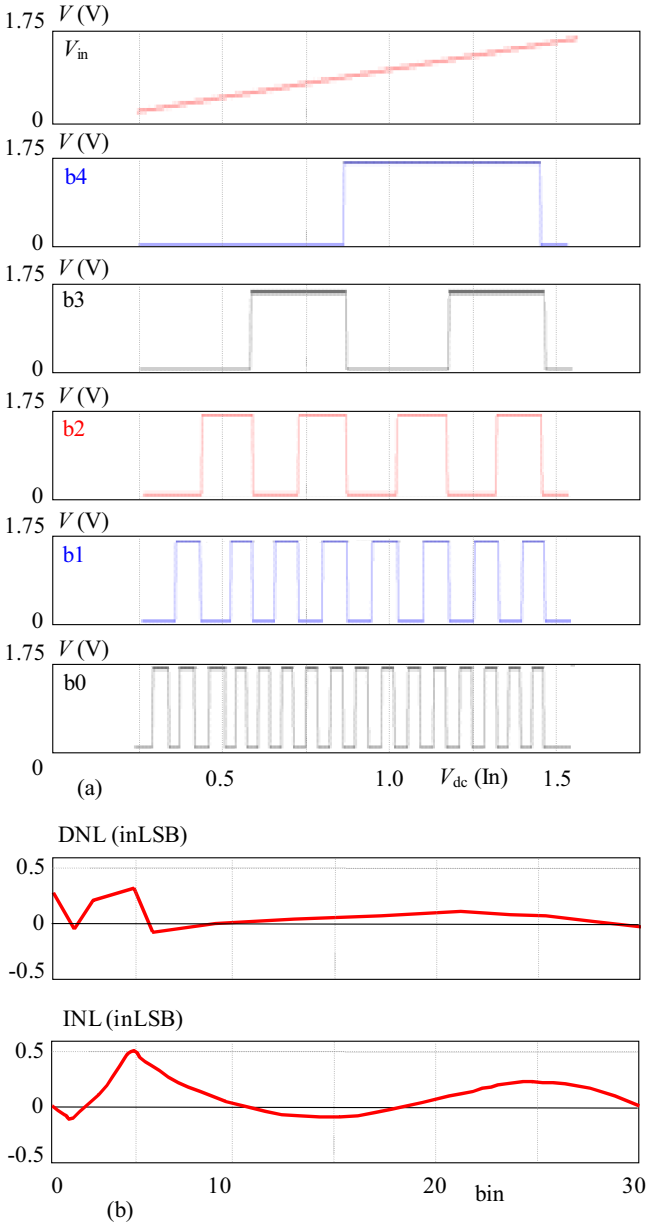

Fig. 11. (a) — The 5 bits DC simulation results, (b) — DNL: average 7.8×10^{-17}, standard deviation 0.1, range 0.4, and INL: average 0.082, standard deviation 0.15, range 0.62, curve plots based on DC results

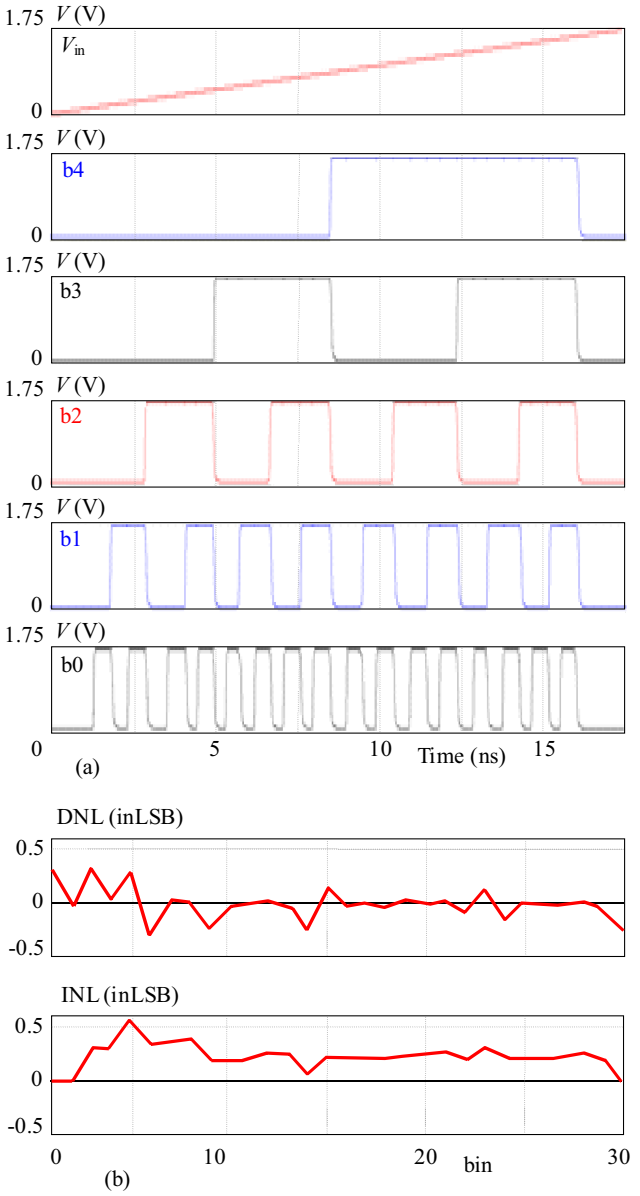

Fig. 12. (a) — The 5 bits results for $f_{in} = 50$ MHz, $f_{clk} = 5$ GS/s, (b) — DNL: average 1.9×10^{-17}, standard deviation 0.14, range 0.58, and INL: average 0.26, standard deviation 0.13, range 0.63, plots for $f_{in} = 50$ MHz ramp, $f_{clk} = 5$ GS/s

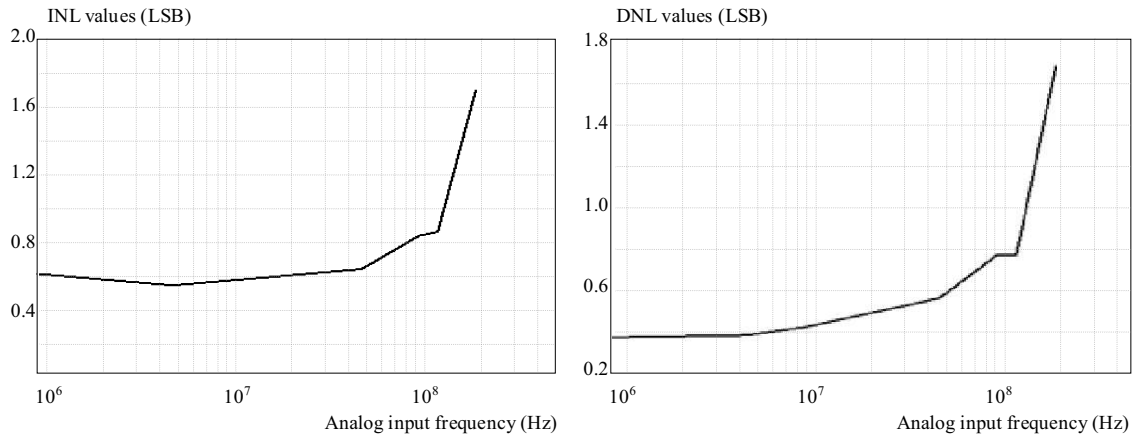

Fig. 13. The worst-case DNL and INL errors for different analog input frequencies

Table 1. The performance summary and comparison of the proposed fully-parallel Analog to digital converter

Performance Parameters	This work	[2]	[3]	[16]	[23]	[24]	[25]
Technology	TSMC 0.18μm CMOS	TSMC 0.13μm CMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	TSMC 0.18μm CMOS	TSMC 0.13μm CMOS
Resulotion (bits)	5	5	5	6	5	5	5
Supply Voltage (V)	1.8	1.2	1.8	1.2	1.2	1.8	1.2
INL(LSB)	$(+0.5/-0.12)$ (DC) $(+0.7/-1)$ ($f_{in} = 200$ MHz)	0.6	0.58	0.35	0.65 ($f_{in} = 1.2$ MHz)	0.70	0.65
DNL(LSB)	$(+0.25/-0.15)$ (DC) $(+1.07/-0.58)$ ($f_{in} = 200$ MHz)	0.42	0.43	0.4	0.55 ($f_{in} = 1.2$ MHz)	0.48	0.60
Power Consumption (mW)	340	120	8	182	300	180	180
Sampling Frequency (GHz)	5	3.2	0.5	1	4.8	1	4.2
Active Area (mm^2)	0.046	0.18	0.132	1.44	–	–	0.16
Calibration	No	–	–	–	–	Yes	–
Architecture	Flash	Flash	Flash	Flash	Time-Interleaved	Flash	Flash

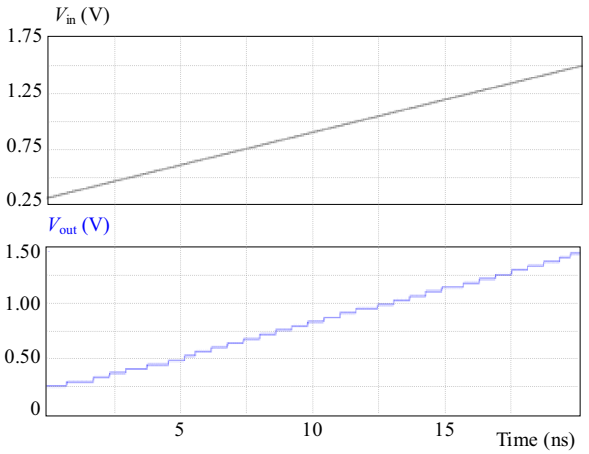

Fig. 14. The output of ideal D/A converter for an analog ramp input signal, $f_{in} = 50$ MHz, $f_{clk} = 5$ GS/s

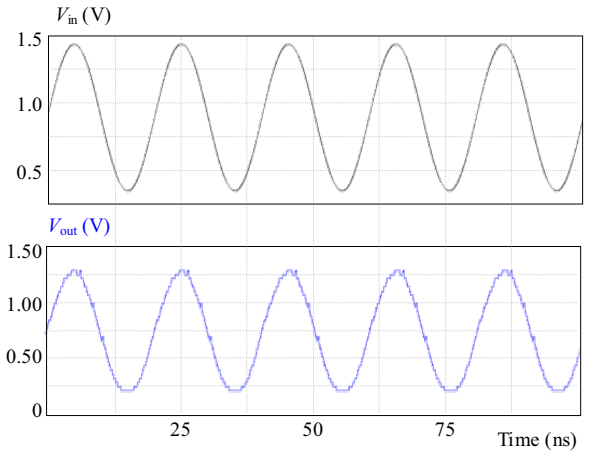

Fig. 15. The output of ideal D/A converter for an sinusoidal input signal, $f_{in} = 50$ MHz, $f_{clk} = 5$ GS/s

can be used different A/D Converter types that require high-speed clock and wide-bandwidth. The only disadvantage of the proposed comparator circuit is power consumption. The average power consumption of comparator block is 139 mW at 5 GHz sampling rate and supply voltage of 1.8 V. The total power consumption of proposed fully parallel A/D Converter is 340 mW. The performance summary and comparison with the other A/D Converter types are shown in Tab. 1

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Received 30 June 2015

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