Journal of ELECTRICAL ENGINEERING, VOL 70 (2019), NO5, 379–385

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PAPERS

Design of a multilayer on-chip inductor by computational electromagnetic modelling

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This paper presents a design of typical multilayer on-chip inductor to determine the layout parameters of the desired inductance value of electromagnetic modeling. The inductance and quality factor of multilayer on-chip spiral inductors are determined by its layout parameters and technological parameters. These layout parameters must be optimized to obtain the maximum quality factor at the desired frequency of operation. An electromagnetic model with fewer assumptions than empirical equations and higher efficiency than full-field solvers would be welcome. So would facile comparisons of different inductor structures. This paper describes recent works on the electromagnetic modeling of on-chip inductor structures applied to the comparison of inductor geometries, including the traditional spiral inductor and a novel multilayer inductor. The electromagnetic modeling of the investigative model is presented. The modeling and simulation are implemented using the method of moments. To simulate the proposed algorithm, the EM Simulator software is used.

K e y w o r d s: inductor, electromagnetic modeling, quality factor, mutual inductance, method of moments

1 Introduction

The multilayer on-chip inductor plays a key role in the design of on-chip radio-frequency (RF) equipment. For circuits such as voltage-controlled oscillators and low-noise amplifiers, the values of the inductance and the Q-factor are essential for the design of spiral inductors. The performance of the spiral inductor depends on the number of turns, line width, spacing, pattern and shape, number of metal layers, oxide thickness and conductivity of substrate. With the appearance of 0.25 μm, 0.18 μm, and recent 0.13 μm CMOS technologies, a complete RF system operating in the gigahertz range can be integrated on silicon with a conventional CMOS process including both active and passive components, such as a wireless transceiver. The on-chip inductor also plays an important role in monolithic RF analog integrated circuits. It is widely used in low-noise amplifiers, mixers, and voltage-controlled oscillators [1].

Obtaining high inductance or high Q for RF circuits with on-chip spiral inductors, which occupy a large surface area, has been a problem. However, the trend has been to pursue better on-chip inductors, for the complete system in a single chip has obvious gains. The search is on for novel on-chip spiral, multilayer and 3-D inductors with large L, small area, low loss and high Q. This requires modeling the inductance characteristics of such structures accurately and efficiently for automated design [2]

Integrating inductors on chip greatly increases system integrity and reduces the packaging parasitic effects. However, because of their large chip area and significant leakage of magnetic energy, on-chip inductors also affect the performance of high-frequency integrated circuits through an electromagnetic coupling [3]. Therefore, it is of great importance to accurately characterize on-chip inductors. Thus, in this study, the design of a typical multilayer on-chip inductor is presented along with its electromagnetic modeling so as to determine the layout parameters of the desired inductance value.

2 Rectangular on-chip inductor design

Conventional on-chip inductor design follows the pattern of metal spirals. The metal is typically chosen to be on the top layer in order to reduce the parasitic capacitance between the metal and the silicon substrate [4–9]. Figure 1 shows a rectangular on-chip inductor.

In order to model the inductance of the entire structure, a rectangular spiral is decomposed into segments, and the total impedance is the summation of the self-impedance of each segment and the mutual impedance between each two of them. The decomposition of a rectangular spiral is illustrated in Fig. 2. N is the number of spiral turns, and the total number of segments is $4N$. A spiral inductor of width 8 μm with four turns was used to lay this out, and the edge-to-edge spacing between parallel segments was 2 μm. The spiral was 11.7 μm above

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DOI: 10.2478/jee-2019–0069, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

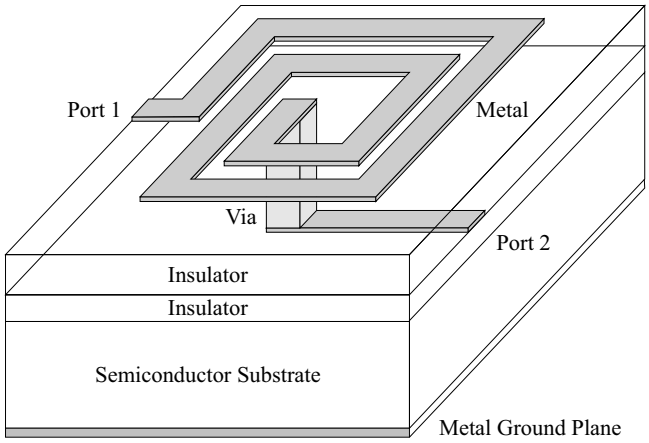

Fig. 1. On-chip rectangular spiral inductor

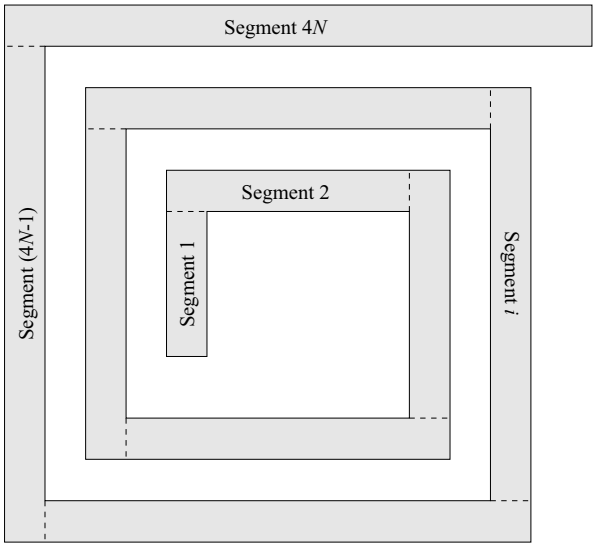

Fig. 2. Decomposition of an N-turn rectangular spiral

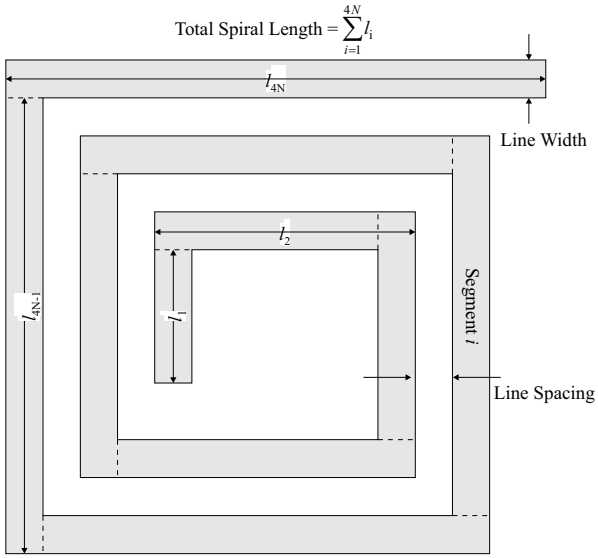

Fig. 3. Illustrations of spiral parameters

a ground plane, and the conductor was assumed to have a thickness of $0.86\,\mu$m. The total length of the inductor was $2000\,\mu$m.

The total AC voltage drop across the two ports of the spiral is the summation of the voltage drop on each segment and is expressed as

$$V = \sum_{i=1}^{4N} V_i \,. \tag{1}$$

According to the inductance definition, the voltage drop on each segment is contributed by both the self-inductance and the mutual inductance between the segment and every other segment and is expressed as

$$V_i = L_i \frac{\mathrm{d}I_i}{\mathrm{d}t} + \sum_{\substack{j=1 \\ j\neq i}}^{4N} L_{\mathrm{m},ij} \frac{\mathrm{d}I_j}{\mathrm{d}t} \tag{2}$$

where L_i is self-inductance, $L_{\mathrm{m,ij}}$ is mutual inductance. Therefore, a matrix of voltage-current relationship can be established as

$$[\,V_1 \quad V_2 \quad \ldots \quad V_{4N}\,]^\top = \begin{bmatrix} L_{11} & L_{m,12} & \ldots & L_{m,1-4N} \\ L_{m,21} & L_{22} & \ldots & L_{m,2-4N} \\ \vdots & \vdots & & \vdots \\ L_{m,4N-1} & L_{m,4N-2} & \ldots & L_{4N-4N} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{4N} \end{bmatrix} \tag{3}$$

where the inductance matrix is

$$\overline{L} = \begin{bmatrix} L_{11} & L_{m,12} & \ldots & L_{m,1-4N} \\ L_{m,21} & L_{22} & \ldots & L_{m,2-4N} \\ \vdots & \vdots & & \vdots \\ L_{m,4N-1} & L_{m,4N-2} & \ldots & L_{4N-4N} \end{bmatrix}. \tag{4}$$

In this matrix, the diagonal elements are the self-inductance of each segment, and the off-diagonal elements

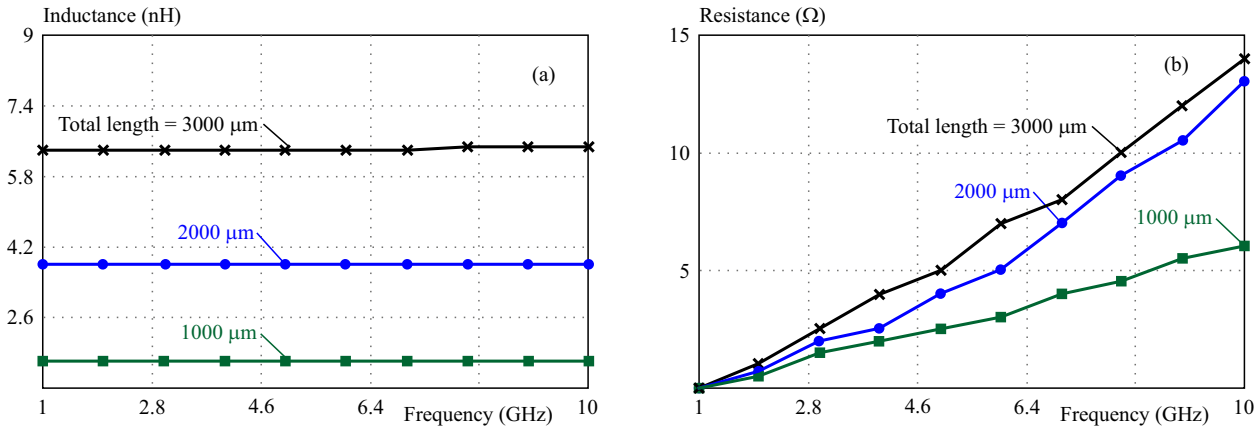

Fig. 4. Spiral inductor impedance with different total spiral lengths versus frequency

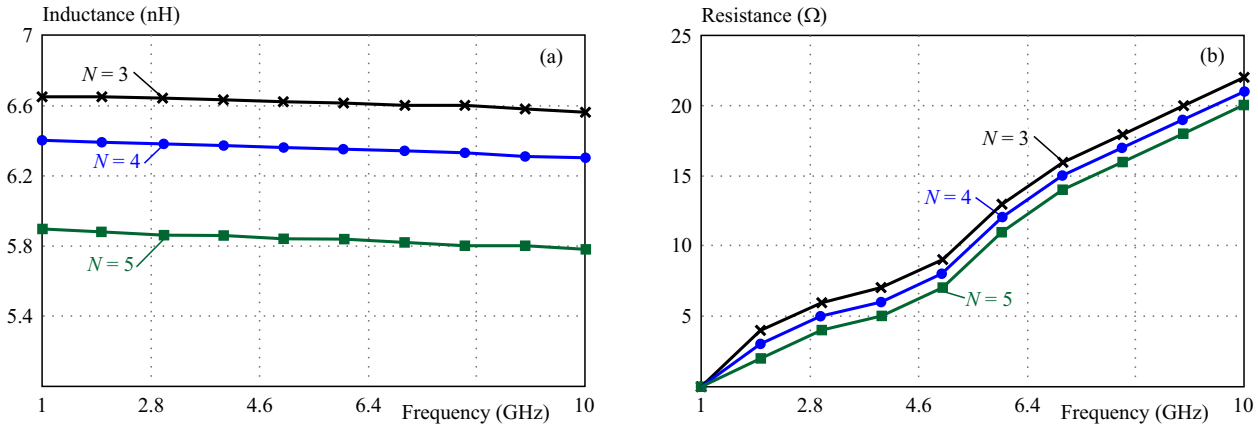

Fig. 5. Spiral inductor impedance with different number of turns versus frequency: (a) – inductance, (b) – resistance

are the mutual inductance between each two segments. Applying (1), the total inductance of the rectangular spiral is the summation of all the elements of the inductance matrix

$$L_{\text{tot}} = \sum_{i=1}^{4N} \sum_{j=1}^{4N} \overline{L}_{ij} \,. \tag{5}$$

Since the inductor is an on-chip component, the inductance of the spiral given by (5) is a complex inductance, which includes both inductance and resistance. The quality factor of an inductor is defined as

$$Q = \frac{\omega L}{R} \tag{6}$$

where ω is the angular frequency, L is inductance and R is resistance.

Quality factor of an on-chip spiral inductor increases with frequency and reaches a maximum value after which it decreases due to the ohmic loss in the series resistance and the loss in the substrate. To investigate the effect of varying width, turns, and spacing on quality factor when the inductance is constant. The quality factor improvement is important for multilayer inductor designs. In the inductor design smaller geometries provide high Q-factors compared to larger coils in the conventional method.

3 Modelling of multilayer on-chip inductors

The inductance of multilayer on-chip inductor depends on several factors such as total spiral length, number of turns, line spacing, line width, and substrate conductivity. These factors are illustrated in Fig. 3. The effects of these factors are studied by computer simulation. Figure 4 plots the impedance of a rectangular spiral with different total spiral lengths versus frequency, while keeping constant the number of turns, line spacing, line width, and substrate conductivity. For this, a 0.25 μm CMOS process is chosen. The spiral is on the Metal 5 layers. The number of turns is set at 4. The line width is set at 8 μm, and line spacing is set at 2 μm. The oxide thickness is 3.96 μm, and the substrate thickness is 250 μm. The metal conductivity is 3.70×10^7 S/m. The substrate doping level is assumed to be 10^{17}cm^{-3}. The total length of the spiral chosen for three different models is 3000 μm, 2000 μm and 1000 μm.

It is seen from Fig. 4 that both the inductance and the resistance of the spiral are roughly proportional to the total spiral length. Therefore, increasing the total length not only increases the inductance but also gives rise to resistive loss and, thus, decreases the inductor quality factor.

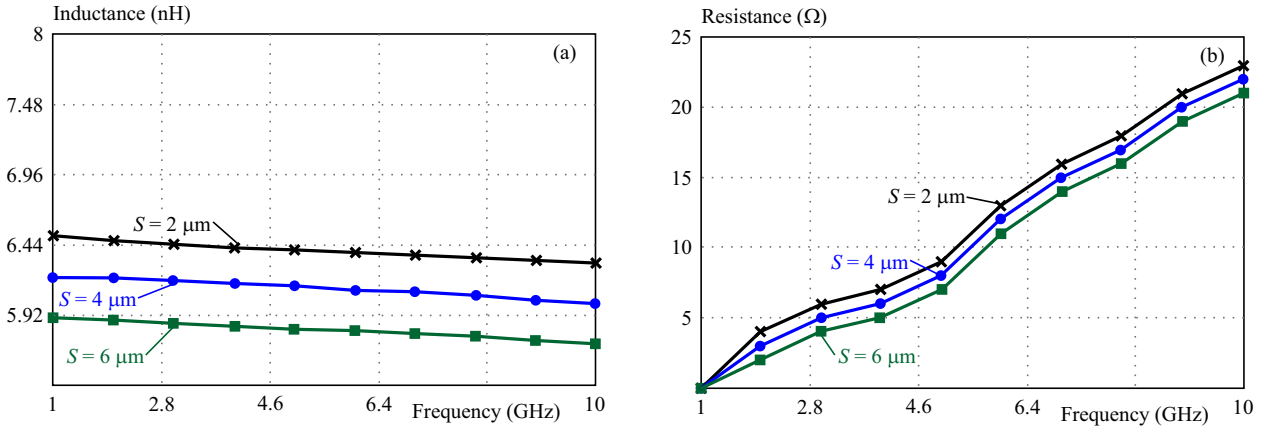

Fig. 6. Spiral inductor impedance with different line spacing versus frequency: (a) – inductance, (b) – resistance

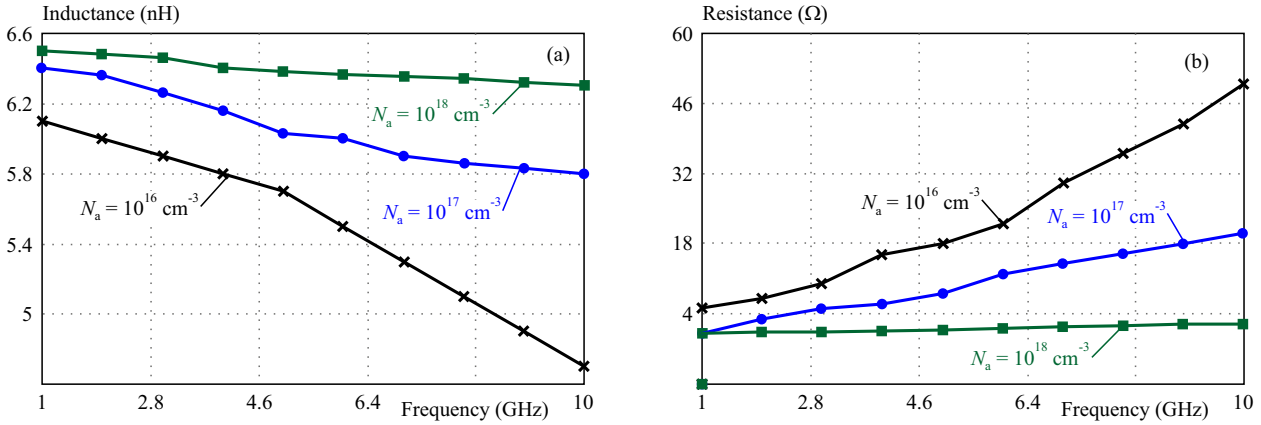

Fig. 7. Spiral inductor impedance with different substrate doping levels versus frequency: (a) – inductance, (b) – resistance

Figure 5 plots the impedance of a spiral inductor with different numbers of turns versus frequency, while keeping constant the total spiral length, line spacing, line width, and substrate conductivity. The spiral parameters are the same as the previous analysis, except that the total length is set at $3000\,\mu$m and the number of turns varies.

It is evident from Fig. 5 that increasing the number of turns can effectively increase the spiral inductance as well as slightly decrease the resistance. This is because increasing the number of turns increases the total magnetic flux of the spiral [10].

Figure 6 plots the impedance of a spiral inductor with different line spacing versus frequency, while keeping constant the total spiral length, number of turns, line width, and substrate conductivity. The spiral parameters are the same as the previous analysis except that the line spacing varies.

It is seen from Fig. 6 that decreasing the line spacing is an effective way to increase spiral inductance without having much effect on the resistance. This is mainly because decreasing the line spacing increases the mutual inductance between the adjacent segments and, thus, the total inductance. The smallest line spacing is limited by the process design rule.

Figure 7 plots the impedance of a spiral inductor with different substrate doping levels versus frequency, while keeping constant the total spiral length, number of turns, line spacing, and line width. The spiral parameters are the same as the previous analysis except that the substrate conductivity varies.

It is seen from Fig. 7 that when the substrate doping level is low (around $N_a = 10^{18}\text{cm}^{-3}$), the inductance increases slightly at higher frequencies. This is because the skin effect in the substrate can be neglected. As a result of the skin effect, the current crowds on the edge of the conductor at higher frequencies. This implies a decreased spacing between the current elements in the adjacent segments and, therefore, an increased mutual inductance. However, if the substrate doping level is high, the spiral inductance decreases with increased frequencies because both the self-inductance of each segment and the mutual inductance between each two segments decreases at higher substrate doping levels. Similar analysis can be applied to spiral resistance, which increases at higher substrate conductivity.

4 Multilayer on-chip inductors design

The conventional spiral inductors are associated with several drawbacks. First, they occupy large chip areas. These include minimizing the noise figure of the amplifier,

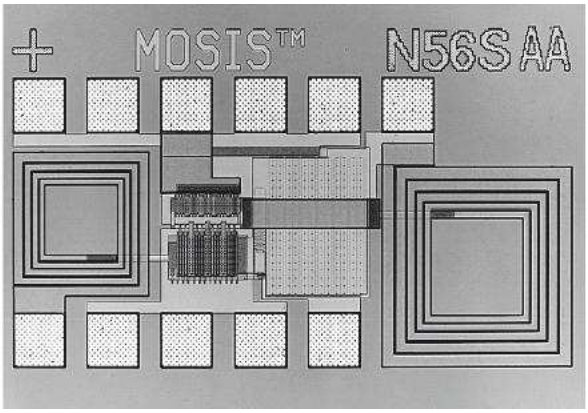

Fig. 8. Die photo of a 1.5 V 1.5 GHz CMOS low-noise amplifier

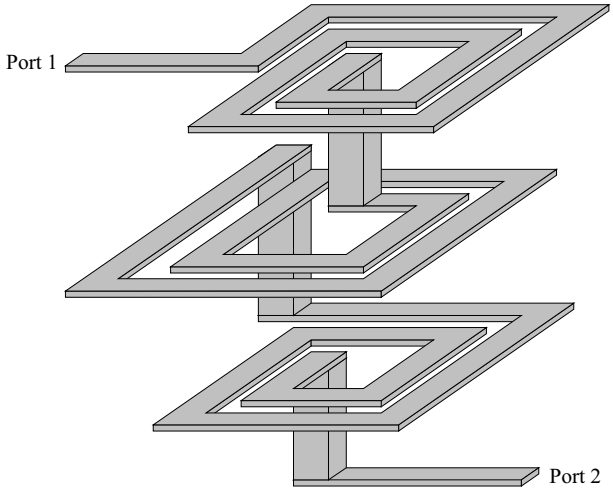

Fig. 9. Illustration of multilayer on-chip inductors

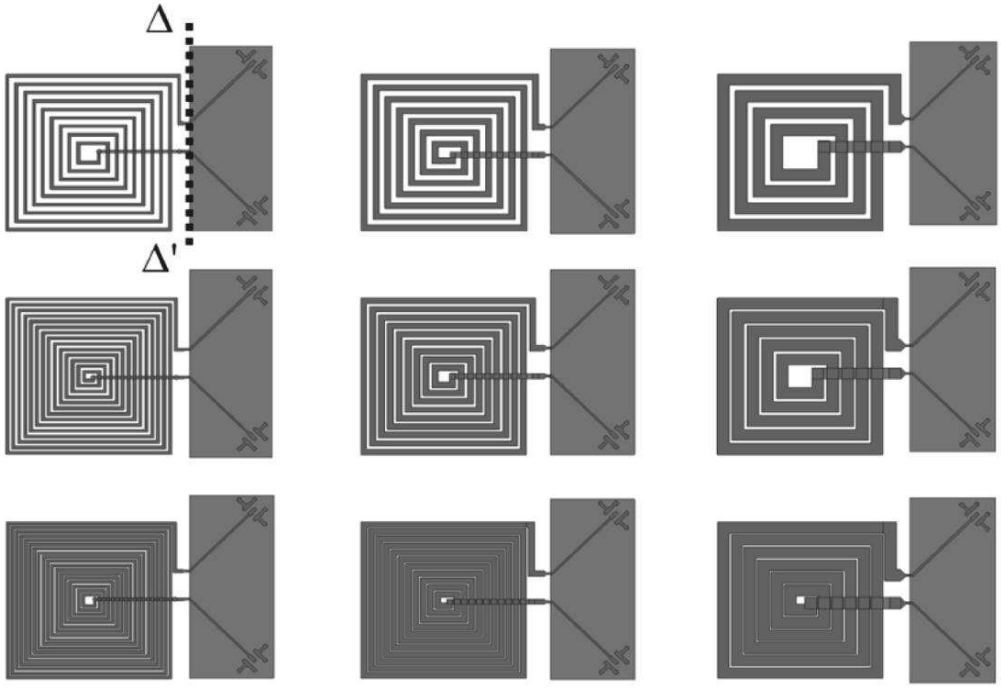

Fig. 10. The layout of multilayer inductor used for computer simulations

providing gain with sufficient linearity and providing a stable 50 Ω input impedance to terminate an unknown length of transmission line. Figure 8 shows the die photo of a 1.5 GHz CMOS low-noise amplifier [11], where two on-chip inductors take about two-thirds of the die area. The input pad is on the lower left corner of the die. The spiral on the left is a 4 nH inductor, and the spiral on the right is a 7 nH inductor that tunes the output of the first stage. The spirals are fabricated in metal [12].

It should be noted that it is hard to fit an inductor of more than 10 nH on a chip. The inductance value is greatly limited for on-chip inductors. As a result, intermediate and low-frequency applications have to turn to off-chip alternatives. Second, because of the lossy semiconductor substrate on which an on-chip inductor is laid out, there is significant resistance as well as capacitive losses associated with on-chip inductors. Therefore, the quality factor of an on-chip inductor is much lower than their off-chip counterparts. The quality factor of on-chip inductors whose inductance is several nH will not go beyond ten in the lower GHz range.

Achieving high quality factor is the key goal of the on-chip inductor design. The inductor quality factor is directly related to the noise performance of RF circuits. An effective way to increase the quality factor of an on-chip inductor without decreasing the inductance is the implementation of multi-layer on-chip inductors. The concept of multi-layer inductors is illustrated in Fig. 9. Its advantage includes the use of multiple metal layers in the conventional CMOS processes. It consists of several stacked N-turn planar spirals. As seen from Fig. 9, all planar spirals have the same direction of current flow (either clock-

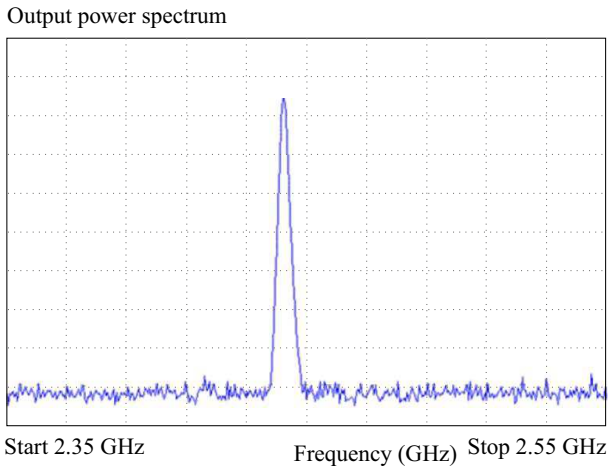

Fig. 11. Output power spectrum

Table 1. Numerical results for planar and proposed inductors

Parameters	Planar	Proposed
Resistance (Ω)	3.117	3.117
Inductor (nH)	1.5	0.452
Length (m)	3000	1000
Area (m)	14884	3186

Table 2. Comparison of planar and proposed inductor Q-factors

f	Q-factor	
(GHz)	planar	proposed
1	1.4	1.8
2	3.0	5.2
3	6.0	8.0
4	4.2	6.8
5	2.8	4.4
6	1.4	1.8

wise or counterclockwise) to maximize the magnetic coupling between them. There are several publications on the experimental investigation of such 3D on-chip inductors [13]. The results of the electromagnetic simulations are verified by measurements of the multilayer spiral inductors. The inductors are processed on a different substrate layer. The different substrate has two 100 μm thick dielectric layers and can be considered a good simulation of a flexible foil substrate.

Multiple inductors with variable track width and spacing are processed in the form of a matrix. Both variations are made simultaneously, thus accounting for unique multilayer spiral inductor designs, as shown in Fig. 10. This metal sheet acted as the ground plane. Based on the observations made on the results of the simulations, a multilayer spiral inductor can be designed. The design of the multilayer spiral inductor for on-chip RF applications is presented. An electrical model parameter is present. The electromagnetic simulations are physically verified by measuring the multilayer spiral inductor designs.

The behavior of spiral inductors is analyzed. Resistive losses and quality factor are modeled by closed expressions that depend on geometrical parameters and the fabrication process. The inductance value is predicted within the limit against measured values for a set of spiral inductors. Our model can predict the frequency at which maximum Q is obtained. This has been validated against measured data [14–16]. This methodology can be extended to other technologies by varying only the technological process parameters. Figure 11 shows the output spectrum of a carrier frequency range from 2.35 GHz to 2.55 GHz. The output power is measured −10.54 dBm at 2.44 GHz.

As Table 1 shows, the proposed inductor saves the area cost. With the fixed resistance, it only uses 20 % of the area occupied by conventional design. Thus, it is more compact and more economic for on-chip design. For future technology generations, as the number of metal levels and the distance from top metal to the substrate will increase dramatically. Even for current technology, the Q factor may not be degraded.

5 Results and discussion

The process parameter variation response is observed in Fig. 4 to Fig. 7 for different total spiral length, different number of turns, different line spacing and different substrate doping, respectively, of same dimensions of inductor structure in three cases. Improving the quality factor is important for all inductor designs. When using an inductor in a circuit where the quality factor is important its resistance becomes an important factor. Any resistance will reduce the overall inductor Q factor. An inductor can be considered in terms of its equivalent circuit.

Achieving high quality factor is the key goal of the on-chip inductor design. The inductor quality factor is directly related to the noise performance of RF circuits. An effective way to increase the quality factor of an on-chip

inductor without decreasing the inductance is the implementation of multi-layer on-chip inductors. The quality factor of planar inductors will be higher than multilayer inductors.

The advantage of the proposed method becomes very clear when the design is compared with planer inductor. The comparison is given in the Tab. 2. The inductor has a peak quality factor of 8 under differential excitation and the frequency of 3 GHz. At 4 GHz the quality factor is around 6.8. The structure is simulated using an EM simulator by defining all the process parameters. The structure was simulated from 1 to 7 GHz. From this proposed technique we can achieve a higher Q factor.

6 Conclusions

In this study, an efficient technique for multilayer on-chip spiral inductor has been developed and tested for many dimensions of the spiral inductor by changing the process parameter such as different total spiral length, different number of turns, different line spacing, and different substrate doping. This technique can achieve a higher Q factor. The proposed multilayer on-chip spiral inductor is designed based on the fabrication rules of 180 nm, which is a layout specific model. The on-chip area of these proposed inductors is very low when compared to planar inductor.

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Received 6 June 2019

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