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PAPERS

Low-power ASIC suitable for miniaturized wireless EMG systems

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Nowadays, the technology advancements of signal processing, low-voltage low-power circuits and miniaturized circuits have enabled the design of compact, battery-powered, high performance solutions for a wide range of, particularly, biomedical applications. Novel sensors for human biomedical signals are creating new opportunities for low weight wearable devices which allow continuous monitoring together with freedom of movement of the users. This paper presents the design and implementation of a novel miniaturized low-power sensor in integrated circuit (IC) form suitable for wireless electromyogram (EMG) systems. Signal inputs (electrodes) are connected to this application-specific integrated circuit (ASIC). The ASIC consists of several consecutive parts. Signals from electrodes are fed to an instrumentation amplifier (INA) with fixed gain of 50 and filtered by two filters (a low-pass and high-pass filter), which remove useless signals and noise with frequencies below 20 Hz and above 500 Hz. Then signal is amplified by a variable gain amplifier. The INA together with the reconfigurable amplifier provide overall gain of 50, 200, 500 or 1250. The amplified signal is then converted to pulse density modulated (PDM) signal using a 12-bit delta-sigma modulator. The ASIC is fabricated in TSMC0.18 mixed-signal CMOS technology.

K e y w o r d s: delta-sigma modulator; EMG system; wireless EMG; ASIC; instrumentation amplifier

1 Introduction

Electromyography (EMG) is a technique for evaluating and recording of electrical activity of skeletal muscles [1]. Standard EMG is acquired using adhesive (non-invasive), or needle (invasive) electrodes, which are now almost entirely disposable. Electrodes are placed on the skin surface, where they are fixed by an adhesive part. There is active part of the electrode coated with conductive gel in the middle. This part is designed to connect the wires through the clip. A signal is transmitted through a wire from the electrode (EMG signal) to an amplifier for further digitization. The digital signal can be processed directly (direct connection to PC), or one can transfer the signal to the PC wirelessly, [2-3]. Wireless transmission is of great importance for the study of motion in which minimum restrictions in movement is required (running, basketball, football *etc*).

Typically, EEG sensor consist of an amplifier with implemented an analog bandpass filter. The amplifiers used biomedical signal processing must meet stringent specifications for low-leakage currents, gain is typically >1000, and their bandwidths reflect the transient nature of the biopotentials. However, surface biopotentials are usually 1 mV or less, even though the source action potentials may be on the order of 100 mV in p-p amplitude [4]. Such signals must be amplified to levels compatible with recording and display devices. The wireless EMG sensors should possess maximized miniaturization and extremely low weight [5-7].

This paper proposes a new sensor (ASIC) for processing of biomedical signals especially EMG signal with the highest possible degree of miniaturization and low power consumption suitable for battery operation. The ASIC is composed of amplifiers, analog bandpass filter and delta-sigma modulator. Instrumentation amplifier together with variable gain amplifier provide overall gain of 50, 200, 500 or 1250. Low-pass (LP) and high-pass (HP) filters (bandpass filter) are implemented separately from amplifier. Designed bandpass frequency is 20–500 Hz. Purpose of the modulator is to convert analog signal to digital for wireless transmission.

2 Application-specific integrated circuit(asic)design

The proposed ASIC, which level block diagram is shown in Fig. 1, consists of several circuits, which are described below. The ASIC takes advantage of novel modulator proposed in [8].

2.1 Instrumentation amplifier

The ASIC consists of two INAs. The first one is supplied by 1.5 V (VDDA). The INA is designed with rail-to-rail input differential pair (consists of both NMOS and PMOS transistors). For this reason, impact of two input differential pairs result into two different sources of mismatch error (INAs offset). Major source of mismatch error depends on INA input voltage level. The second one

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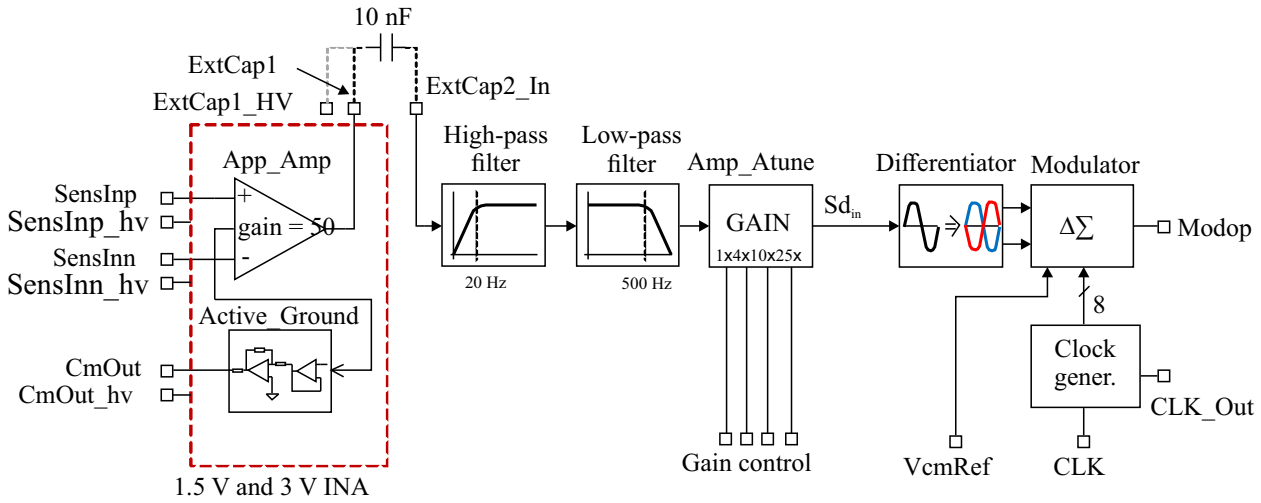

Fig. 1. ASIC level block diagram

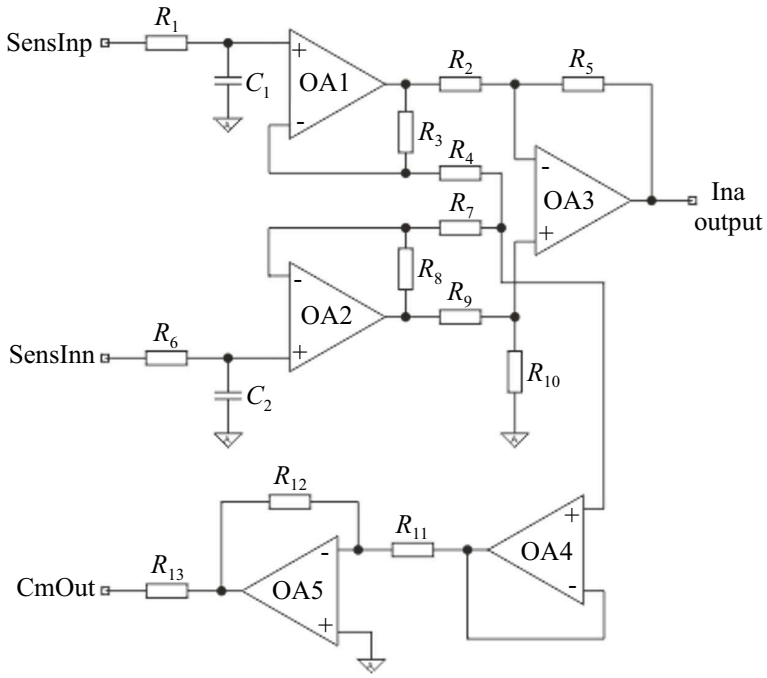

Fig. 2. Circuit diagram of the INA include active ground part

is supplied by higher voltage 3 V (VDDA_HV). Thanks to it, there can be one PMOS differential pair only. The INA offset is given by one source of mismatch error and the offset is independent of the input voltage level. Figure 2 shows internal circuit diagram of the INA including active ground part. For HV version of the INA all operational amplifiers (OA) are replaced with OA powered by 3 V.

Measuring electrodes are connected to the INA, which contains CMOUT output for active ground setting. The main purpose of the circuit for active ground is to decrease INA input noise from electrodes. The circuit has negative feedback, where the noise signal is sent back to patient from internal INA structure. The noise signal is impedance matched, after that is inverted through 390 kΩ, resistance and currently limited (circuit ACTIVE GROUND). The INA voltage gain is given by

$$A_V = \left(1 + \frac{R_3}{R_4}\right)\frac{R_5}{R_2} \tag{1}$$

Gain is fixed to 50. Due to precision matching gain variation is under 1 %.

2.2 Analog filters

The second bloc consists of two second order analog filters (low-pass and high-pass), which remove useless signals and noise with frequencies below 20 Hz and above 500 Hz. The low-pass filter is implemented using active RC circuit with operational amplifier and take advantage of external capacitor due to its high capacity (10 nF). The high pass filter is implemented using Huelsmann structure with on-chip capacitors.

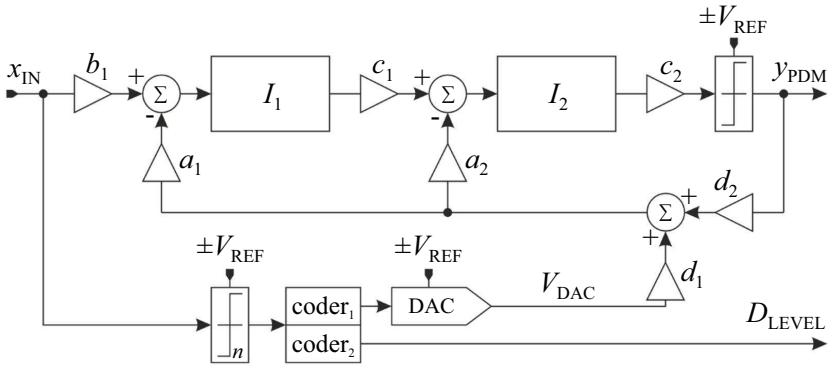

Fig. 3. Circuit diagram of 3rd order ΔΣ modulator

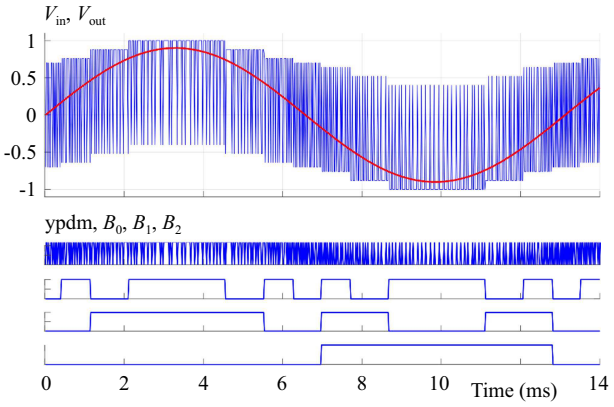

Fig. 4. Waveforms at various nodes of the ΔΣ modulator

2.3 Variable-gain amplifier

The third block is an amplifier with reconfigurable gain (AMP_ATUNE) which can be set by resistor network in amplifier's feedback loop. Matching error of resistor network is under 1 %. Input INA together with the reconfigurable amplifier provide overall gain of 50, 200, 500 or 1250.

$$Gain = A_{\mathrm{INA}}\, A_{\mathrm{TUNE}} \tag{2}$$

where, A_{INA} is 50 and A_{TUNE} is 1, 4, 10 or 25.

2.4 Delta-sigma modulator

For conversion of analog signal into digital delta-sigma converter topology was chosen. This topology is most suitable for high resolution applications due to their high linearity issue. The most important parameters for modulator are overall resolution in specified bandwidth 500 Hz, dynamic input voltage range, power consumption (influence on supply battery life) and chip area. Based on these requirements a 2nd order single-loop modulator was designed. Single-bit, low-order, single-loop delta-sigma modulators are characterized by their stability, simple circuit design, small chip area, linearity, and high transfer coefficient tolerance. However, a high oversampling ratio (OSR) is necessary to provide for a high signal-to-noise and distortion ratio (SNDR). Low-order delta-sigma modulators also suffer from harmonic tones in the output spectrum, which can significantly reduce the achieved SNDR. Due to this reason the system takes advantage of our novel delta-sigma modulator topology presented in [8].

This structure (see Fig. 3) prevents the emergence of higher harmonic tones and decreases the quantization noise in the baseband. An input part of the modulator comprises sample and hold circuit which is designed as fully differential signal converter utilizing switched capacitor technique. The sampled signal passes on to the input of the first integrator as well as to the network consisting of n comparators. These comparators indicate the states where the input signal exceeds certain reference values VREF. (±VREF1, ±VREF2, ±VREF3) Comparators output signals drives the switching of the common reference values added to the signal yPDM. The signal DLEVEL is sent into the digital filter simultaneously. The rule for the coefficients d_1 and d_2 is

$$d_1 + d_2 = 1 \tag{3}$$

then, the signal transfer function (STF) and noise transfer function (NTF) with the coefficients $a_1 = b_1 = c_1 = c_2 = 1$, $a_2 = 2$ are expressed as

$$STF(z) = z^{-2}, \tag{4}$$

$$NTF(z) = (d_2 + d_1 V_{\mathrm{DAC}}) \frac{(1 - z^{-2})^2}{1 - z^{-1} + 0.5 z^{-2}}. \tag{5}$$

The quantization noise id multiplied by coefficient d_2 (where $d_2 < 1$) for a small input signal amplitude. Therefore, it is possible to detect smaller input signal amplitudes, and this precondition subsequently increases the dynamic range of the modulator. The STF and NTF with the transfer coefficients can be described as

$$STF(z) = \frac{b_1 c_1 c_2}{z^2 - (2 - a_2 c_2) z - a_2 c_2 + a_1 c_1 c_2 + 1} \tag{6}$$

$$NTF(z) = \frac{(d_2 + d_1 V_{\mathrm{REF}n})\,(z-1)^2 z^2}{(z^2 - z + 0.5)[z^2 - (2 - a_2 c_2) z - a_2 c_2 + a_1 c_1 c_2 + 1]} \tag{7}$$

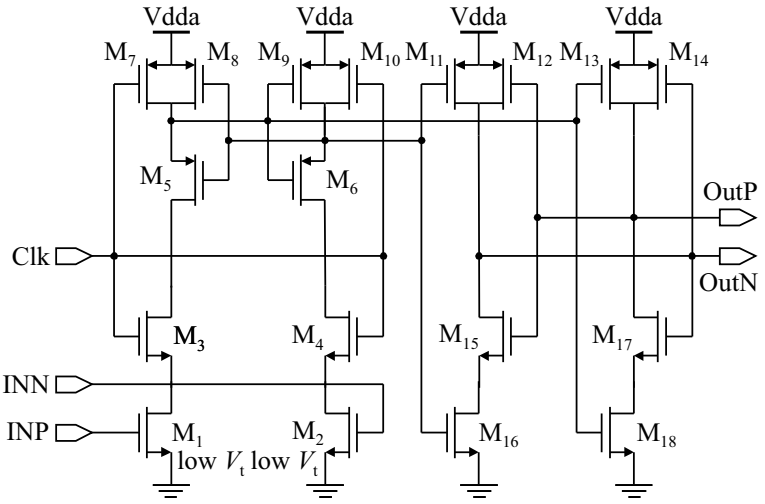

Fig. 5. Circuit diagram of the comparator and latch

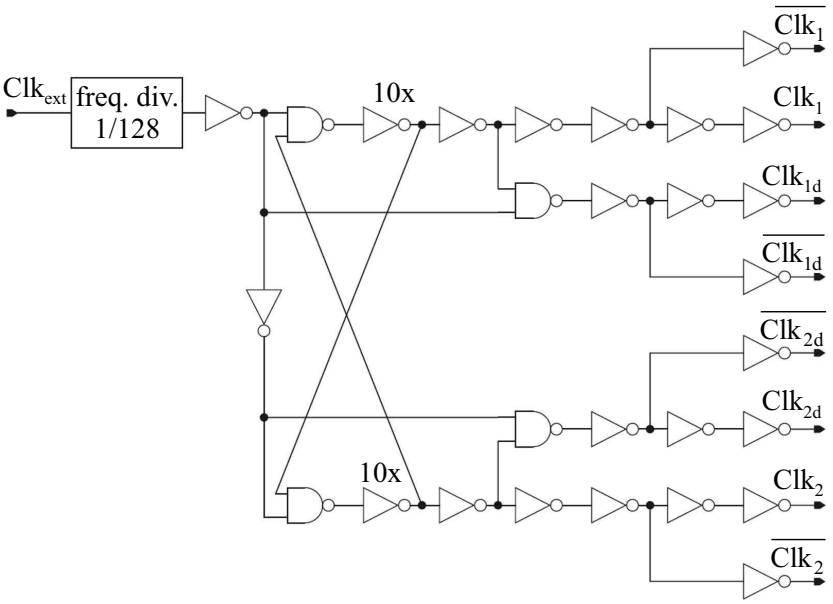

Fig. 6. Non-overlapping clock generator

The accuracy of the analog voltage levels VREF1-3 is not critical, because its possible variations have no impact on the values of the analog VREF or the digital values which are saved in a digital post-processing circuit. In other words, if a comparator output has not changed the output level because of the comparator reference voltage levels inaccuracy or comparator offset, the VREF selection is not altered, and therefore there is no change in the signal level information. This causes only a modification of the input signal range that will be described by the modulator.

The signal level information DLEVEL (B0, B1 and B2) is led outside the ASIC in order to be processed together with yPDM.

To set transfer coefficients a MATLAB model of selected delta-sigma modulator was created. Beside transfer coefficients settings the MATLAB model makes it possible to determine other parameters for analog blocks such as operational amplifiers and comparator (gain, gain bandwidth, slew-rate, offset, *etc*). Size of capacitors are important for two reasons mismatching error and thermal noise. Therefore, the first integrator has larger capacitors size (integrating $C_{\mathrm{I}} = C_s = 6$ pF MIM capacitor with 2 fF/μm^2 because errors in the first integrator has the most significant impact on signal-to-noise ratio (SNR) of the delta-sigma modulator. Second integrator has capacitors $C_{\mathrm{I}} = C_s = 2.5$ pF and $C_s(a_2) = 5$ pF.

The modulator works in fully differential mode, therefore operation amplifier with fully differential output was required. Two-stage structure without cascade was chosen. This structure provides high gain, low noise and possibility of low voltage supply voltage. Designed parameters are gain = 80 dB, gain bandwidth = 12 MHz, phase margin = 60°, slew rate = 13 V/μs, power consumption = 200 uW at 1. 5 V supply with total area of 0. 022 mm

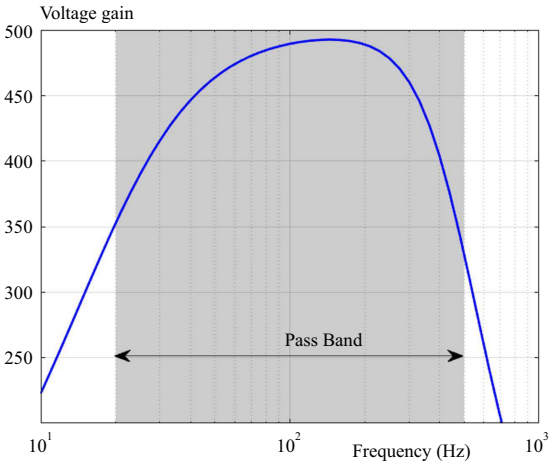

Fig. 7. Measured bandpass characteristic

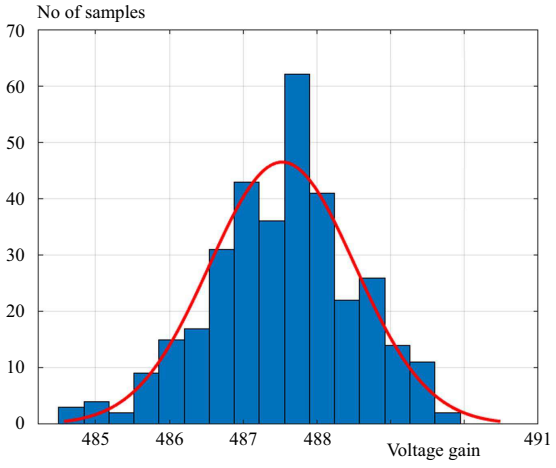

Fig. 8. DC transfer Monte Carlo statistical analysis

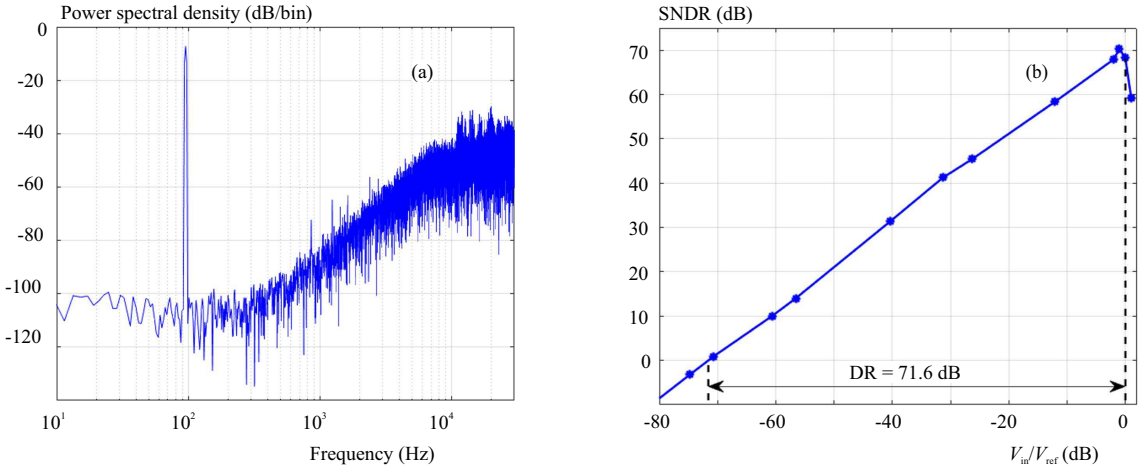

Fig. 9. Delta-sigma modulator measurement results,(a) – power spectral density, and (b) – dynamic range

^{2}. Maximum power supply is 1. 8 V. These parameters were verified with corner analysis (process variations).

Next important building block is a comparator (quantizer). The comparator can work at hundreds Hz clock frequency and consumes dynamic power only. As the offset requirement is quite relaxed, no pre-amplifier is used in front of the comparator (Fig. 5). The output of the comparator is lead throug SR latch of 0.032 mm^2 area.

A schematic of the clock generator circuit is shown in Fig. 6. It is driven by a reference clock provided from an external source and is followed by frequency divider which divides the frequency of the input signal by 128. Two non-overlapping clocks are generated from it to operate switched-capacitor integrators. The non-overlapping interval is created by a propagation delay in inverter chains. An additional pair of delayed clock phases is also generated for a bottom-plate sampling technique to reduce charge injection errors. All these clocks are generated include a negative form for complementary CMOS switches. Clock phases are distributed by eight local clock signals.

3 Experimental results

The proposed ASIC has been designed and fabricated in TSMC 0. 18 μm CMOS IC technology. The integrated circuit, occupying 1.6 mm $\times$ 1.6 mm area and consisting of two instrumentation amplifiers, LP and HP filter, variable-gain amplifier, delta-sigma modulator and a bias circuit. The IC is covered by dummy layers which are necessary due to the technology requirements for minimum layer density in an area. Only top metal 6 is visible in the micrograph.

The chip has three independent power supplies: two for analog blocks and one for the digital domain (clock generator, digital I/O cells). The nominal measurement conditions were at a supply voltage of 1.5V and a reference voltage of 750 mV. Since the analog and digital power supplies are separated, an individual power measurement was possible. A 3 V power supply is utilized by HV INA for testing purposes. The system was measured as a whole. The input data is generated by a 16-bit DAC and, together with output stream of the modulator, are stored in a memory and transferred to PC. Consequently, data is processed by MATLAB software. Figure 7 shows

the measured AC transfer characteristic using a gain of 500. Peak gain is 488, cutoff frequencies are 19 Hz and 505 Hz, respectively.

The gain can be set by four external signals which are connected to CMOS switches located in resistor network in OA feedback loop. Owing to an advanced layout technique, matching error of the resistor network is under 1 %. Overall gain of the system was measured. Due to the low number of samples additional Monte-Carlo analysis covering process and mismatch errors was performed (Fig. 8). Simulated mean gain (487.5) corresponds to measured gain (488 at 200 Hz). Expected variation of the gain is 3 in case of 3 σ.

The delta-sigma modulator was measured discretely using external input pin SDIN established for measurement purposes. The output data of the modulator is stored in a memory and transferred to PC. Consequently, data is processed by MATLAB software. The oversampling ratio is 64, 128 or 200. Figure 9(a) shows the measured output spectrum of a 99 Hz signal. A peak SNDR of 72.1 dB has been reached in 500 Hz signal bandwidth. Figure 9(b) shows the SNDR curve *vs* the input signal amplitude. The modulator reaches a dynamic range (DR) of 71.6 dB.

Table 1. Summarized parameters of the ASIC

	Condition	Value	Unit
Technology	TSMC 0.18 CMOS		
Supply voltage (VDDA)	1–1.8* (3 at VDDA_HV)		V
Max. input signal amplitude		VDDA	V
Power consumption	max. at OSR=200	2.9	mA
Gain	50	49	V/V
	200	195	V/V
	500	488	V/V
	1250	1230	V/V
Resolution	OSR		
	64	11.7	bits
	128	14.5	bits
	200	15.9	bits
Input noise		1.8	$\mu V/\sqrt{Hz}$
Chip die area		2.56	mm^2

The summarized parameters of the designed ASIC are presented in Tab. 1. The chip die area is 2.6 mm^2, while the area without bond pads corresponds to 1. 3 mm^2.

4 Example of application

This chapter presents utilization of the ASIC in a miniaturized wireless electromyogram (EMG) system for the measurement of electrical activity of muscles. The system consists of MCU, EMG electrodes, ASIC - based sensor device, RF module and logger (PC). The prototype is powered by 3V button cell (LR44). Sensing electrodes are placed in the non-conductive "patch" which is used to attach the electrodes, but also as a carrier of the necessary electronics. The patch is easy to stick to the place of shooting without the need to install additional wiring and electronics.

The patch will automatically activate itself after sticking to the shooting location. In order to restrict the movement of individual patch, the part made of flexible material. All necessary parts (ASIC, MCU, RF module include antenna, battery) are part of the patch. Each patch has its own unique code transmitter, which can be retrieved using the bar code on the package and facilitate identification of the system. There is a transmitter with low power and reach in units of meters. In order to reach higher range, transponders, which will be in the vicinity of transmitters or will be carried by the individual, can be used. All structures patches are flat and completely sheltered from water. This allows to use (acquiring EMG) in an environment with water or wear any clothing over the sensor.

The main parameters that were considered for component selection are power consumption and area. Selected components including power consumption are summarized in Tab. 2.

Table 2. Selected components in the system

Part	Selected component	Consumption mode active (mA)	Consumption mode power-down (μA)
MCU	ATmega88	1.8	5
Sensor	Proposed ASIC	2.9	2900
RF Module	NRF24L01	12.3	0.9

Overall consumption is 17 mA in active mode if data are sent continuously from patch to logger (PC). However, data are not typically sent continuously. How frequently depends on the measurement setup. Capacity of LR44 battery is given by discharging conditions and is 100-120 mAh. It provides 6-7 hours of operation in case of continuous data sending.

5 Conclusion

In order to design miniaturized smart low weight biomedical signal processing systems, the low-voltage low-power integrated ASIC has been developed. The ASIC contains two instrumentation amplifiers, analog filters, a variable-gain amplifier and 12-bit delta-sigma modulator. Overall power consumption is 4.4 mW, while the chip area corresponds to 2.56 mm^2. The circuit has been designed and fabricated in TSMC 0.18 μm CMOS

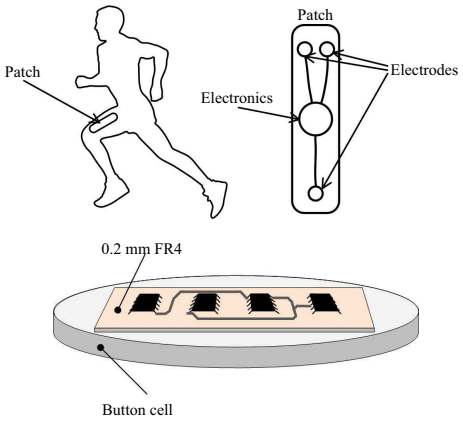

Fig. 10. Patch can be placed on the thing

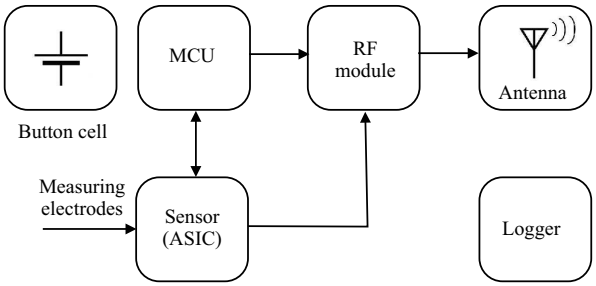

Fig. 11. System architecture

IC technology. The proposed circuits are suitable for various applications demanding low-voltage low-power consumption, mainly for biomedical implantable and battery equipped devices. An example of application demonstrated that it is possible to implement the ASIC in modern miniaturized low-power biomedical system.

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